EDT for Power Devices

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Power electronics requirements

Review of PCB-based packaging

Proposed Embedding Technique



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Layout of a power electronic device





- ► 1-2 pads on top, one on the bottom
- ► 50-400 µm thick, 1-100 mm² die area

Geeps

- Usually AI on top, Ag on the back
- Up to hundreds A/thousands V



- ► Junction temperature up to 175 °C (Si)
- Efficient cooling to avoid thermal runaway
- Ceramics often used







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- Standard Power Modules offer good thermal management
- Well suited to higher voltages (>1200 V)
- Issues: large, not flexible, and high parasitic inductance





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Effect of the Packaging on Electrical Performance



- Stray inductances cause ringing and switching losses
- Caused by packaging
- Issue highlighted by fast WBG semiconductors



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Active devices – Evolution of the Packaged Devices



source: wikimedia commons for all packages except the Directfet, courtesy International Rectifier, and the WL-CSP, c.f. below

| Package type | Volume (mm ³) | molding compound% | silicon % | leadframe % | interconnect % |
|--------------|---------------------------|-------------------|-----------|-------------|----------------|
| DPAK | 90 | 75 | 4 | 20 | 1 |
| SO8 (wire) | 28 | 83 | 6 | 10 | 1 |
| SO8 (clip) | 28 | 70 | 6 | 20 | 2 |
| MOSFET BGA | 20 | 0 | 40 | 50 | 10 |
| WL-CSP | 20 | 0 | 82 | 0 | 18 |

source for table and bottom figure: "Trends of power semiconductor wafer level packaging", Yong LIU [2]

- Gradual disappearance of the FLP (First Level Packaging)
- All fabrication steps made directly on wafer: Wafer Level-Chip Scale Packaging



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Literature Review - Converter on a flex substrate

- Flex PCB instead of wirebonds
- backside attached to a DBC
- advantages:
 - low profile, low inductance
 - higher interconnect density
- Implementations:
 - ▶ GE [3]
 - ► CPES [4]
 - ► TU Berlin/Fraunhofer Inst. [5]
 - Semikron [6]...



images from ECPE Seminar "Power PCBs and Busbars", Delft, 2008, Papers: [7, 8]



T. Stockmeier et al. "SKIN: Double side sintering technology for new packages", ISPD 2011



Literature Review - "PCB-like" 3D structures



module", IEEE Trans on PE vol 25, 2010, 25, 2059

Silver-sintered interconnects and Epoxy/Kapton insulation [9]



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Original chip on DCB



Isolation by lamination



Laser structuring



Metallization



Photostructuring and Electroplating





Difference etching/Finish



Weidner, et al. "Planar Interconnect Technology for Power Module System Integration", CIPS 2012

SiPLIT Copper electroplating, laminated isolation laser-structured *in-situ* [10]

Literature Review – Die embedding in PCB

Low-inductance packaging for SiC [11]

- Half bridge module
- 0.8 nH loop inductance
- Embedding die using stud bumps



E. Hoene, "Ultra Low Inductance Package for SiC" ECPE workshop on power boards, 2012



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- Power module development through german project Hi-LEVEL [12]
- 10 kW and 50 kW demonstrators
- Thick copper or DBC for thermal management

http://www.pcdandf.com/pcdesign/index.php/editorial/menu-features/9257-component-packaging-1405



Power electronics requirements

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- Start with a DBC substrate
- Die attach (silver sintering)
- PCB stacking
- PCB lamination
- Topside copper etching
- Laser ablation
- Copper electroplating





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Backside die attach with silver sintering:

- The die does not move during assembly
- Accurate positioning
- Ablation using a CO₂ laser
 - Very good selectivity (metal layers insensitive to laser light) I use of the cooper layer as an alignment mask
- Prototype-scale equipment used
 - Can manufacture prototypes from 4x4 cm² up to 21x28 cm²
 - Affordable, useful for process development.



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Need for a suitable topside finish for electroplating : copper





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Cross section





- Vertical walls in epoxy layers
- Good self-alignment
- No degradation of die topside metal due to CO₂ laser
- Die contact not yet perfect





- Thick topside copper foil (35 μ m)
- Thin electroplated copper (10 μ m)

Many wells:

More copper section on walls

Large well(s):

Thicker die contact metallization
 reduction of topside copper section





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Electrical Characterization



Tests performed in air, without additional passivation

 Most important parameter for contact resistance: distribution of contacts over die area



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Embedding of power devices

- Scalable technology
- Allows for more compact systems
- Custom design
- Attractive for fast, wide-bandgap devices

Simple process

- Lab-scale process presented
- Good compatibility with CO₂ lase
- Main issue: die topside finish

Developments to come:

- Half-bridge with gate drivers.
- Multi-layer design
- Embedding of passive components
- Work on thermal design





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Geeps

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