

Comparison of topside contact layouts for power dies embedded in PCB

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Chenjiang Yu¹, Cyril BUTTAY², Éric LABOURÉ¹,
Vincent BLEY³, Céline COMBETTES³, Gilles BRILLAT³

¹GEEPS, Paris, France

²Laboratoire Ampère, Lyon, France

³LAPLACE, Toulouse, France

14/09/16

Introduction

Proposed Embedding Technique

Effect of Contact Area/Layout

Summary and Conclusion



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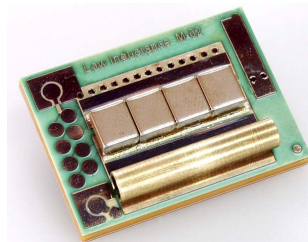
Summary and Conclusion



Advantages of die embedding

The Printed-Circuit-Board technology (PCB) enables:

- ▶ higher interconnect density
 - ▶ multi-layer
 - ▶ small pitch (down to 25 μm linewidth)
- ▶ Low inductance [1]
 - ▶ small size
 - ▶ laminated busbar structure
- ▶ batch-processed manufacturing
 - ▶ all interconnects are processed at once



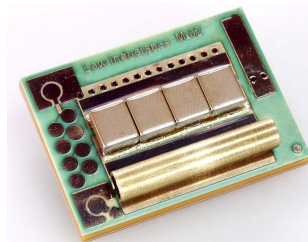
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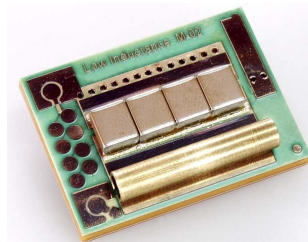


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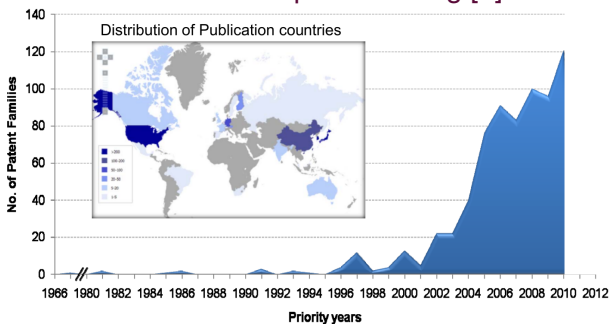
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Patents on chip embedding [2]



A. Ostmann, "Leistungselektronik in der Leiterplatte" AT&S Technologieforum, 2013

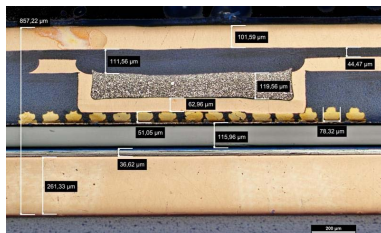
- ▶ Very active area in recent years
- ▶ Many applications to high interconnect density
- ▶ Several industrial developments (AT&S, Schweizer, etc.)



Literature Review – Die embedding in PCB – 2

Low-inductance packaging for SiC [1]

- ▶ Half bridge module
- ▶ 0.8 nH loop inductance
- ▶ Embedding die using stud bumps

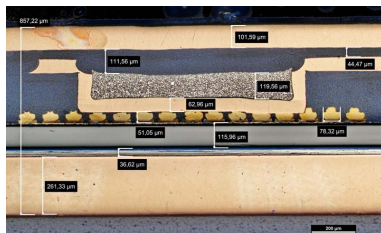


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- ▶ Power module development through german project Hi-LEVEL [3]
- ▶ 10 kW and 50 kW demonstrators
- ▶ Thick copper or DBC for thermal management

<http://www.pcdandf.com/pcdesign/index.php/editorial/menu-features/9257-component-packaging-1405>



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Overview of the process



- ▶ Start with a DBC substrate
- ▶ Die attach (silver sintering)
- ▶ PCB stacking
- ▶ PCB lamination
- ▶ Topside copper etching
- ▶ Laser ablation
- ▶ Copper electroplating



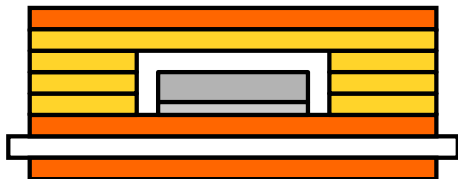
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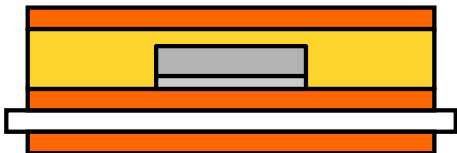
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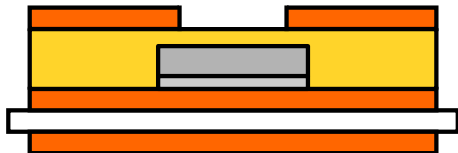
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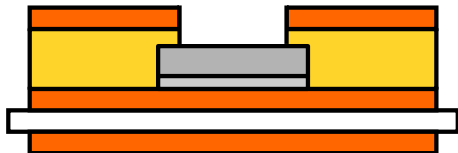


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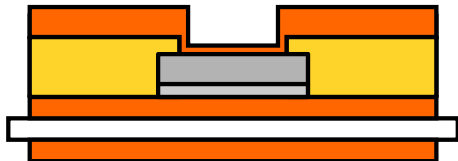
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Overview of the process – significant points

- ▶ Backside die attach with silver sintering:
 - ▶ The die does not move during assembly
 - ▶ Accurate positioning
- ▶ Ablation using a CO₂ laser
 - ▶ Very good selectivity (metal layers insensitive to laser light)
 - ▶ Use of the copper layer as an alignment mask
- ▶ Prototype-scale equipment used
 - ▶ Can manufacture prototypes from 4x4 cm² up to 21x28 cm²
 - ▶ Affordable, useful for process development



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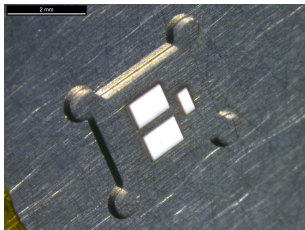
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- ▶ Ti/Cu PVD with a shadow mask (50/500 nm)
- ▶ Simple process for singulated dies



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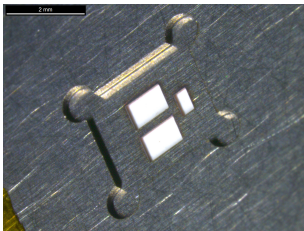
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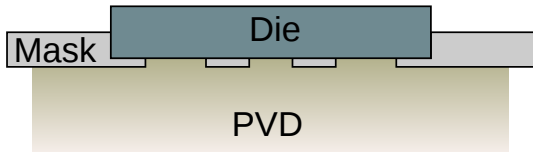
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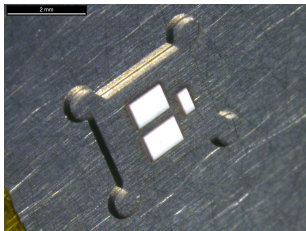
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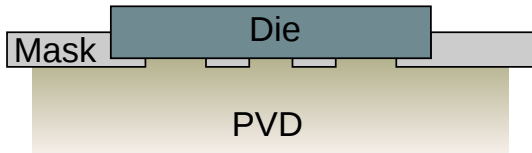
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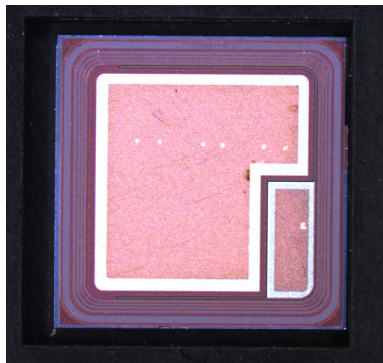
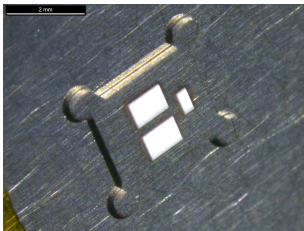
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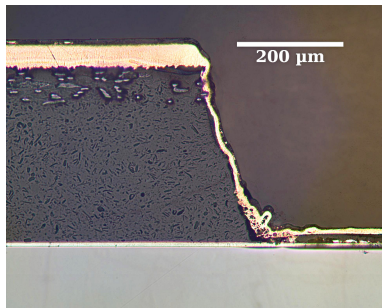
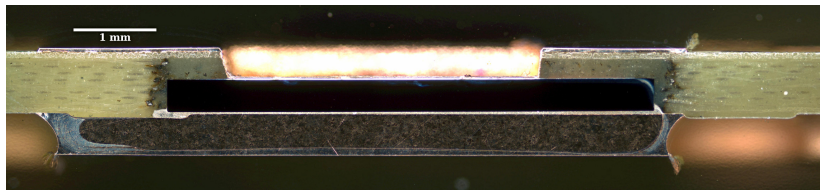
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5×5 mm² IGBT die



Cross section



- ▶ Vertical walls in epoxy layers
- ▶ Good self-alignment
- ▶ No degradation of die topside metal due to CO₂ laser
- ▶ Die contact not yet perfect

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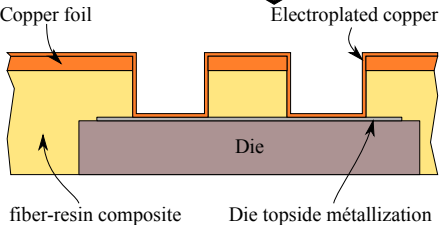
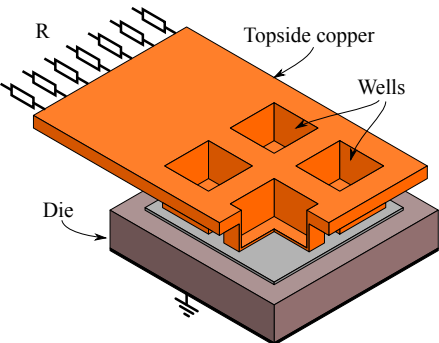
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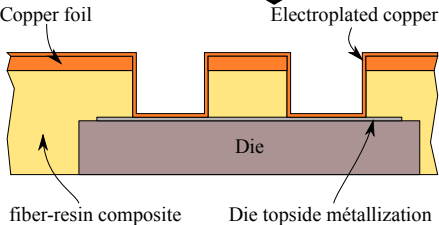
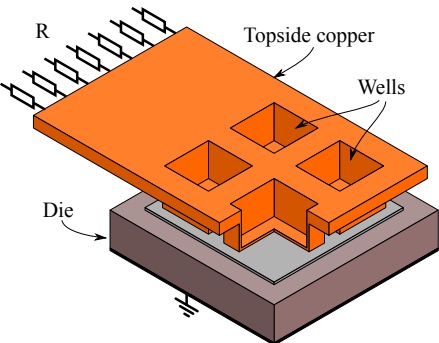


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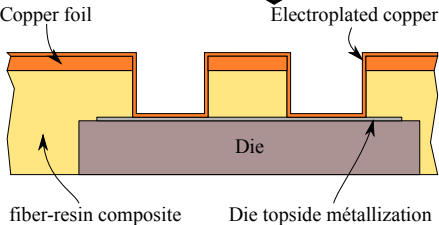
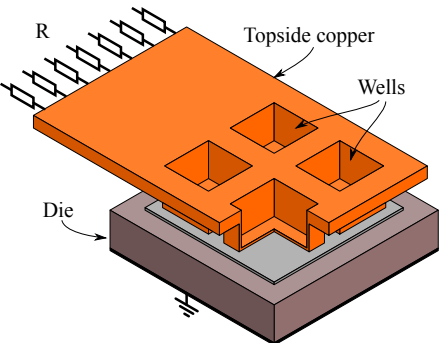
- ▶ Thick topside copper foil ($35 \mu\text{m}$)
- ▶ Thin electroplated copper ($10 \mu\text{m}$)
- ▶ Many wells:
 - ▶ Move copper section on walls
- ▶ Large well(s):
 - ▶ Thicker die contact metallization
 - ▶ reduction of topside copper section

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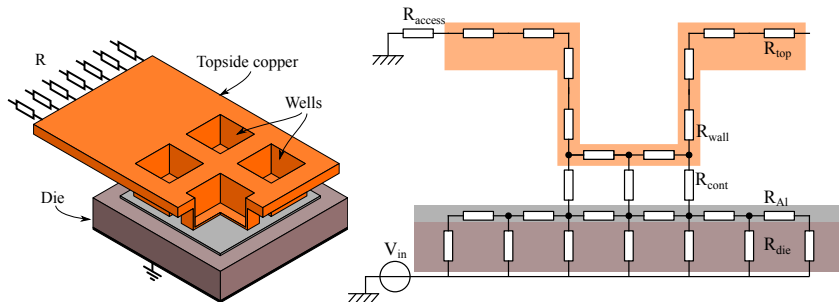
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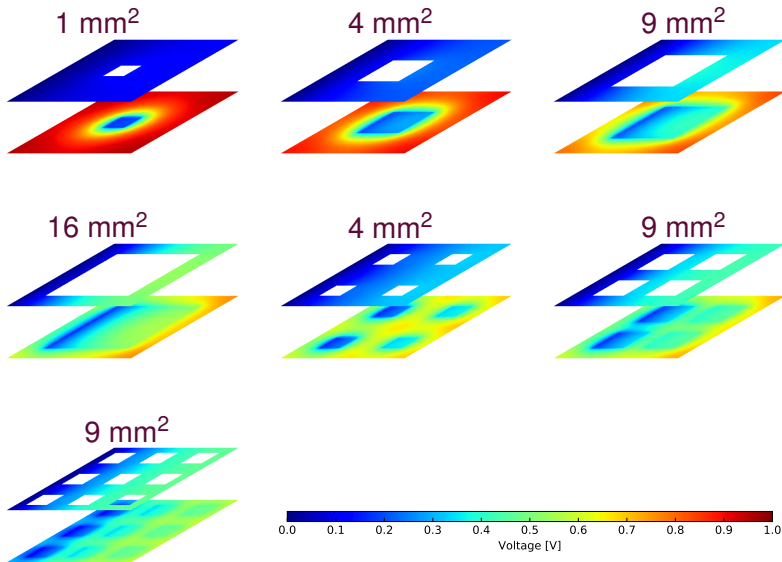
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Modelling



- ▶ Structure divided into $100 \times 100 \mu\text{m}$ cells
- ▶ 2-D current flow assumed
- ▶ Generation of a meshed circuit of resistors
- ▶ Solving using Modified Nodal Analysis.

Modelling — Results

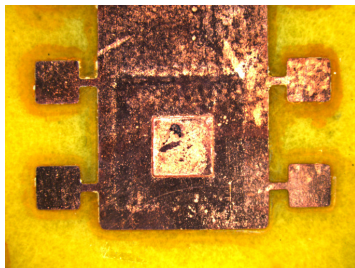
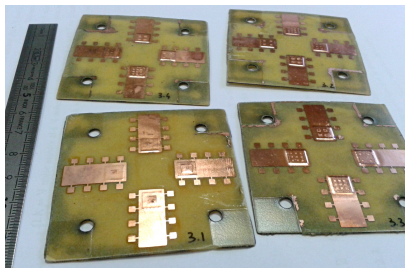


# of contacts	Surface (mm ²)	Resistance (mΩ)
1	1	3.80
1	4	2.16
1	9	1.55
1	16	1.32
4	4	1.40
4	9	1.26
9	9	1.13

Resistance decreases with:

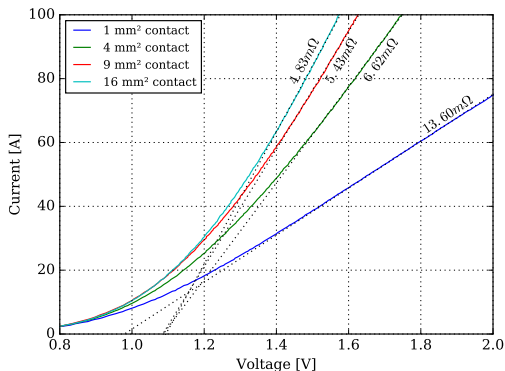
- ▶ Contact area
- ▶ Contact distribution
- Well spread contacts are more efficient
- split 4 mm² contact comparable to single 16 mm²

Experimental Validation — Test Vehicles



- ▶ $6 \times 6 \text{ mm}^2$ diodes embedded in PCB
- ▶ 4-point connexions for accurate resistance measurement
- ▶ high current (up to 100 A), pulsed measurement

Experimental Validation — Test Results



# of contacts	Surface (mm ²)	Resistance (mΩ)
1	1	16.5
1	4	5.6
1	9	4.9
1	16	4.7
4	4	5.4
4	9	4.4
9	9	5.2

- ▶ Resistance value extracted from I(V) characteristic of diode
- ▶ Large scattering of experimental data ($\pm 20\%$)
- ▶ Same die in standard TO-247 package: 4.4 mΩ



Contact Resistance — conclusions

- ▶ Contact distribution is important, contact area not so much
- ▶ Experimental results show same trend as simulation
 - ▶ Resistance 4 times higher!
 - ▶ Resistance equivalent to that of (commercial) wirebonded dies



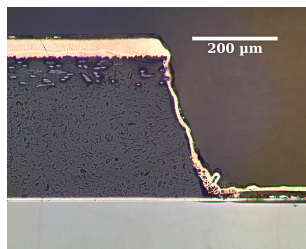
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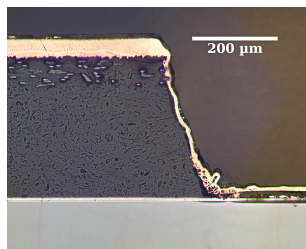
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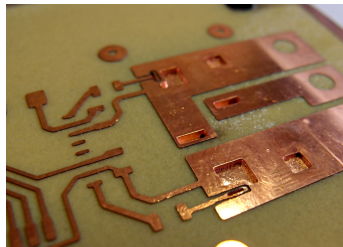
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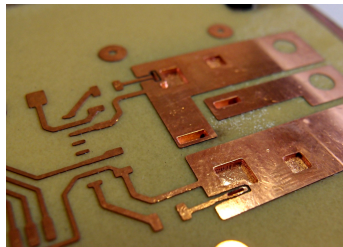
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 - ▶ Custom design at die level
 - ▶ Attractive for fast, wide-bandgap devices
 - ▶ Contact layout allows for better current spreading
- ▶ Simple process
 - ▶ Lab-scale process presented
 - ▶ Low contact resistance achieved
 - ▶ Main issues: die topside finish
- ▶ Developments to come:
 - ▶ Half-bridge with gate drivers
 - ▶ Embedding of passive components
 - ▶ Work on thermal design



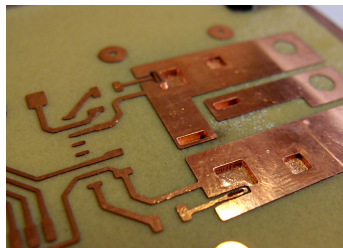
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-  A. Ostmann, L. Boettcher, D. Manassis, S. Karaszkiwicz, and K.-D. Lang, “Power modules with embedded components,” in *Microelectronics Packaging Conference (EMPC) , 2013 European*, pp. 1–4, Sept. 2013.



Thank you for your attention

contact: cyril.buttay@insa-lyon.fr

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