

# High temperature operation of SiC transistors

ATW on Thermal Management, Los Gatos

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23/9/15

Introduction

High-Temperature behaviour of SiC Devices

Packaging for high-temperature converters

Conclusion

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Vehicle Location	Max Temp (°C)
Drive train high temp location	177
Floor	85
Near radiator support structure	100
Back of alternator	160
Cooling circuit	120
Exhaust manifold	649



Most data: Kassakian, J. G. et al. "The Future of Electronics in Automobiles", ISPSD, 2001, p 15-19

- ▶ Low-cost, high-volume applications;
- ▶ Moving to higher voltages (12V->300V for hybrids)
- ▶ Little cooling headroom with silicon devices ( $T_J=150$  to  $175^\circ\text{C}$ )

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  - ▶ Little cooling headroom with silicon devices ( $T_J=150$  to  $175^\circ\text{C}$ )
- ⇒ dedicated cooling circuit for power electronic systems



## The trend:

- ▶ Hydraulic, Pneumatic and Electric networks co-exist in current systems
  - ▶ More-electric aircraft should reduce complexity
  - ▶ objective: 1 MW on-board electrical power
- 
- ▶ From mild to very harsh:
    - ▶ Some systems are located in the cabin
    - ▶ Jet engine actuator will face  $-55^{\circ}\text{C}$  to  $225^{\circ}\text{C}$  cycling
    - ▶ Many systems are located in non-pressurised areas
  - ▶ Long system life: around 30 years
  - ▶ Reliability is the main concern



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- ▶ NASA missions to Venus and Jupiter
  - ▶ Venus surface temperature : up to 480°C
  - ▶ Pressure a few kilometres inside Jupiter: 100 bars, at 400°C
- ▶ Strong thermal cycling, as temperature can drop to 140K at night;
- ▶ Other awful conditions: winds, corrosive gases. . .

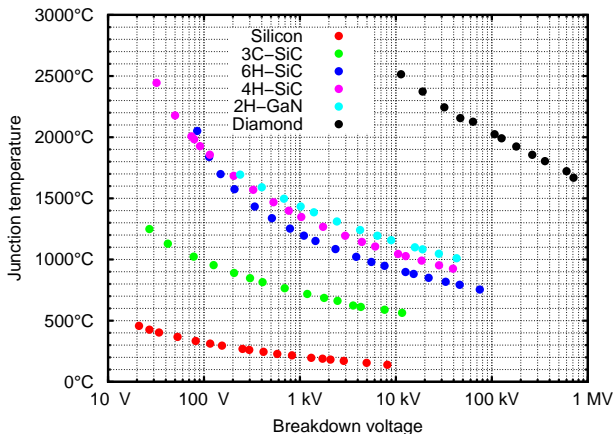


# Deep oil/gas extraction



- ▶ Continuous operation, relatively low cycling
- ▶ Deep drilling: high ambient temperature (up to 225 °C)
- ▶ Expected lifetime: 5 years
- ▶ Main requirement: sensors and datalogging
- ▶ Example of new applications: downhole gas compressor

# Maximum operating temperature



Silicon operating temp is intrinsically limited at high voltages.

- ▶ 1200 V devices rated at <200 °C junction temperature

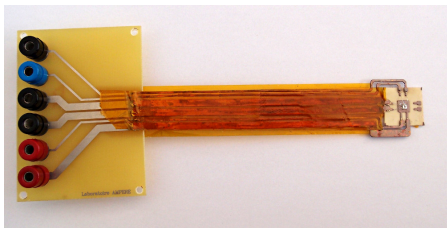
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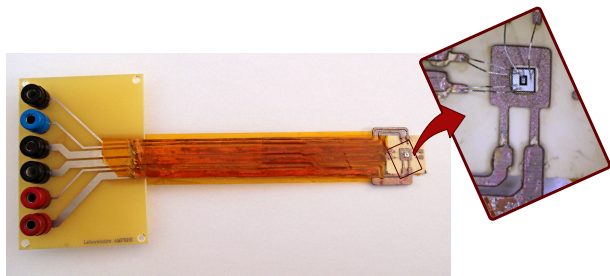
# Test configuration



- ▶ High temperature test system
  - ▶ Silver-sintered interconnects
  - ▶ Ceramic substrate (DBC)
  - ▶ Copper-kapton leadframe
- ▶ DUT: 490 m $\Omega$  SiC JFET from SiCED
- ▶ characterization:
  - ▶ Tektronix 371A curve tracer
  - ▶ Thermonics T2500-E conditioner

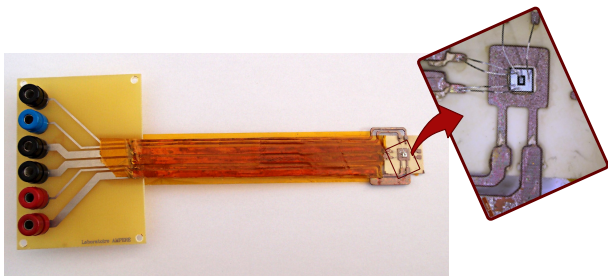


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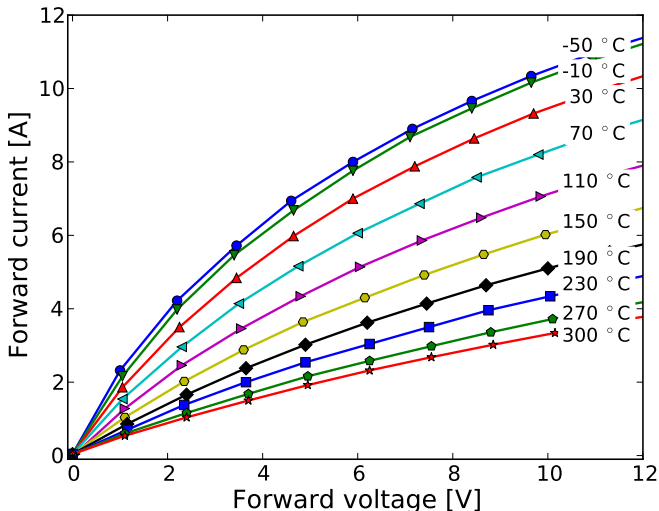
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Source: Thermonics T-2500E Datasheet

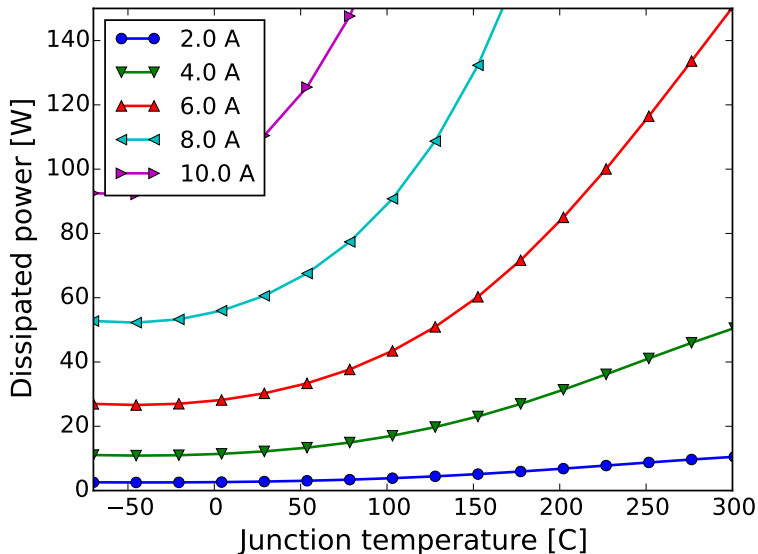
# Static Characterization of 490 mΩ JFET

Buttay et al. "Thermal Stability of Silicon Carbide Power JFETs" IEEE transactions on Electron Devices, 2013, 60, 4191-4198

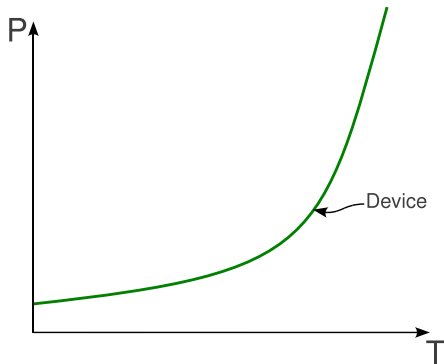


$V_{GS} = 0$  V, i.e. device fully-on

# Power dissipation as a function of the junction temp.

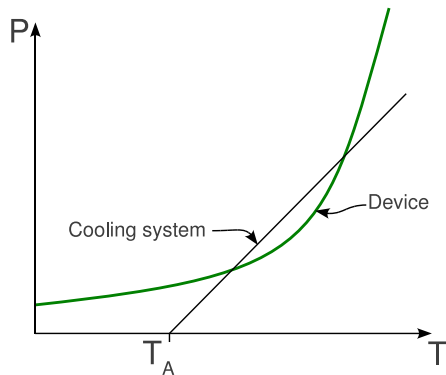


# Thermal Run-away mechanism – Principle



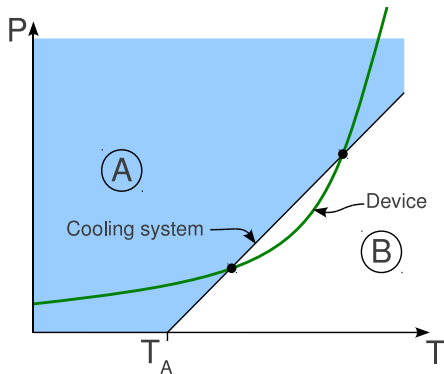
- ▶ The device characteristic
- ▶ Its associated cooling system
- ▶ In region A, the device dissipates more than the cooling system can extract
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- ▶ Two equilibrium points: one stable and one unstable
- ▶ Above the unstable point, run-away occurs

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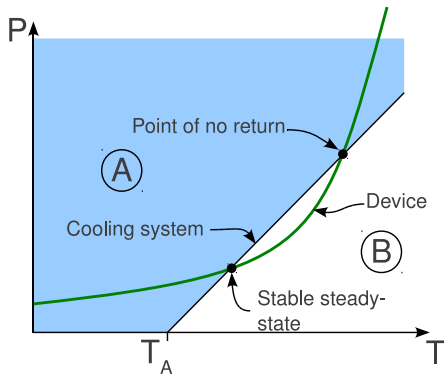
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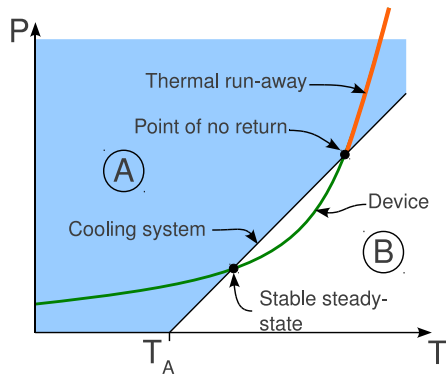
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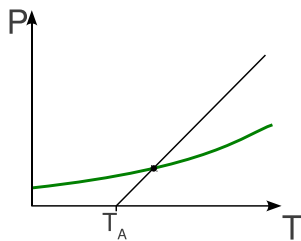


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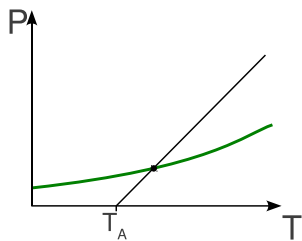
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# Thermal Run-away mechanism – examples

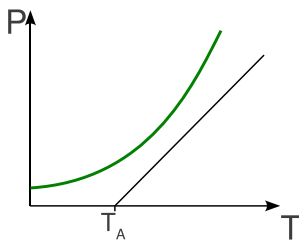


Always stable

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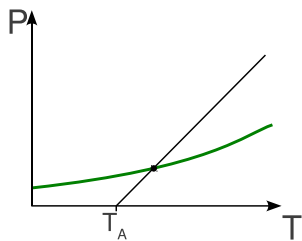


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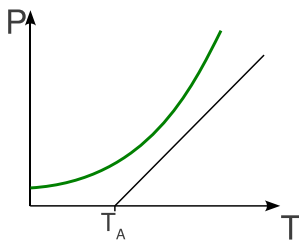


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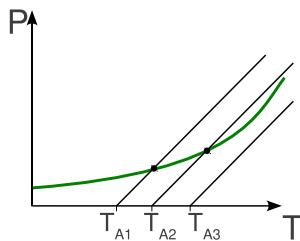
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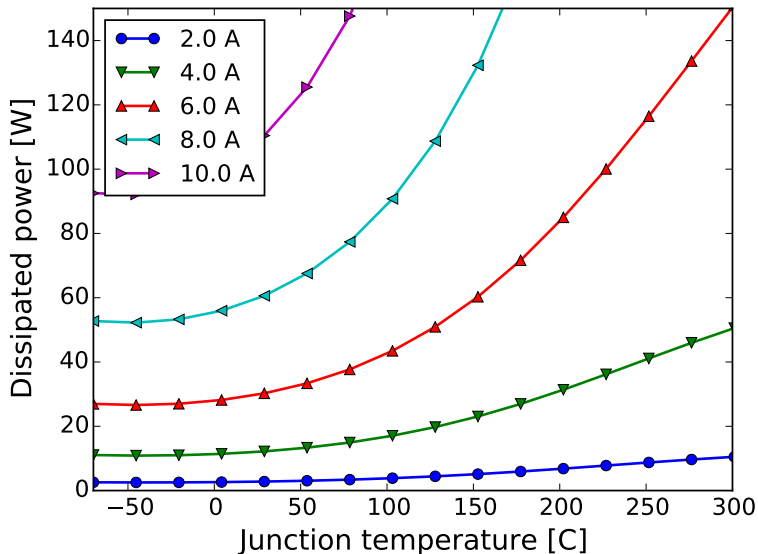


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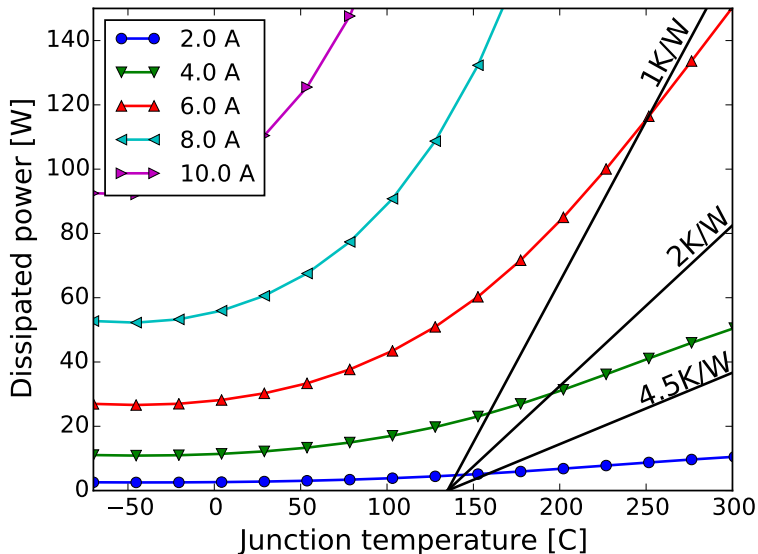


Becoming unstable  
with ambient  
temperature rise

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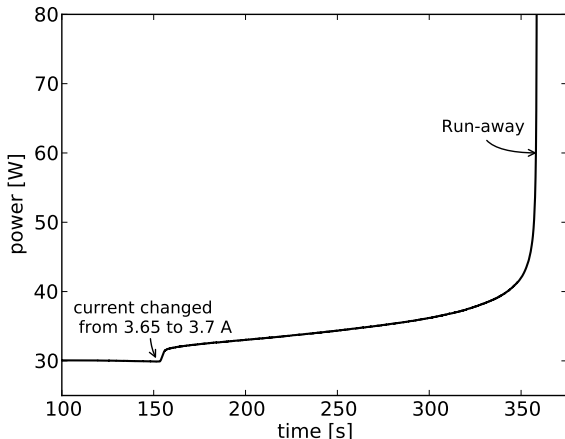


# Power dissipation as a function of the junction temp.



# High Temperature Thermal Management

Buttay et al. "Thermal Stability of Silicon Carbide Power JFETs", IEEE Trans on Electron Devices, 2014



## SiC JFET:

- ▶ 490 m $\Omega$ , 1200 V
- ▶  $R_{ThJA} = 4.5 K/W$
- ▶ 135 °C ambient
- ▶ On-state losses

High temperature capability  $\neq$  reduced cooling needs!

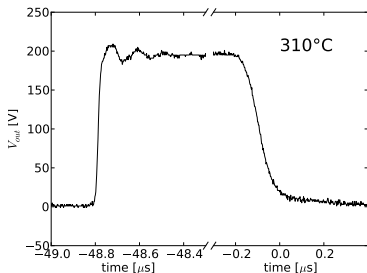
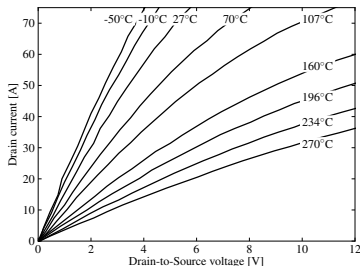
**SiC JFETs must be attached to a low- $R_{Th}$  cooling system.**



# Conclusions on high-temp. behaviour of SiC JFETs

- ▶ SiC JFETs can operate at  $> 200\text{ }^{\circ}\text{C}$
- ▶  $R_{DS(on)}$  dependent on temperature
- sensitive to thermal run-away
- ▶ Require efficient thermal management
  - ✦ low thermal resistance (1-2 K/W)
  - ✦ low or high ambient temperature ( $> 200\text{ }^{\circ}\text{C}$  possible)

Falahi et Al. "High temperature, Smart Power Module for aircraft actuators", HITEN 2013

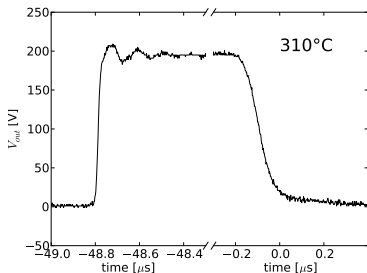
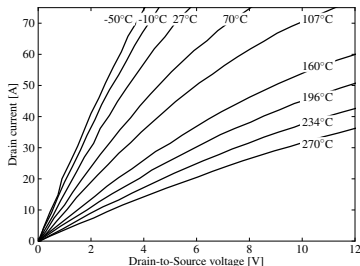




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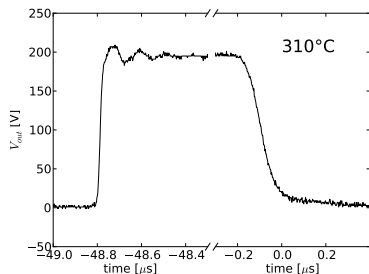
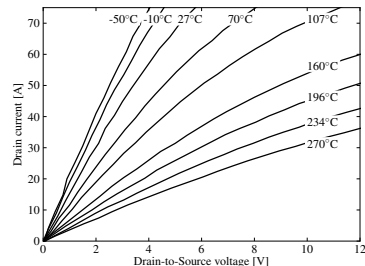
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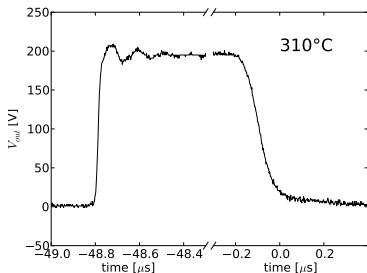
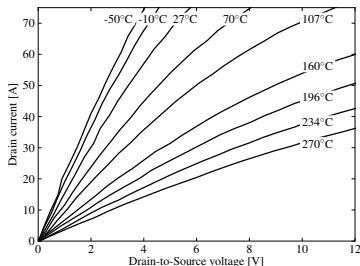
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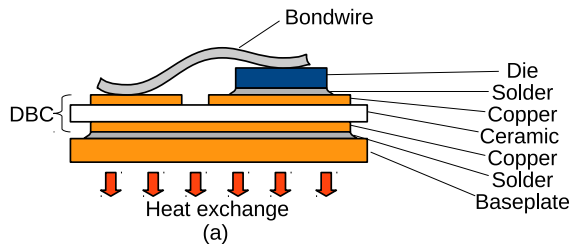
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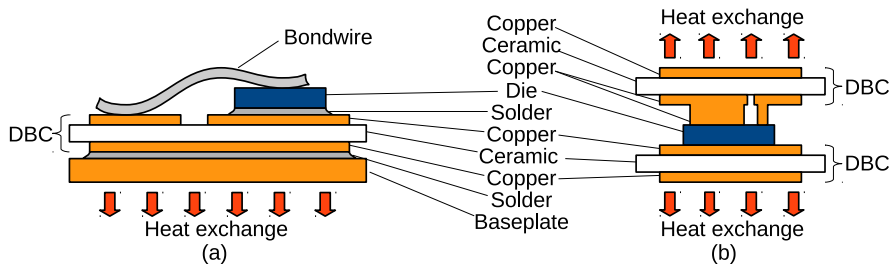
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# Double Side Cooling



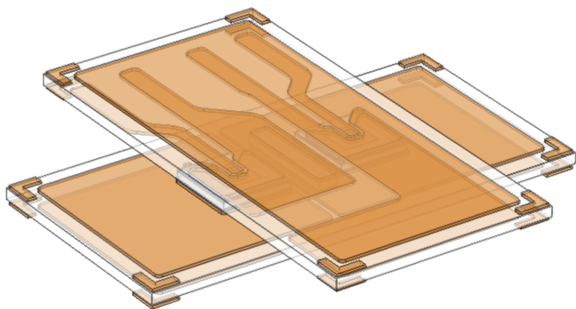
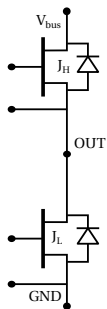
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- ▶ “3-D” or “Sandwich” package offers thermal management on both sides
- ▶ Requires suitable topside metal on the die
- ▶ Requires special features for topside contact

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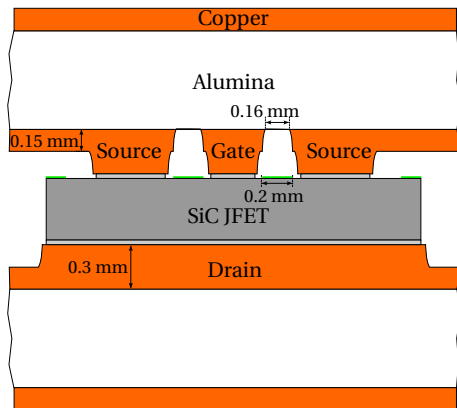
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# The proposed 3-D Structure



- ▶ Two ceramic substrates, in “sandwich” configuration
- ▶ Two SiC JFET dies (SiCED)
- ▶ assembled using silver sintering
- ▶ 25.4 mm×12.7 mm (1 in×0.5 in)

# Ceramic Substrates

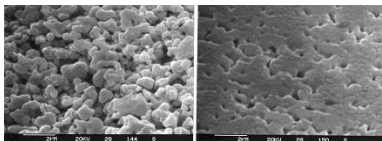


Scale drawing for  $2.4 \times 2.4 \text{ mm}^2$  die

- ▶  $\text{Si}_3\text{N}_4$  identified previously for high temperature
- ▶ For development: use of alumina
- ▶ Etching accuracy exceeds standard design rules
- ▶ Double-step copper etching for die contact
- ➔ Custom etching technique



# Bonding Material: Silver Sintering



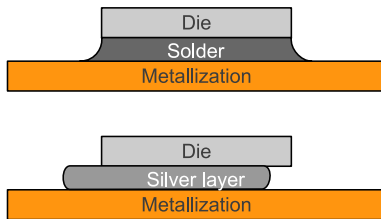
Göbl, C. et al "Low temperature sinter technology Die attachment for automotive power electronic applications" proc of APE, 2006

## Silver Paste

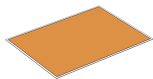
- ▶ Based on micro-scale silver particles (Heraeus LTS-11702P2)
- ▶ Low temperature (240 °C) sintering
- ▶ Low pressure (2 MPa) process

## No liquid phase involved:

- ▶ No movement of the die
- ▶ No bridging across terminals
- ▶ No height compensation thanks to wetting



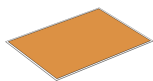
# Preparation of the Substrates



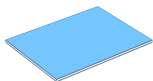
plain DBC board

- ▶ Final patterns within  $50\ \mu\text{m}$  of desired size
- ▶ Two designs, for  $2.4 \times 2.4\ \text{mm}^2$  and  $4 \times 4\ \text{mm}^2$  dies
- ▶ Total copper thickness  $300\ \mu\text{m}$ ,  $\approx 150\ \mu\text{m}$  per step

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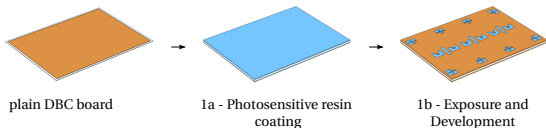
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1a - Photosensitive resin coating

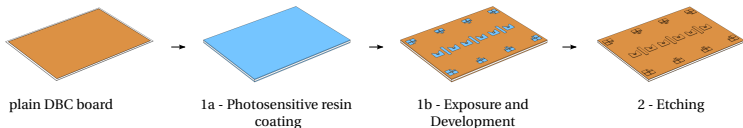
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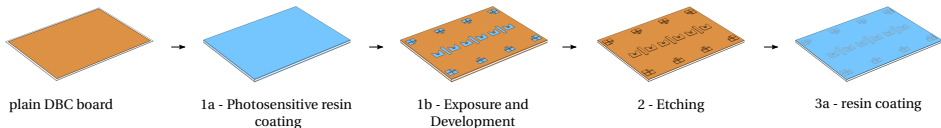
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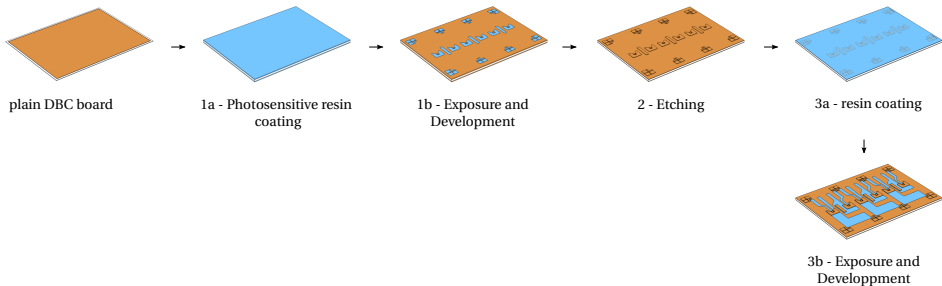
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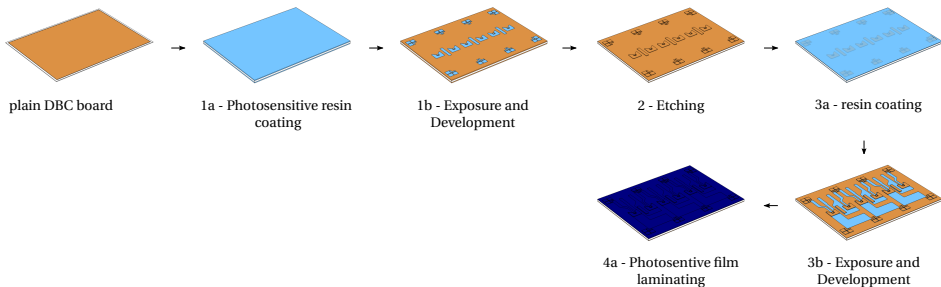
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- ▶ Final patterns within  $50\ \mu\text{m}$  of desired size
- ▶ Two designs, for  $2.4 \times 2.4\ \text{mm}^2$  and  $4 \times 4\ \text{mm}^2$  dies
- ▶ Total copper thickness  $300\ \mu\text{m}$ ,  $\approx 150\ \mu\text{m}$  per step

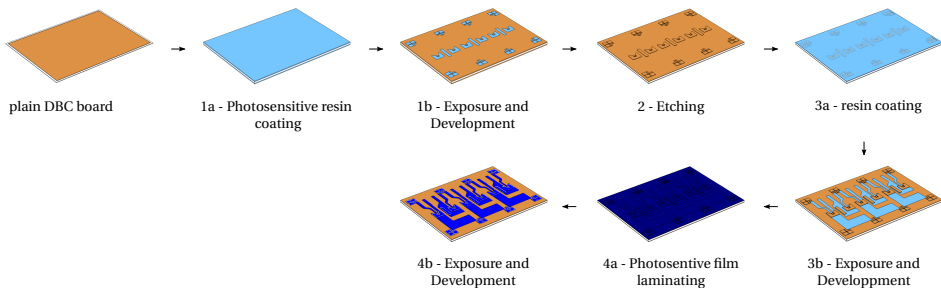
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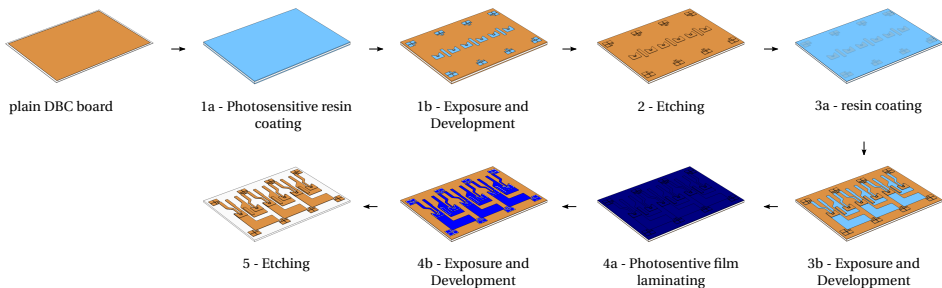


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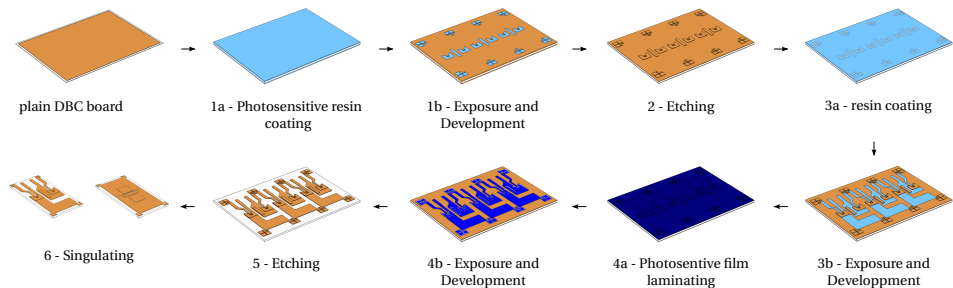
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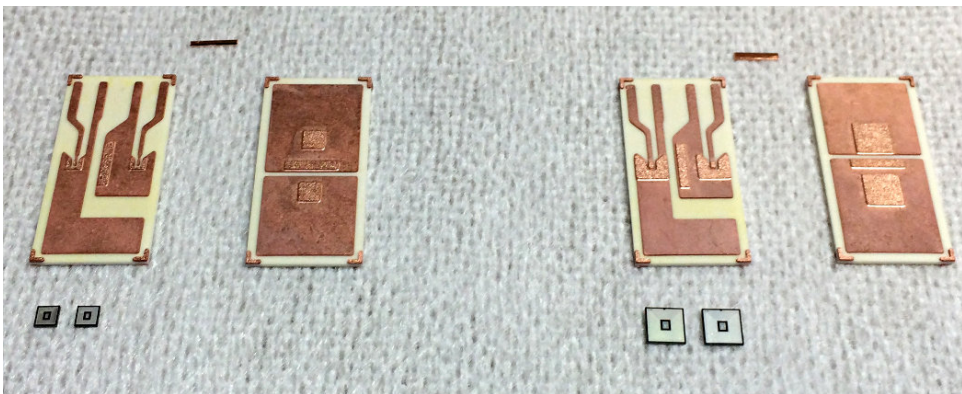
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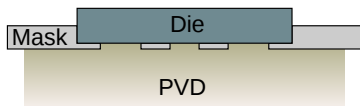
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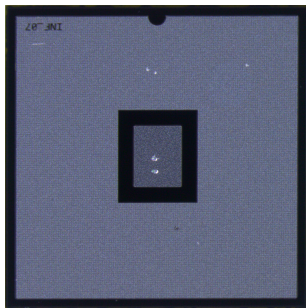
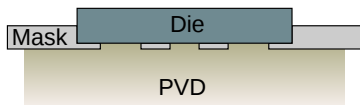
# Preparation of the Dies

- ▶ Standard aluminium topside finish not compatible with silver sintering
- ▶ Ti/Ag PVD on contact areas
- ▶ Need for a masking solution
- jig with locating pockets.



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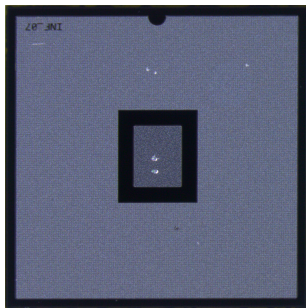
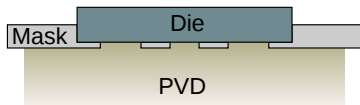
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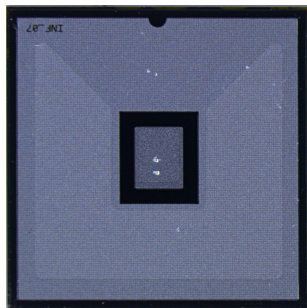
Before PVD

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Before PVD



After Ti/Ag PVD



## Screen printing

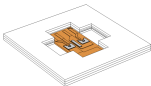
- ▶ Ceramic laser-cut jigs for precise alignment of dies and substrate
- ▶ Two sintering steps using the same temperature profile



# Assembly



Screen printing



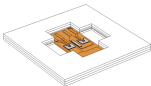
2- Mounting in alignment jig

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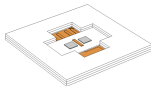
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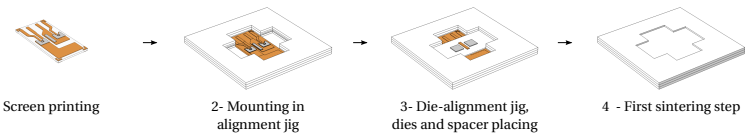
2- Mounting in alignment jig



3- Die-alignment jig, dies and spacer placing

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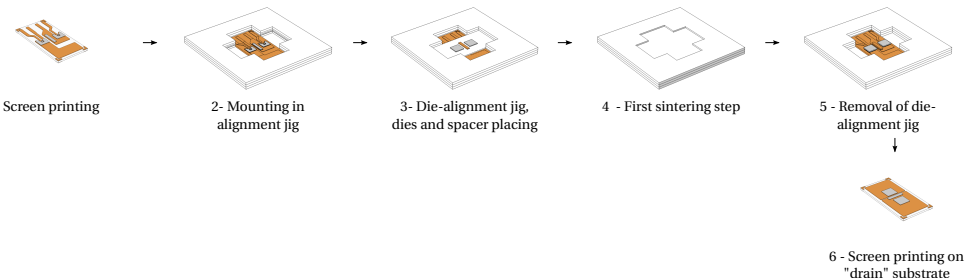
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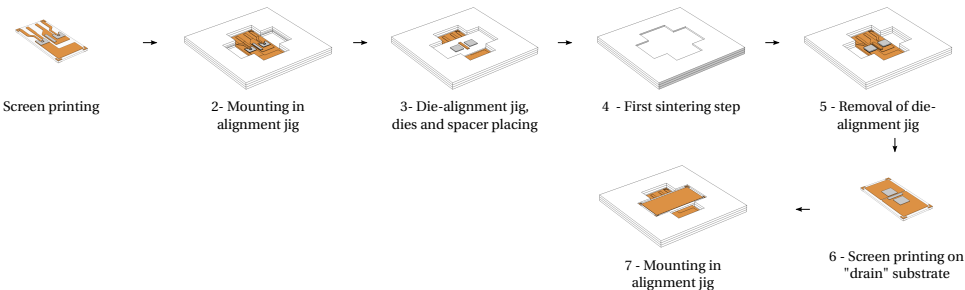
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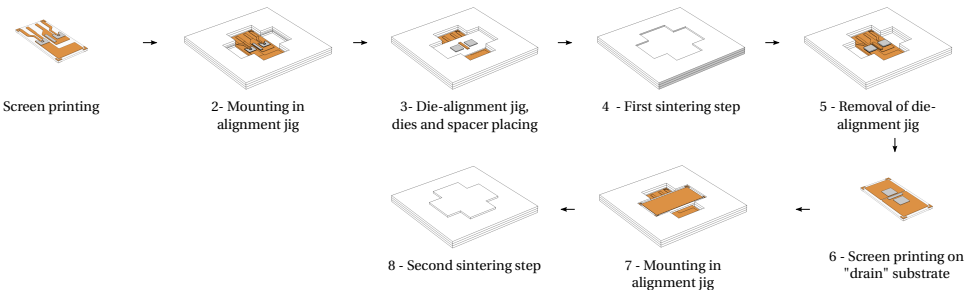
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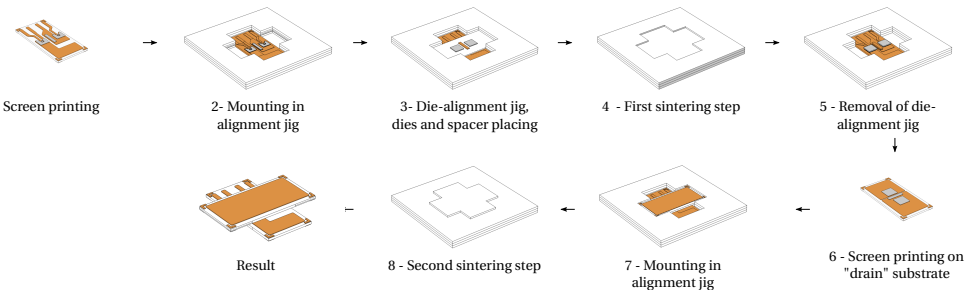
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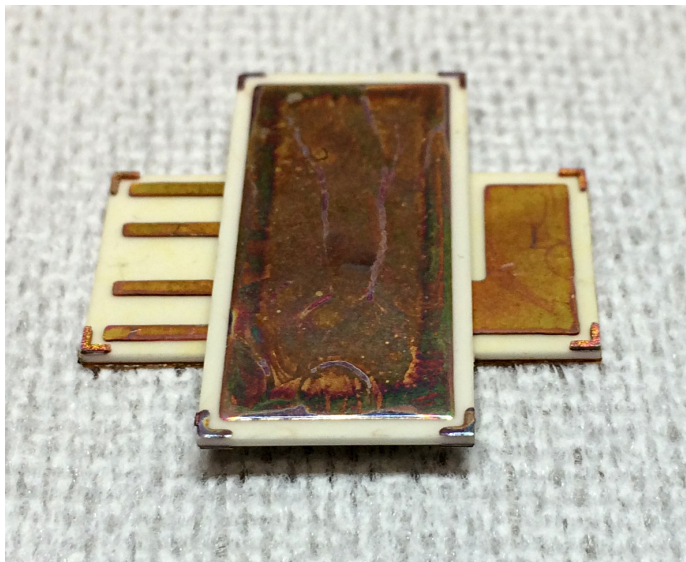
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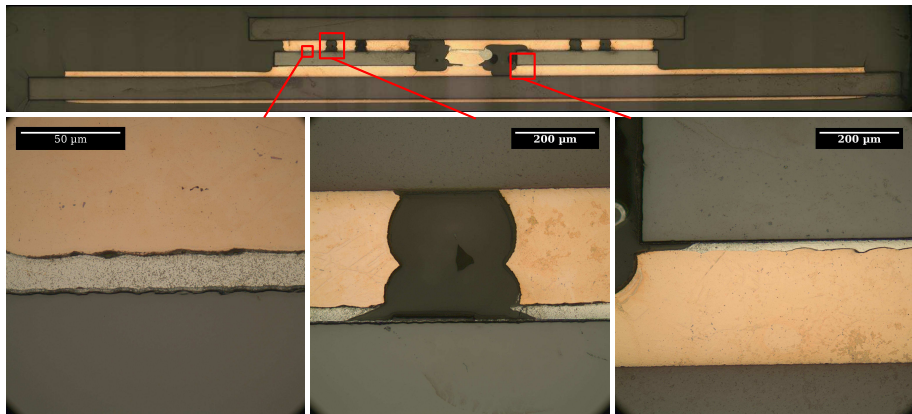


## Some results

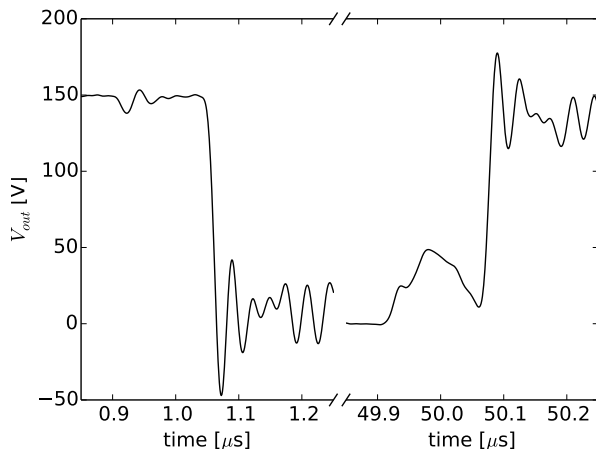


Size:  $25 \times 25 \text{ mm}^2$

# Some results



# Some results



- ▶ 300  $\Omega$  Resistive load, 0.5 A current (no cooling system used)
- ▶ oscillations due to external layout

Introduction

High-Temperature behaviour of SiC Devices

Packaging for high-temperature converters

**Conclusion**

# Conclusion

- ▶ SiC JFET able to operate continuously at high temperature ( $> 200\text{ }^{\circ}\text{C}$ )
- ▶ Must be provided with efficient thermal management ( $R_{Th} = 1\text{--}2\text{ K/W}$ )
- ▶ Proposition: introduce dual-side cooling
- ▶ 3D structure using only high-temperature-rated materials
  - ▶ Should be able to operate continuously at  $300\text{ }^{\circ}\text{C}$ , including passivation (pylyene HT or F)
  - ▶ Proposed etching technique offers satisfying resolution
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This work was funded by Euripides-Catrenes under the grant name “THOR” and FRAE under the grant name “ETHAER”.

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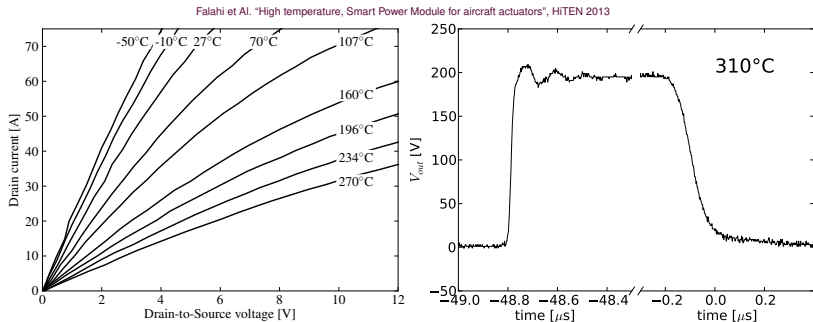
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UNIVERSITÉ  DE LYON

[cyril.buttay@insa-lyon.fr](mailto:cyril.buttay@insa-lyon.fr)

- ▶ picture of the Airbus A350: [airbus](#)
- ▶ picture of the thrust reverser: Hispano-Suiza  
<http://www.hispano-suiza-sa.com/spip.php?rubrique48>
- ▶ picture of the Toyota Prius: Picture by Pawel Golsztajn, CC-SA, available on Wikimedia Commons [http://commons.wikimedia.org/wiki/File:Toyota\\_Prius.2.JPG](http://commons.wikimedia.org/wiki/File:Toyota_Prius.2.JPG)
- ▶ downhole gas compressor: <http://www.corac.co.uk/products/downhole-gas-compressor>
- ▶ picture of Jupiter: NASA  
[http://en.wikipedia.org/wiki/File:PIA04866\\_modest.jpg](http://en.wikipedia.org/wiki/File:PIA04866_modest.jpg)
- ▶ MOSFET wafers from Mitsubishi  
<http://compoundsemiconductor.net/cws/article/fab/38238/1/siliconcarbide-wafers>

# Static and Dynamic Characterization of 60 m $\Omega$ JFET



Previous results show that SiC JFETs are attractive for  
> 200 °C operation:

- ▶ rated at 1200 V (or more), several Amps
- ▶ Voltage-controlled devices
- ▶ No reliability issue related to gate oxide degradation

# Properties of some semiconductors

	"Classical"		wide-bandgap				
	Si	GaAs	3C-SiC	6H-SiC	4H-SiC	GaN	Diamond
Bandgap Energy $E_g$ (eV)	1,12	1,4	2,3	2,9	3,2	3,39	5,6
Elec. mobility $\mu_n$ (cm <sup>2</sup> .V <sup>-1</sup> .s <sup>-1</sup> )	1450	8500	1000	415	950	2000	4000
Hole mobility $\mu_p$ (cm <sup>2</sup> .V <sup>-1</sup> .s <sup>-1</sup> )	450	400	45	90	115	350	3800
Critical elec. field $E_C$ (V.cm <sup>-1</sup> )	$3.10^5$	$4.10^5$	$2.10^6$	$2,5.10^6$	$3.10^6$	$5.10^6$	$10^7$
Saturation velocity $v_{sat}$ (cm.s <sup>-1</sup> )	$10^7$	$2.10^7$	$2,5.10^7$	$2.10^7$	$2.10^7$	$2.10^7$	$3.10^7$
Thermal cond. $\lambda$ (W.cm <sup>-1</sup> .K <sup>-1</sup> )	1,3	0,54	5	5	5	1,3	20