

Improving the thermal management of power GaN devices

ATW on Thermal Management, Los Gatos

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Introduction

Thermal Management Strategies

Experimental Characterization

Conclusions

Introduction

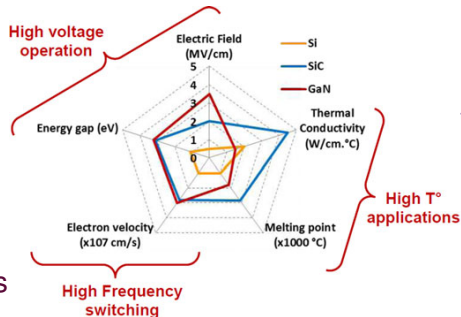
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GaN Devices for Power Management

- ▶ Low on-state specific resistance (100 times lower than Si)
- ▶ Fast-switching device
- ▶ Low cost (GaN-on-Si substrate) [5]
 - ▶ GaN on SiC: 20 \$/cm²
 - ▶ GaN on Sapphire: 5 \$/cm²
 - ▶ GaN on Si: 0.5 \$/cm²
- ▶ Lateral devices (no GaN substrates available)
 - Specific thermal management



P. Roussel, "SiC market and industry update," presented at the Int. SiC Power Electron. Appl. Workshop, Kista, Sweden, 2011.

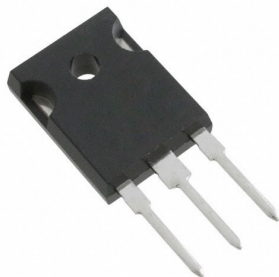
Overview of Available GaN Devices – 1

Source: Transphorm TPH3205WS datasheet

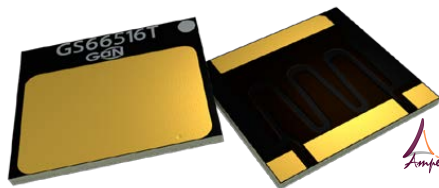
Manufacturers:

- ▶ Panasonic (600 V, 71 m Ω)
enhancement mode
- ▶ GaN Systems (650 V, 27 m Ω)
enhancement mode
- ▶ Transphorm (600 V, 52 m Ω)
Cascode with HeMT
- ▶ EPC (30 V, 4 m Ω)
enhancement mode

Packaging options from standard to highly specific

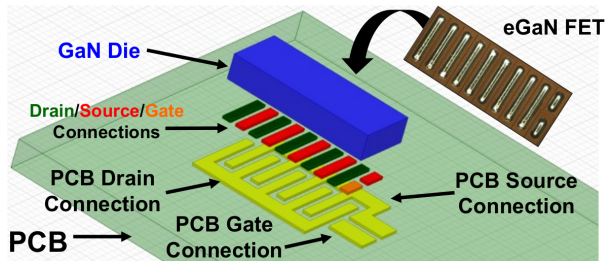


Source: GaNSystems GS66516T datasheet



Overview of Available GaN Devices – 2

- ▶ EPC 2015 GaN transistor chosen for this study
 - ▶ 30 V, 33 A, 4 m Ω
 - ▶ 4x1.6 mm², die 685 μ m thick
- ▶ Wafer-level packaging
 - ▶ Land Grid Array (solder bumps on die)
 - ▶ simple configuration for modelling, processing. . .
- ▶ Mounting technique: flip-chip on board, cooling via the bumps.



Lidow, A. et al. "A New Generation of Power Semiconductor Packaging Paves the Way for Higher Efficiency Power Conversion" (IWIPP 2015) [3]

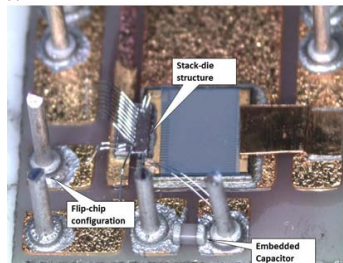
Packaging Requirements for GaN Devices – 1

- ▶ Most devices are very sensitive to overvoltage, no avalanche allowed
 - ▶ EPC eGaN transistors:
 - recommended gate voltage 5 V, absolute maximum: 6 V
- ▶ Switching frequency: 100s to 1000s of kHz
 - ▶ Stray inductances of power circuit will cause large losses
- ▶ Small package size
 - ▶ High power density, need to provide good thermal management.

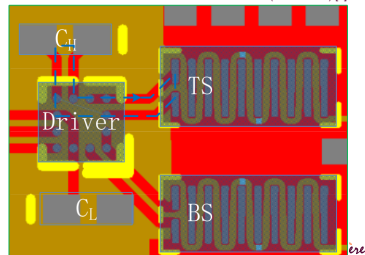
Packaging Requirements for GaN Devices – 2

- ▶ Very low layout inductance (ideally < 1 nH)
- ▶ Driver and capacitors as close as possible to power devices
 - ▶ Use of multi-layer PCB
 - ▶ Short interconnexions
 - ▶ Die stacking

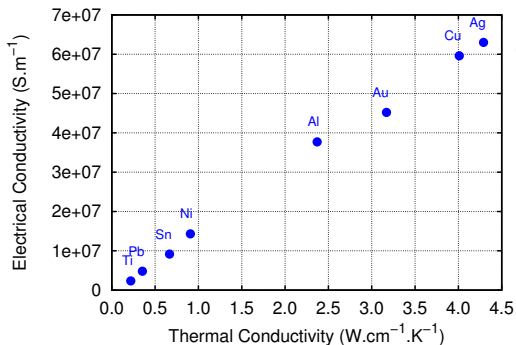
Source: Lee, F. C. et al "A New Package of High-Voltage Cascode Gallium Nitride Device for High-Frequency Applications" (IWIPP 2015) [2]



Kangping, W. et al. "An Optimized Layout with Low Parasitic Inductances for GaN HEMTs Based DC-DC Converter" (APEC 2015) [1]



Substrates for Power Electronics – 1



Thermal conductivity

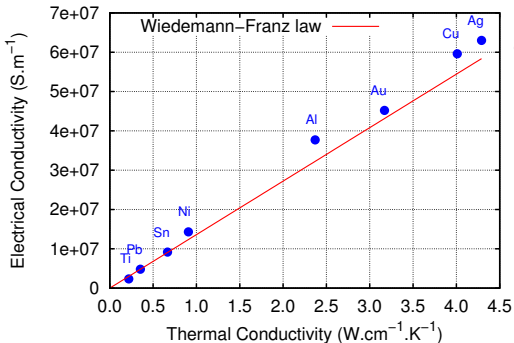
$$\lambda = \lambda_e + \lambda_p$$

▶ λ_e : charge carriers
(electrons)

$$\lambda_e = LT\sigma$$

▶ λ_p : phonons (vibrations of
the atomic lattice)

Substrates for Power Electronics – 1



Thermal conductivity

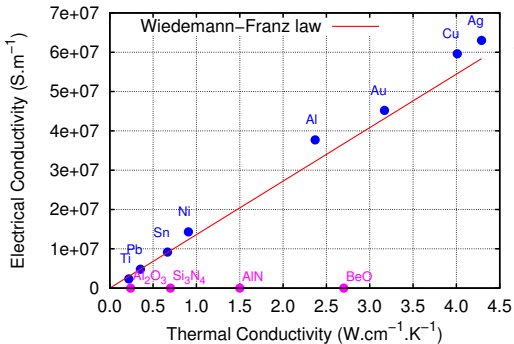
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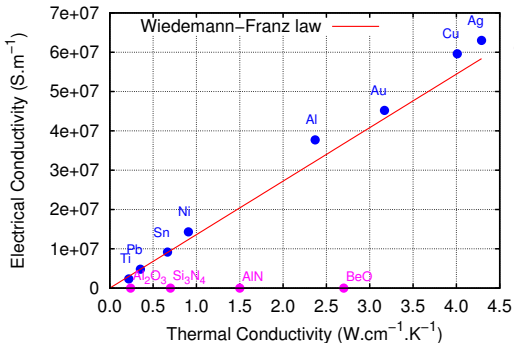
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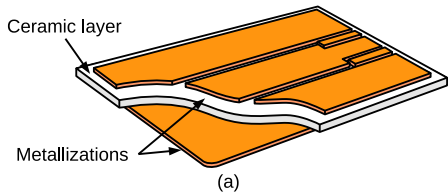
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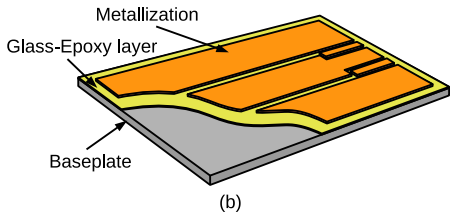
- ▶ λ_p : phonons (vibrations of the atomic lattice)

→ Few materials are both Thermal conductors and electrical insulators (diamond, AlN, Si₃N₄, Al₂O₃).

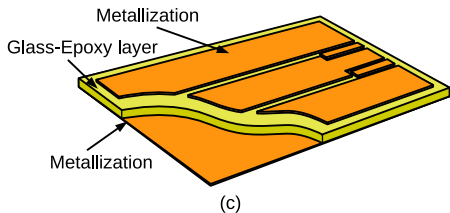
Substrates for Power Electronics – 2



- ▶ **(a) DBC:** ceramic dielectric (Al_2O_3 , AlN , Si_3N_4)
 - ▶ high thermal conductivity (20-180 W/K.m)
 - ▶ expensive



- ▶ **(b) IMS:** organic dielectric clad on thick metal
 - ▶ low thermal conductivity ($\approx 1-2$ W/K.m [4])
 - ▶ thin dielectric layer
 - medium thermal resistance
 - ▶ low cost



- ▶ **(c) PCB:** organic dielectric
 - ▶ low thermal conductivity
 - ▶ multi-layer possible
 - ▶ low cost

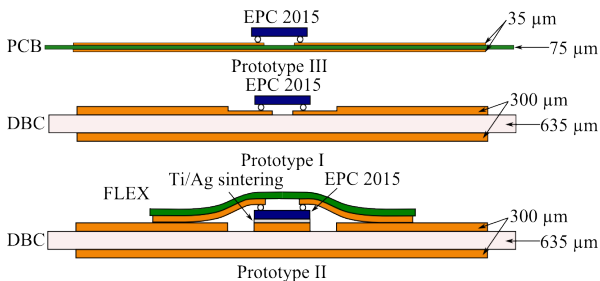
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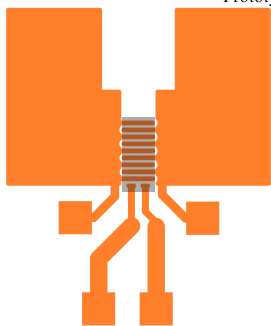
Overview of Prototypes



GaN device on thin PCB

GaN device on DBC

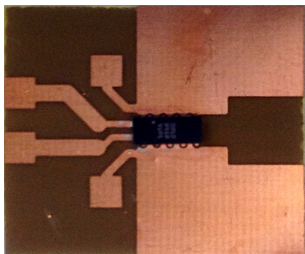
“flip-flip” GaN device DBC



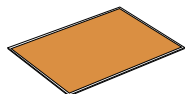
- ▶ 4-point resistance measurement
 - ▶ $R_{DS(on)}$ used as a temperature measurement
 - ▶ GaN transistors have very low $R_{DS(on)}$ (4 m Ω)
- ▶ Interleaved pattern for LGA package
 - ▶ 400 μm pitch (200 μm features)

Manufacturing of the PCB prototype

- ▶ Ultra-thin PCB
(70 μm resin, 35 μm copper)
- ▶ Cleaning
- ▶ Mounting of GaN transistors using BGA repair equipment (Zevac Onyx 21)
 - ▶ flip-chip alignment feature
 - ▶ reflow of SAC bumps (217 $^{\circ}\text{C}$)
 - ▶ no additional solder (only tacky flux)

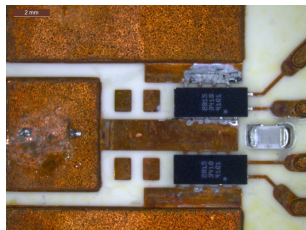


Manufacturing of the DBC prototype

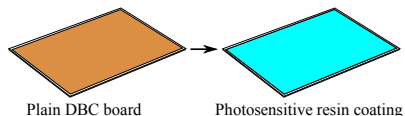


Plain DBC board

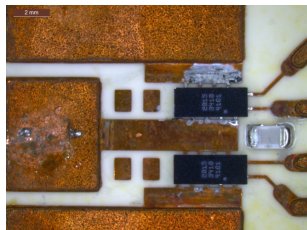
- ▶ Two-step etching:
 - ▶ thinning of copper in high-resolution areas ($300\ \mu\text{m}$ down to $50\ \mu\text{m}$)
 - ▶ patterning of remaining copper
- ▶ Mounting using Zevac ONYX 21



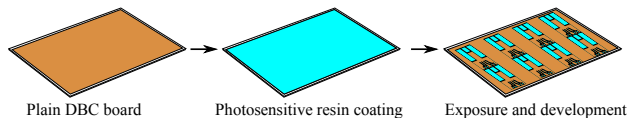
Manufacturing of the DBC prototype



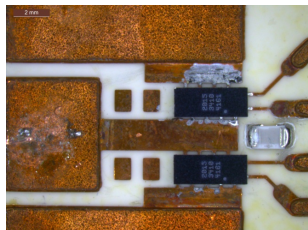
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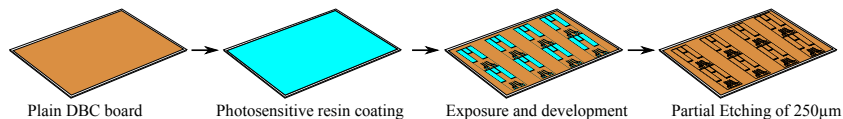
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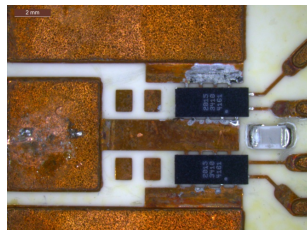
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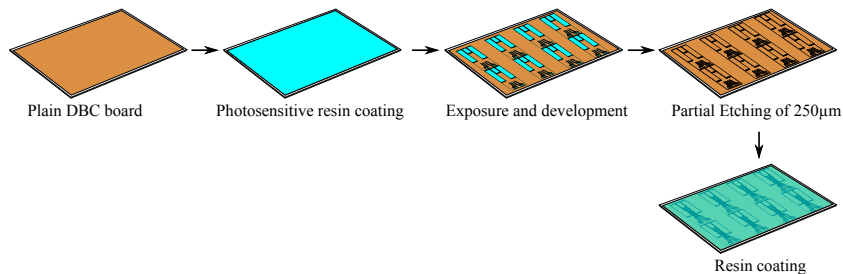
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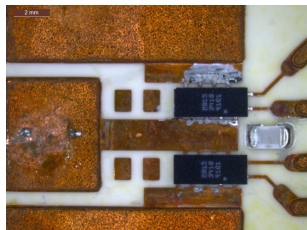
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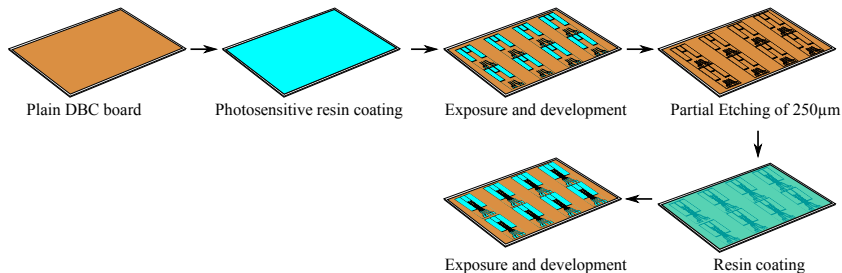
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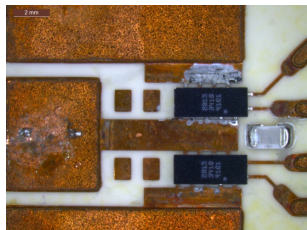
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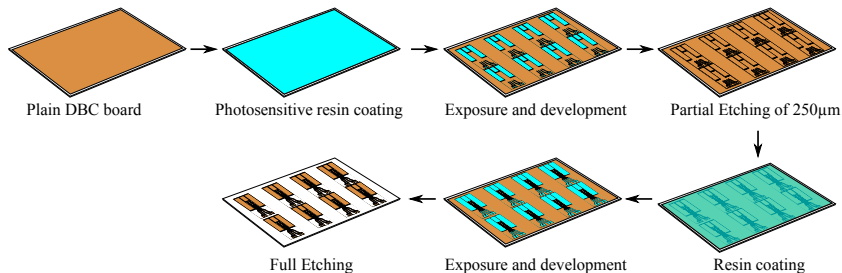
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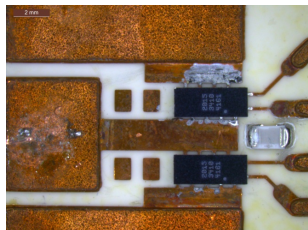
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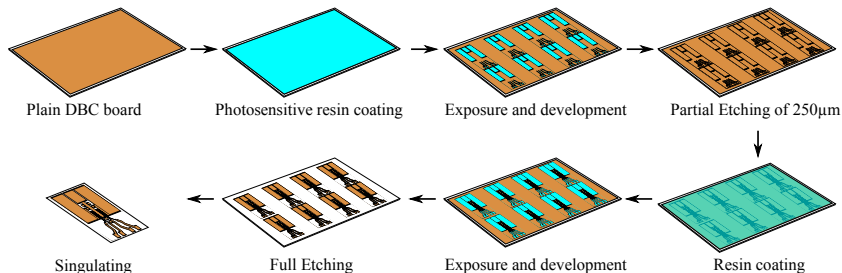
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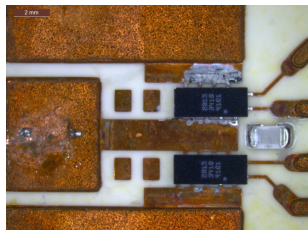
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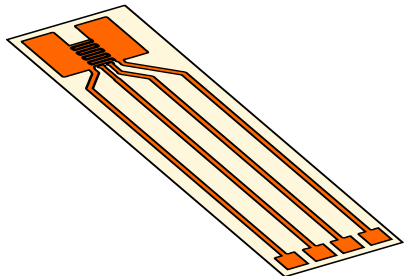
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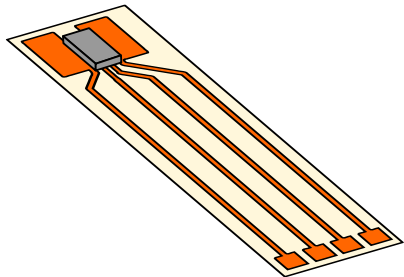


Manufacturing of the “Flip-Flip” Prototype – 1



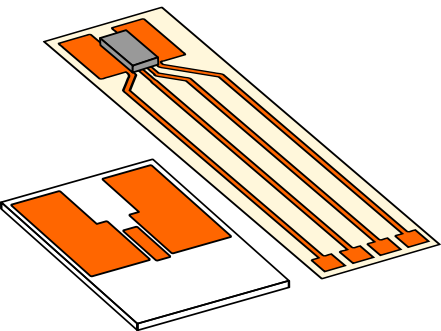
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- ▶ Mounting of GaN transistor
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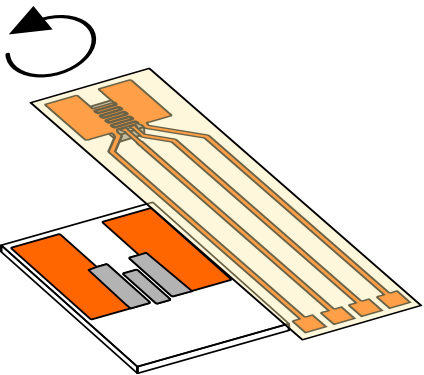
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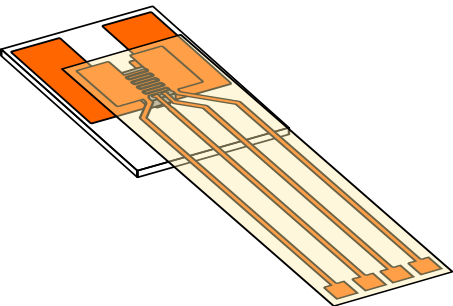
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Manufacturing of The “Flip-Flip” Prototype – 2

Preparation of dies:

- ▶ Grinding of silicon substrate
 - ▶ use of mounting wax
 - ▶ grinding with P1200 grit paper
- ▶ $\approx 600 \mu\text{m}$ substrate ground down to $200\text{-}400 \mu\text{m}$
- ▶ PVD plating (50 nm Ti, 150 nm Ag)
- ▶ Mounting on flex substrate
- ▶ Sintering
 - ▶ Nano-Tach-X (NBE tech)
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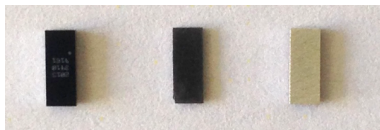
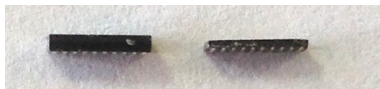
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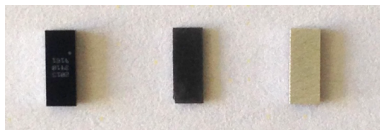
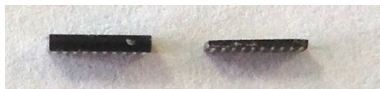
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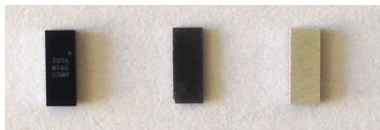
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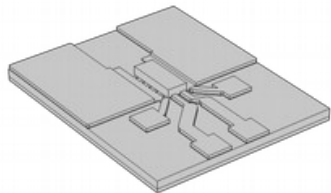
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Simulation – Conditions



	Thermal Cond. $W/K \cdot m$
Copper	400
Alumina	27
Solder bumps	62
Silicon substrate	130
PCB prepreg	0.4
Sintered silver	200

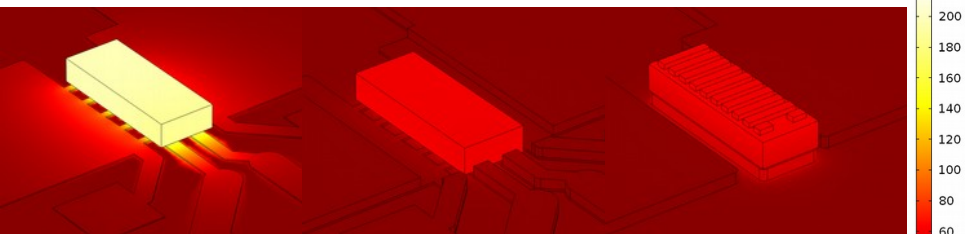
- ▶ FEM simulation using COMSOL
- ▶ External boundaries: convection conditions ($h=8 W/m^2 \cdot K$)
- ▶ backside of substrate:
 - ▶ TIM
 - ▶ Heatsink with natural convection boundary ($T_A = 25 \text{ }^\circ\text{C}$)
- ▶ Surface power dissipation for GaN device: 10 W.

Simulation – Results

PCB

DBC

“Flip-flip”



▶ $T_J=206^{\circ}\text{C}$

▶ $R_{Th}=18\text{ K/W}$

▶ $T_J=76^{\circ}\text{C}$

▶ $R_{Th}=4.9\text{ K/W}$

▶ $T_J=75^{\circ}\text{C}$

▶ $R_{Th}=4.8\text{ K/W}$

▶ Dissipated power: 10 W

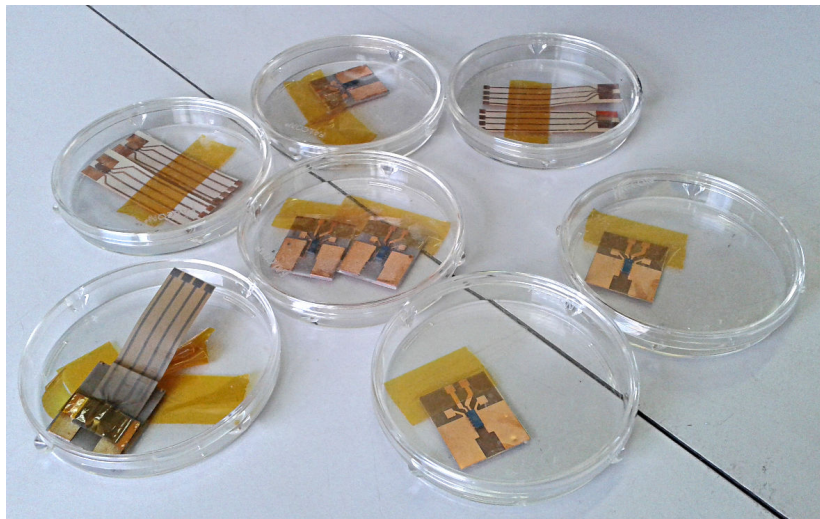
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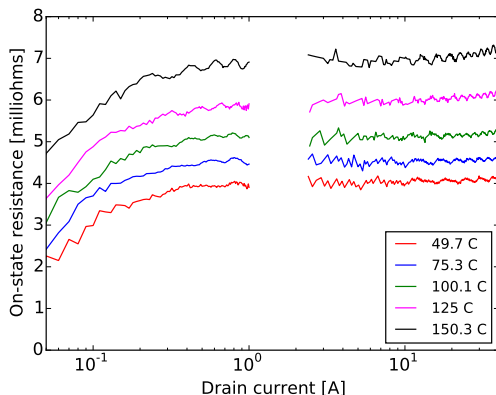
Photograph of the Prototypes



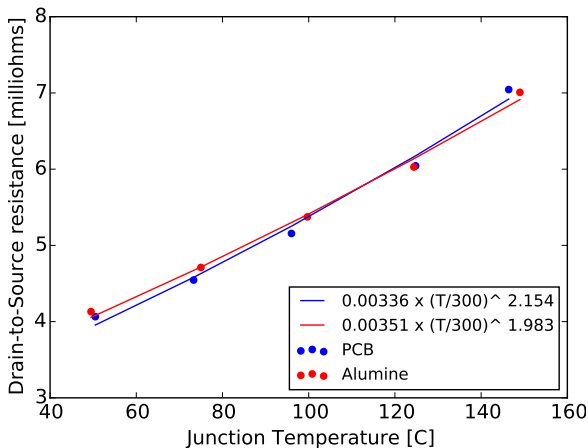
Experimental Characterization – Calibration

Use of R_{DSon} as a temperature sensitive parameter

- ▶ Allow for temperature estimation during operation
- ▶ Good sensitivity to temperature
- ▶ R_{DSon} is low
- ▶ non-linearities at low drain current



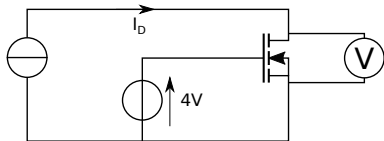
Experimental Characterization – Identification



- ▶ Calibration curve useable from 1 to 40 A drain current
- ▶ Voltage-drop to monitor of 50–300 mV

Experimental Characterization – Measurement of R_{Th}

- ▶ Test vehicle attached to a large heatsink with TIM
- ▶ Device continuously on
- ▶ Monitoring of V_{DS} for 20 min
- ▶ Estimation of temperature from $R_{DS(on)}$ variation
- ▶ “Flip flip” prototype not fonctionnal
- ▶ Ambient: 26 °C



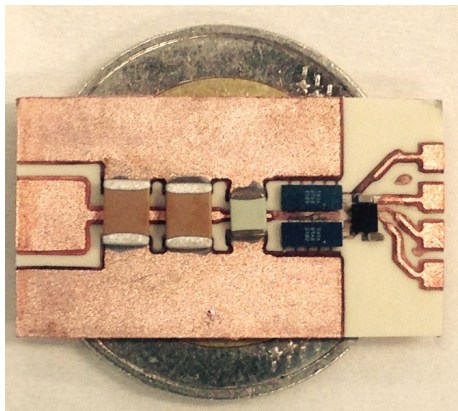
	$I_D = 20 \text{ A}$	$I_D = 30 \text{ A}$	$I_D = 40 \text{ A}$
PCB	85 °C	Run-away	
DBC	36 °C	49 °C	73 °C

Measurement Results

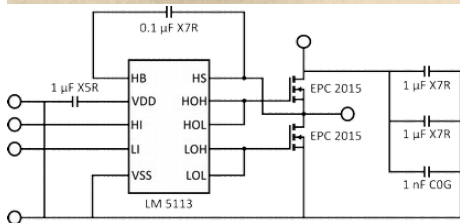
	I_D (A)	Power (W)	T_J (°C)	R_{Th}	
				Experimental	Simulation
PCB	25	3.9	125	25 K/W	18 K/W
DBC	40	7.46	73	6.2 K/W	4.9 K/W

- ▶ High experimental R_{Th} for PCB might be due to bending
- ▶ Clear improvement of ceramic substrate over PCB

Integrated Half-Bridge on DBC



- ▶ Layout: design reference from TI
- ▶ Substrate: DBC
- ▶ Thinned-down copper on high-res areas:
 - ▶ GaN devices (EPC 2015)
 - ▶ Gate driver (TI 5113)
 - ▶ Capacitors for driver
- ▶ Remaining copper 300 μm thick
 - ▶ On par with 4 m Ω transistors



Introduction

Thermal Management Strategies

Experimental Characterization

Conclusions

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- ▶ Proposed manufacturing technique for high-resolution etching of DBC
- ▶ Electrical-based junction temperature measurement method inaccurate, improvements needed

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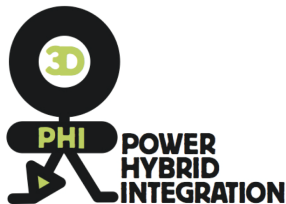
Future Work:

- ▶ Assemble operating “flip-flip” structures
- ▶ Investigate AlN ceramic (expected improvement ≈ 1 K/W in R_{Th})
- ▶ Improve thermal measurements, including Z_{Th} measurement

Thank you for your attention,

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