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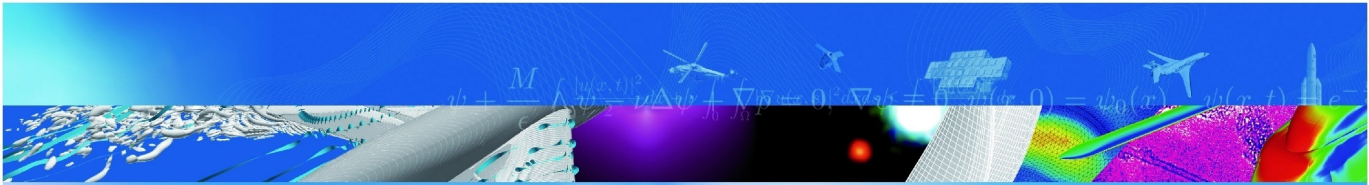
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## ESD AND SECONDARY ARCING POWERED BY THE SOLAR ARRAY -TOWARD FULL ARC-FREE POWER LINES -

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### ABSTRACT

We crossed all the experiments made over 15 years at ONERA during CNES R&D activities; we made hundreds of secondary arcing on Solar Panels or coupons, connectors, SADM1 or simple aged cracked wires. Thanks to the knowledge we have, from ESD<sup>2</sup> or secondary arc triggering, to the analysis of in-flight anomalies; we deduct very simple design rules reducing drastically the probability of secondary arcing.

Let's follow the trail of the power line to find where there would be protection gaps.

### 1. STATE OF ART

From Tempo and Panamsat, Nigast or Adeos 2 and others X, Y or Z Sat, the numbers of power failures that can be attributed to secondary arcing in orbit are commonplace.

All over the world, many studies were performed, some of them together, leading to an ISO Standard in [1] : ISO 11221 in 2011. However, the risk is still present. The main reason is that the mitigation technics were not applied along the full power line of a spacecraft. We all stopped at the front face of a Solar array using blocking diodes limiting

judiciously the current to a single string, which is acceptable, while the size of the cells is not too large or voltage too high (Direct Drive necessary high voltages remains a real problem).

Thinking the problem avoided, we all waited that discharges occurred elsewhere, close to the power line, creating enough conductive plasma path, showing us that where there are two biased power wires separated by vacuum (in the initial design or due to aging effect), but also by dielectric, the danger is still present. Wouldn't there be any solution?

Arcs are possible on the front and rear face of solar panel, on connectors, flex print, SADM<sup>1</sup>, finally all along the power line until the battery.

### 2. THE THREAT

#### Introduction

From ESD, outgassing, increase of pressure, to micrometeorites, which sizes lead to a sufficient impact probability or every other phenomena leading to plasma around biased voltages are able to trig Secondary Arcs Powered by the Solar Array<sup>3</sup> everywhere between the SA<sup>4</sup> and the battery.

The most tenuous plasma is able to create an enough conductive path to allow an arc between two or more power lines. This plasma bubble shall never connect two biased parts. This lead directly to the conclusion that mitigations to apply are made of simple design rules which some of them cost nothing.

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1 Solar Array Driving Mechanism

2 ElectroStatic Discharge

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3 SAPSA

4 Solar Array

*Note: A mitigation concept will be valid only if it is applicable during a full life of the spacecraft, taking into account the global environment, aging effect, temperature and so on.*

### 3. THE RULES

#### NSA<sup>5</sup>, TSA<sup>6</sup>, PSA<sup>7</sup>, Test acceptance

During each discharge, a part of the current in the arc comes from the solar array itself. It is the normal process since a secondary power is available; the electrons from the secondary source follow the lower impedance path through the plasma bubble and participate to create more plasma. If this secondary power source delivers a sufficient energy to maintain this arc alone temporary (TSA) and it becomes very dangerous or permanently (PSA) and it becomes dramatic.

We can easily understand that NSAs only are acceptable because we do not control our set-up enough and the full process of the discharge to authorize any TSA as a successful laboratory test. In addition the variability of wiring configuration of the different section over all the panel is never fully estimated nor tested in laboratory.

*Note: Only NSAs are acceptable as a successful test*

Voltage and current margins to take during test is a difficult question as the results are very sensitive to those parameters.

One should think to take:

- the maximum possible voltage on the SA (section in open circuit if it is a real configuration),
- The real max biasing voltage including possible shadowing or shunted or switching sections during power regulation and possible overshoots.

During laboratory tests, the duration of the (primary) ESD on small samples was perfectly quantified (some tens of  $\mu\text{s}$ ). Now, we all agreed on the fact that a large panel flashover simulator has to be included during the test.

<sup>5</sup> Non Sustain Arc: Secondary Arc lasts only the time of the primary ESD

<sup>6</sup> Temporary Sustain Arc: Secondary Arc lasts alone over the time of the primary ESD

<sup>7</sup> Permanent Sustain Arc: Secondary Arc lasts alone permanently

ESD (including flashover) lasts some hundreds  $\mu\text{s}$ . It reinforced the fact that if secondary power is sufficient it will lead more easily to a PSA and the frontier between TSA and PSA become tenuous.

#### Guidelines: what is written (in Europe)?

Unfortunately, nothing is specified except on the front face of the SA<sup>8</sup>

#### *In ECSS E-ST-20-08 [1]*

##### 5.5.1.5 Electrostatic discharge (ESD) test

###### 5.5.1.5.1 Purpose

The purpose of the ESD test is to demonstrate that the use of adequate design rules reduces the risk of ESD. This is done by demonstrating that ESD primary discharge does not lead to a self-sustained secondary arc, which can lead to loss of permanent power or insulation in the solar array.

The tests are performed on solar array coupons using instrumentation specially designed for that purpose. Typical rules and a test procedure are described in ECSS-E-ST-20-06.

###### 5.5.1.5.2 Pass-fail criteria

- No sustained arc shall occur.
- Testing shall demonstrate that the observed primary arcs do not produce any type of damage to the solar array or to the cells.

#### *In ECSS E20-06c [2]*

Power the solar cell string with an ESD representative Solar Array Simulator at nominal interesting voltage and nominal string current, including margin and the switching transients (overshoot) due to the operation of the power regulator.

No TSA nor PSA are accepted but the margins assessment, is for now completely left to the primes judgment. We can find a 10% of derating.

Degradation due to cumulative effect of 100 ESD (including a 4m<sup>2</sup> panel flashover) should also be included.

Tests cover the risk both at cells level, panel routing and section level. No related failures related on the front face since the implementation of these rules.

<sup>8</sup> Solar Array

*Note: The tests shall reproduce the real situation encountered in space, taking into account aging effect for example, if needed*

#### 4. SOLAR ARRAYS

##### SA Front face ESD

###### *Situation*

On the front face of a SA, IPG<sup>9</sup> situation is the classic configuration. As long as a global approach of the voltage behaviour of the spacecraft is not taken into account during the spacecraft design phase, we can notice that ESD are very common, even out of storm irradiation conditions.

*Note: The simulation of the good electrostatic behaviour of the spacecraft shall be demonstrated at PDR<sup>10</sup> level*

Thus an electrostatic discharge, more precisely its flashover component is able to propagate toward the full panel 3% of the time and is also able to jump over a 10cm gap (EMAGS 3 Study in [6] or up to 50cm in [5] to reach the next adjacent panel.

Distant ARC, were measured up 38mm between ESD starting point and secondary arcing cell in [7] , So a discharge can start on an interconnector and is able to trig a secondary powered arc in a surrounding gap. On High voltage SA, this distance could increase.

Thus each biased gap between string and sections is concerned.

###### *Solutions options*

Three options are possible; limit the current-voltage capabilities to a secure non-arcing area, separate plasma from biased metallic part thanks insulation (like a specific grouting for example) and/or reduce the arc duration by increasing space between gap (since the arc resistance increase). We will see that the only possible solution is to limit the secondary arcing capability.

- *The grouting*

Insulating two biased electrodes by a dielectric seems to be a very simple and good idea. The

two electrodes will remain insulated and separated as long as the dielectric will stay efficient. An embedded metal doesn't discharge easily and not in the IPG situation. As ionizing irradiation dose modify mechanical properties of dielectrics (generally on silicon glues it is a cross-linking process in [15] which lead after a few years of exposure, to cracks apparition).

Unfortunately many studies demonstrate that when biased electrodes are facing again and are surrounded by the "walls" of cracked dielectric ESD are more frequent and inception voltages occur at lower values (NEDO round robin in [12] or 200 Volts by Wright in [13] in USA or Siguier in [14] in France and more.

*Note : Grouting protect for secondary arcing for satellite mission up to three years. Over it is no more an ESD solution.*

*Note : Testing of grouted panel shall be made with cracks as a minimum or better without grouting (to take into account EOL<sup>11</sup>)*

- *Gap between sections*

This is the missing point to make the front face arc free or arc resistant.

Indeed, it is not possible to warranty a limited potential gradient between two sections, just because one section can be alternatively connected to the bus or shunted for the regulation. Thus except in some specific case, this is the full voltage which has to be taken into account.

And if the specific strings routing on a panel permit low voltage value between adjacent cells (below 40V), the increase of both cell size and voltage will be in a very next future an important problem to solve.

It does make a great difference if you have 1.3A and 30V or the same 1.3A and 130 or 150V. In one case, you can have a classical gap below 1mm but in the other one, a 2mm gap is still not sufficient.

The sections distance gap needed to be safe is above 2cm length. We never find such distances in space but more from 2mm up to 5mm.

<sup>9</sup> Inverted Potential Gradient

<sup>10</sup> Preliminary Design Review

<sup>11</sup> End Of Life

And this point will become more and more critical as the bus voltage will increase.

*Note : Grouting can be apply on normal gap for a short-term mission (<3ans). For Long term mission a larger inter-sections gap coupon has to be tested and qualify.*

- **Limited current-voltage capabilities**

The first limitation, globally accepted, was to use a blocking diode at the top of each string. The objective was to limit the current available for the secondary arc to a single string and no more to a whole section. As the current was reduced down to 0.5A (30 cm<sup>2</sup> GaAs solar Cells), the energy available was sufficiently low to have NSA<sup>12</sup> only. Thus the secondary arc stops when the initial ESD stop. It was tested for 0.5A up to 200 Volts without any problem (CNES-ONERA R&T 2013).

Next generation of cells will have current around 1.2-1.3A (72.44cm<sup>2</sup> SpectroLab or 80cm<sup>2</sup> TAS<sup>13</sup>).

During tests,

- At 1.1A TSA appears from 80V and at 220V we still do not have PSA,
- At 1.5A TSA appears from 50V,
- At 3A 50V are sufficient to trig a PSA.

On High Voltage SA, the todays solutions will remain effective, if the maximum cell to cell voltage remains very low (30-37V seems to be a good idea).

This protection will be more difficult to apply since the string voltage increase up to very high value with an objective compatible with EOR<sup>14</sup> (~350V)

*Note : Maintain the use of blocking diodes. Maintain cell to cell voltage at low value (below 40Volts including shadowing. Grouting does not reduce other constraints for mission above 3 years in orbit.*

#### Other points

- **Wires gluing**

To put a spot of glue on a bus bar certainly improve the durability of the bus bar fixation,

but it also generates a triple point that will allow ESD. As there is not a really safe distance to take from a biased gap, wiring has to be glued directly on polyimide dielectric.

*Note : gluing wires on a busbar should be avoided.*

- **Polyimide-Panel structure conductivity**

Polyimide have, thanks to their good RIC and Photoconductivity, an excellent behaviour under irradiation in space. Unfortunately, carbon fibre is often covered by epoxy glue which tend to limit the leakage current. Then the total conductivity of the assembly is in fact the conductivity of the epoxy glue only.

To insure a better electrostatic behaviour of the spacecraft in space, polyimide shall be "grounded".

## 5. CONNECTORS

### Naked facing Wires

#### RTV 691 or equivalent insulation

Leaving naked tracks inside a connector is not recommended, nor to cover them with silicone glue. Exposed to space radiation, cracks will appear after some years in orbit and ESD and SAPSA also. As there is no current limitation, the full section current will be available, many sections will be soon involved and the full tracks and sections connected to the connector can burn.

*Note: silicone glue is not a good insulator versus time*



Figure [1] Example of flexprint connector

Cracks appear with aging effect leading to ESD.

Leaving a cross section without separation is also dangerous. Each pin shall never face another pin without any dielectric in-between.

<sup>12</sup> Non Sustain Arc: Secondary Arc lasts only the time of the primary ESD

<sup>13</sup> Thales Alenia Space

<sup>14</sup> Electrical Orbit Raising

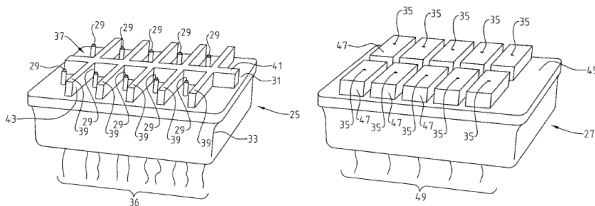


Figure [2] Dielectric Barrier on a connector [16]

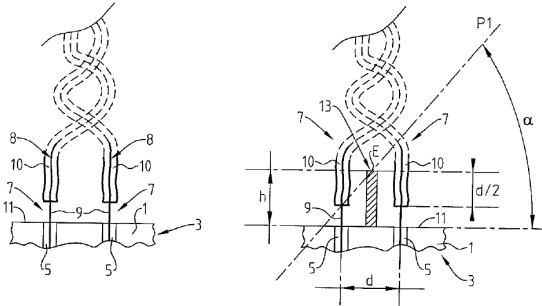


Figure [3] Dielectric barrier between two biased wires [16]

A very simple dielectric barrier with the good height characteristics will prevent from connecting the two wires by the conductive plasma bubble

## 6. FLEXPRINT

Flexprint are usually made of several metallic layers insulated in-between two layers of Polyimide. Thanks to the good behaviour of Polyimide in space (good photoconductivity and good RIC<sup>15</sup>) there is no reason to think that and ESD could generate a SAPSA<sup>16</sup>. A Normal Potential Gradient ESD with a significant punchthrough is improbable or will only create one hole of some tens microns. As there is also no apparent triple point (layers are embedded in Polyimide), an Inverted Potential Gradient seems to be no more probable.

So is a SPASA possible? An arc remains possible if a micrometeorite pierces the Polyimide pierce through and through and creates a plasma and a hole between two biased conductive layers.

To do so, it requests the good angle and a sufficient particle energy, which make this rare, but effective.

Thus, this should have already happened in orbit.

To pierce from 1mm to 2mm we need particles between 500 microns and 1mm, the impact probability is around 0.05 impacts/m<sup>2</sup>/year in GEO and 0.08 impacts/m<sup>2</sup>/year in LEO.

To reduce this probability down to 1E-2 you need particles around 800µm in LEO at 600µm in GEO, and to reach 1E-3, particles from 1mm to 2mm able to pierce a dielectric from 2mm to 3 mm.

*Micrometeorite has to be evocated as a probable arcing failure cause in case of an anomaly analyse.*

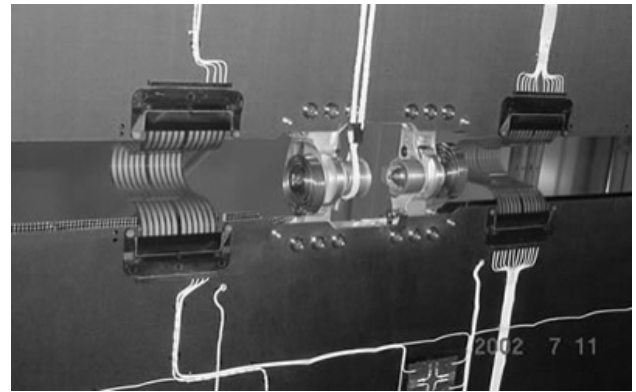


Figure [4] Example of flexprint connector



Figure [5] Example of flexprint connector

All the different copper layers, are generally segregate depending on their voltage, but we can't avoid all the risky configurations. And because of shunt regulation a "plus" wire can be momentarily grounded and be just next to others "plus" wires. In case of arc, All the tracks on the flexprint will arc and probably disconnect their connected sections.

We clearly understand that the problem will be avoid only if the distance between tracks will be large enough. Can we take the risk to lose a

<sup>15</sup> RIC : Radiation Induced Conductivity

<sup>16</sup> SAPSA: Secondary Arcing Powered by the Solar Array

connector (and the power behind) or shall we estimate the minimum distance needed?

*Note: A 5mm distance is recommended as a minimum distance between two flexprint tracks.*

## 7. SADM

A SADM is a volume where all the power of each panel go through. It is mandatory to insure that no discharge is possible inside. The first step is done when the spacecraft venting is no more possible through it. Then there will be no dust deposition.

The second one is made when using dielectric barrier and dielectric brush cover to warranty that two biased metallic parts will never face together. Thus a plasma will not connect sections wires.

*Note: no venting or outgassing through a SADM dielectric barrier are mandatory*

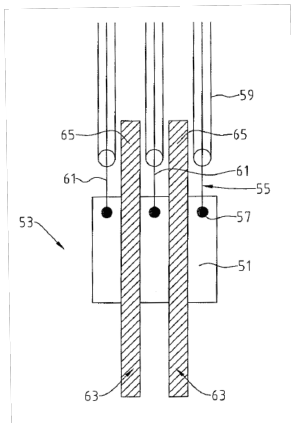


Figure [6] Dielectric Barrier in a SADM [16]

## 8. POWER CONFIGURATION

Blocking diodes or any other system (MOS or others) preventing backflow current from the battery itself is the mandatory condition.

This is the case with a shunt regulation (Telecom satellite for example)

This is not systematically the case when using a Buck regulator

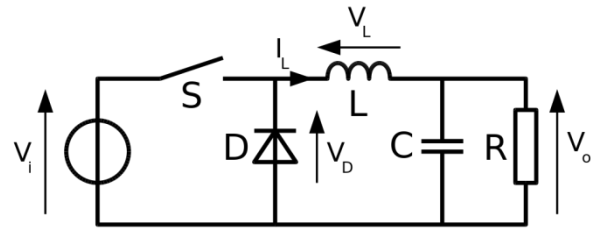


Figure [7] Buck regulation

In ECSS E20 in [3] fortunately the electronic shall be sustain an arc on solar array. It was made for AIT human security and it is also effective to insulate battery power from any temporary ESD

5.2.7 Conditions at start-up/ switch off

5.2.7.5 LCL start-up on SC 1

5.2.7.5.1 Nominal condition

a. The LCL/RLCL shall start up correctly (and within applicable rating/derating limits) when an overload or short circuit is already present at its output.

It works also for Space ESD and SAPSA and insulated SA structure

## 9. CONCLUSION

The manufacturer who will make the choice of a full free-arcing power line will take the advantage. On the other side it is surprising that a satellite which doesn't cover this condition in 2016, is still launched and insured.

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