Design and optimization of IGBT gate drivers for high insulation voltage up to 30kV

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ABSTRACT –In this article, a design methodology to optimize IGBT gate drivers for high insulation voltage capability (up to 30kV) is proposed. A Pot core ferrite with circular coils transformer is used for high insulation capabilities. The insulation voltage level is defined by the air gap length and the dielectric material. The pulse width modulation (PWM) signal transmission and power transmission functions of IGBT gate driver are studied and optimized. For both functions, the objective of the studies is to optimize the geometric elements of transformer and the associated electrical components by the help of a virtual prototyping tool. Therefore, the optimization results are proposed under Pareto fronts: optimization objectives for a set of the barrier insulation thickness. Finally, the experimental verifications are shown to validate the proposed methodology.

Keywords—Insulated gate bipolar transistor IGBT, gate drivers, high insulation voltage capability, planar transformer, PWM signal transmission, power supply function.

1. INTRODUCTION

For the application of IGBTs/MOSFETs in Medium Voltage (MV) converters or multilevel converters, gate driver need high insulation voltage capabilities. The main requirements of such system are safety and long production life. As depicted in Fig. 1a, the synopsis and functions of a single channel IGBT gate driver are: (i) switching signals transmission, (ii) defaults information, (iii) power transmission and (iv) protections [1-3]. In the proposed article, the authors address the optimization design of the PWM signal transmission function and power supply function. The galvanic insulation system can be performed through technologies such as: planar transformers [3-5], optical insulation system [6], and piezoelectric coupling [7]. According to [8], the optical insulation devices such as optocoupler have limited range of operating temperature less than 100°C. An addition to this, as discussed in [9], the optically power supply is today impractical because the power efficiency is limited to around 5%. Piezoelectric coupling cannot response to the high insulation voltage demand [9]. Moreover, the articles [10-11] present the comparison between coreless transformer and compact ferrite core transformer for this kind of application. As a result, with the same transformer dimension, a pot core ferrite transformer with circular coils on printed-circuit-board (PCB) provides the best performance for PWM signal transmission function with low average power consumption and high efficiency for power supply function. Thus, pot core ferrite transformers are used for both functions (PWM signal transmission and power transmission).

The optimization strategies of these functions are to optimize the geometric elements of transformer and their associated electronic components in their proposed circuits. The geometrical modeling of transformer is performed with finite element (FEMM^{TM}) software. The values of the electrical parameters of the transformer (L_p, R_p, L_s, R_s, M, k) and other electrical elements in the system are simulated with a transient electrical simulator (LTSpice^{TM}). Then, a genetic algorithm (GA) coded in a MATLAB^{TM} script is used to run FEMM^{TM} and LTSpice^{TM}. Thus, the optimization results are proposed under Pareto fronts' curves.

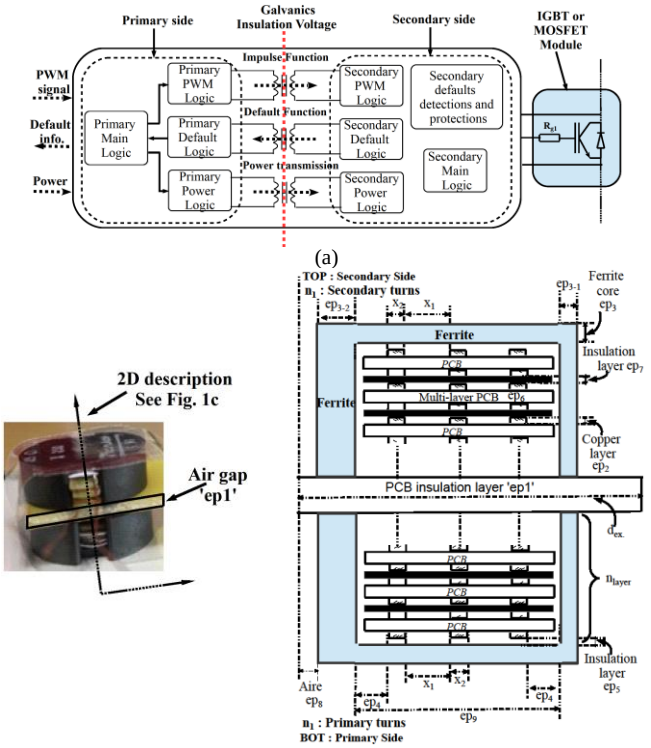


Fig.1 (a) Synopsis of a single channel gate driver. (b) a pot core ferrite planar transformer with winding on PCBs. (c) 2D descriptino of pot core planar transformer geometric.

This article is structured into four mains sections: Section 2 justifies the dielectric material for the insulation system. Section 3 describes the optimization design for PWM signal transmission function and power transmission function of IGBT gate drivers. Moreover, the optimization variables, parameters, constraints, and optimization processes are

detailed. Then, in Section 4, simulation results are provided. These results are compared with the experimental ones to validate the proposed methodology. Finally, the conclusions and perspectives are presented in Section 5.

2. Galvanic Insulation Barrier

2.1. Galvanic insulation barrier material and thickness

The galvanic insulator barrier suffers from two main issues under high electric fields. The first one is dielectric breakdown related to the bulk properties of the insulating materials (defects, electrical and mechanical properties, interfaces and electrode nature…) while the second is due to the external partial discharge occurrence related to the environment and electric field distribution around the electrodes which can lead to the sample degradation and its failure.

Firstly, the most used dielectric materials for galvanic insulation are categorized into ceramics and polymeric films [12]. Ceramic dielectrics have relatively low dielectric strength (<50kV/mm) due to the presence of grain boundaries, porosity, and other defects. Polymer dielectrics, especially unfilled films, have higher dielectric strength (>300kV/mm), lower dielectric loss (<0.01) and dielectric permittivity (<4).

According to the application needs (i.e. high dielectric strength and low dielectric constant at room temperature operation), it appears that polymers are more adequate than ceramics since they can withstand the target voltage with thinner films, and hence they allow the increase of the transformer efficiency. Among the different polymer dielectric, epoxy films are generally used in such application. However, their main drawback is the high water adsorption capability. The influence of water adsorption on epoxy composite has been widely reported. It has been evidenced that the moisture increases the dielectric permittivity and the loss tangent and reduces the breakdown voltage [13]. Similarly, fillers generally decrease the breakdown voltage of polymer. A hydrophobic and unfilled polymer, such polysterimide, is necessary to increase the breakdown voltage of the insulation barrier. Polysterimide has also a high dielectric strength (50-100 kV/mm), a low dielectric constant 3.5 and films of few millimeters are simple to prepare. The breakdown field and the reliability of polysterimide under AC voltage are experimentally investigated in Section 4.2.2. The influence of moisture and filler is also revised.

Secondly, the field distribution and the environment where the sample is placed can significantly change the partial discharge apparition and activity and hence affects the reliability of the dielectric. The reduction of field strength enhances significantly the system lifetime. For a constant applied voltage, the field strength can be essentially reduced by changing the nature of the packaging system (around the electrodes and the dielectric) as well as the geometry of insulator and the electrodes. As electrical discharges occur in air for a local field of 3 kV/mm (at room temperature and at atmospheric pressure), it is important to avoid the exposure of the system to ambient air. It should be provided to package the planar transformer within an insulator having higher dielectric strength than the air (such as gel or liquid insulator). It should be noted that higher is the permittivity of the packaging insulator, the lower is the local field.

2.2. Experimental validations of dielectric materials

In order to verify the influence of the moisture, fillers and sample diameter on the dielectric strength of the selected polymers experimental measurements are carried out. Breakdown measurements are done at a frequency of 50 Hz with an applied voltage up to 40 kV. In order to minimize the influence of surface discharges on the breakdown voltage, measurements are done in a sphere plane electrode system immerged in vegetal oil, as described in Fig. 2. The sphere and the plane electrode diameters are 2.5cm and 2cm, respectively. Breakdown is detected by the large current spike occurring when the sample is short-circuited by the breakdown arc.

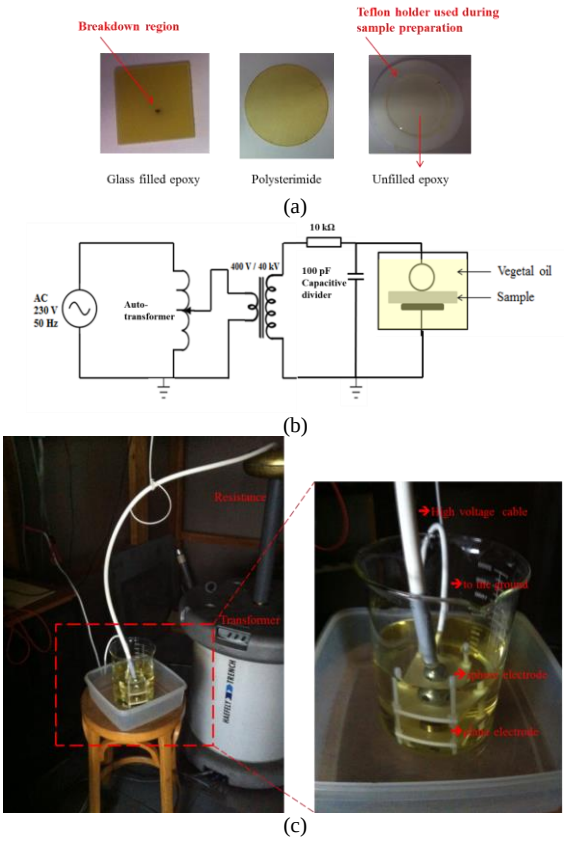


Fig. 2 Validation of the insulator breakdown voltages: (a) Sample insulator for testing experimental works: glass filled epoxy, polysterimide, (b) Schematic of the experimental set-up for breakdown measurement, (c) Experimental instruments for breakdown voltage measurement.

The breakdown measurements versus sample type, diameter and water content are presented in Table 1.

Table 1: Breakdown voltage of selected polymers versus sample diameter, fillers and water content (sample thickness is in the order of 1 mm)

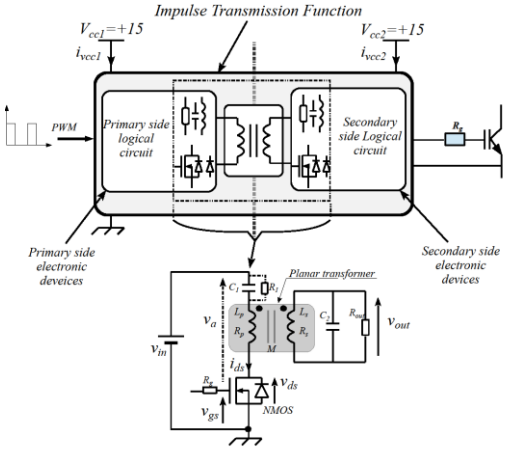
Polymer	**Specifications**	**Sample dia.**	**Breakdown voltage**
Epoxy	Unfilled – 0.8% of water content	40 mm	28 kV
	Glass filled epoxy (PCB – FR4) – ~ 0.2% of water content	25 mm	Surface discharges followed by breakdown at 37 kV
Polysterimide	Unfilled and hydrophobic polymer	25 mm	Surface discharges followed by breakdown at 40 kV (after 5 min)
		40 mm	> 40 kV No breakdown at 30 kV (for at least 2 hours)

The results demonstrate that the breakdown voltage is more influenced by the water content than the filler. One of the features of such results is that the volume dielectric strength of polysterimide (hydrophobic and unfilled polymer) is higher than 40kV for a thickness of 1mm. It can be used as insulator barrier for the pot core planar transformer while ensuring that its diameter is at least twice than that of the electrode subjected to the high voltage to avoid the flashover occurrence.

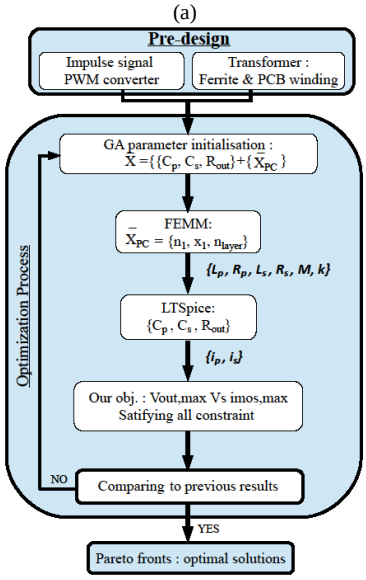
3. Optimization Design Consideration

In this section, the optimization design of PWM transmission and power transmission functions for high insulation voltage capability are presented.

3.1. PWM signal transmission function optimization



(a)



(b)

Fig.3 (a) Synopsis and schematic of the impusle tranmsission function based on a magnetic transformer. (b) GA flowchart for overall system optimization based on FEMM™ and LTSpice™.

As shown in Fig. 3a and depicted in [2], the synopsis and the schematic of impulse transmission function is presented. The galvanic insulation level depends on a barrier thickness (ep_1=0.5mm-3mm) and a dielectric material. The primary side of the transformer is a series resonant topology and an N-MOSFET. This MOSFET is used to generate an impulse voltage and a series capacitor C_1 to avoid a steady-state current in the primary side of transformer. Moreover, a fixed resistance R_1=10kΩ is placed in parallel to C_1. Then, at the secondary side of the transformer a parallel resonant topology is proposed {L_s, R_s} and C_2. Then, the authors define three electrical variables: C_1, C_2 and R_{out}. The other variables are related to the pot core planar transformer geometry (n_1, x_1, n_{layer}) (cf. Fig. 1c).

Two criteria are proposed to be defined as objective functions in the optimization process: the maximum value of the output voltage v_{out} (to be maximized) and the maximum value of the primary current i_{mos} (to be minimized) of the proposed circuit. Then, according to Pareto front results, additional aspects such as propagation delay is considered by driver designers to choose the final design.

3.1.1. Signal transmission optimization variables and parameters

Optimization variables: as previously presented, the six optimization variables are summarized here:

$$X_{PWM} = (n_1, x_1, n_{layer}, C_1, C_2, R_{out})^t$$

- n_1: turn number on primary/secondary sides,
- x_1: distance between two copper windings,
- n_{layer}: number of layers,
- C_1: series capacitor on the primary side,
- C_2: parallel capacitor on the secondary side and
- R_{out}: parallel resistor on the secondary side.

Then x_2 is considered as an internal optimization variable. According to Fig. 1c, this variable can be computed as a function of the geometrical variables n_1 and x_1.. x_2 is also as function of some fixed parameters (ep_9 and ep_4).

$$x_2 = \frac{ep_9 - 2\times ep_4 - (n_1 - 1)x_1}{n_1} \quad (1)$$

Optimization parameters: according to Fig. 1c, the constant parameters' definitions and their values are:

- ep_1={0.5mm, 1mm, 1.6mm, 2mm, 2.5mm, 3mm},
- ep_2={70µm, 105µm}: copper thickness;
- ep_4=0.2mm : extra length of the ferrite relative to the edge of the last coil,
- ep_6=0.4mm : PCB thickness for multi-layers assembling,
- ep_7=18µm : insulation thickness between layers,
- {ep_3, ep_{3_1}, ep_{3_2}, ep_8, ep_9, ep_{10}}: pot core dimensions (D_F = {7mm, 9mm, 14mm}),
- $ep_5 = ep_{10} + ep_7 - n_{layer}(ep_6 + ep_7 + 2ep_2)$ (2): insulation between coil and ferrite

3.1.2. Optimization objective, constraints and process

The first objective is to obtain the maximum value of V_{out} and the second one, which has to be minimized, is primary current i_{mos}. V_{out} must be maximized to increase the electromagnetic immunity of the system, where i_{mos} must be minimized to decrease the average power consumption of the system. The Pareto front of V_{out} against i_{mos} is the main plot to be analyzed to choose the suitable configuration.

The flowchart of the optimization procedure is presented in Fig. 3b. To achieve the optimization objective, the optimization design must verify some constraints:

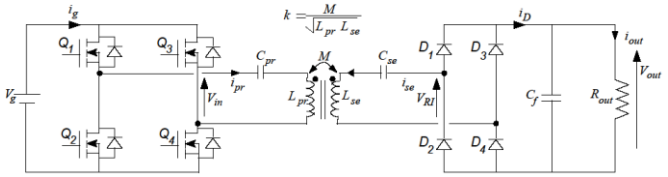
- n_1, n_{layer} ϵ {2,3},
- x_1 ϵ [0.2mm, 0.4mm],
- C_1, C_2 ϵ [0.1nF, 1nF],
- R_{out} ϵ [1kΩ, 10kΩ],
- $B_{max} < B_{sat}$: induction of pot core ferrite,
- ep_5 < 0.3mm, and
- C_{ps}<10pF: parasitic capacitor of transformer (primary side to secondary side).

3.2. Power transmission function optimization

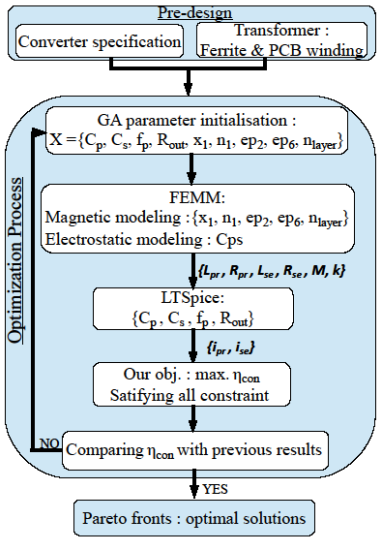
According to the articles [11,14-15], a dc-to-dc full-bridge series-series (FBSS) resonant converter (depicted in Fig. 4a) is a suitable topology for power transmission function for IGBT gate drivers. The advantages of this converter are: high efficiency with the operation in zero voltage switching (ZVS) conditions, enhance the energy transfer from primary to secondary by the help of both series capacitors, etc. The analysis of this resonant converter is organized as follow: series-series (SS) resonant tank modeling, voltage transfer ratio

considerations, ZVS conditions, frequency controllability of SS tank, capacitor compensation calculations, equivalent impedances, robust controller design are detailed in the previous publications [11, 14-16].

Based on the losses calculations in [15], the converter efficiency is derived. The converter efficiency is set as our main optimization objective. Then, for a set of barrier thickness, several Pareto fronts (proposed the converter efficiency against converter output power) are obtained. This converter output power helps us to choose the suitable solution.



(a)



(b)

Fig.4 (a) Dc-to-dc full-bridge series-series (FBSS) resonant converter. (b) GA flowchart for overall power transmission system optimization based on FEMM™ and LTSPice™.

3.2.1. Power transmission optimization variables and parameters

Optimization variables: n_1, x_1, n_{layer} are considered as geometrical optimization variables. Pot core with 14mm, 18mm, 22mm of diameters are selected for this application. Thus, the copper thickness (ep_2) and multilayer thickness (ep_6) are also regarded as optimization variables.

Moreover; to achieve ZVS condition and high efficiency; C_{pr}, C_{se}, f_p and R_{out} are considered as electrical optimization variables.

$$X_{power} = (n_1, x_1, n_{layer}, ep_2, ep_6, C_{pr}, C_{se}, f_p, R_{out})^t$$

Optimization parameters: the constants parameters are summarized as follow:

- ep_1 = {0.5mm to 3mm},
- ep_4 = 0.2mm,
- ep_7 = 18µm,
- D_F = {14mm, 18mm, 22mm},
- ep_3, ep_{3_1}, ep_{3_2}, ep_8, ep_9, ep_{10}: depend on pot core dimensions,
- ep_5 : equation (2), and
- x_2 : equation (1).

3.2.2. Optimization objective, constraints and process

The main objective is to maximize the converter efficiency η_{con}. Then, the Pareto fronts' results propose the converter efficiency against the converter output power. The flowchart of the optimization process is summarized in Fig. 4b. And some variables and technical constraints are listed as follow:

- $x_1 \in$ [0.2mm, 0.5mm],
- $n_1 \in$ {1, 2, 3, 4, 5},
- $n_{layer} \in$ {2, 3, 4},
- $ep_2 \in$ {35, 70, 105, 210, 235, 435} [µm],
- $ep_6 \in$ {0.4, 0.5, 0.8, 1.2, 1.6} [µm],
- C_{pr}, $C_{se} \in$ [1nF, 100nF],
- $f_p \in$ [150kHz, 1MHz],
- $R_{out} \in$ [10Ω, 100Ω],
- $V_g \leq V_{out} \leq$ 20V, $i_{out} \leq$ 0.5A, $f_{res} \leq f_p \leq f_v$,
- $B_{max} \leq B_{sat}$, $k \geq 0.2$, $ep_5 \leq$ 0.5mm, $C_{ps} \leq$ 10pF.

4. Simulation and Experimental Results

In this section, optimization results of PWM signal transmission and power transmission functions are presented and analyzed. Furthermore, the experimental results are compared to the simulation ones to validate the proposed methodology.

4.1. Simulation results

4.1.1. PWM signal transmissionfunction

The parameters of the genetic algorithm (GA) are: 10 individuals and 50 generations which require 2 hours of computation times (with an Intel Core 2Duo CPU, DELL). Fig. 5a illustrates the Pareto fronts' curves for different insulation barrier thickness (ep_1 = {0.5mm, 1mm, 1.6mm, 2mm}), different ferrite maximum diameters (7mm, 9mm and 14mm). According to the insulation material validation in Section 2, a 0.5mm thickness of polysterimide is a suitable choice for medium voltage applications (where the insulation voltage is up to 30kV). As presented in Fig. 5d, two Pareto fronts from two different ferrite diameters (D_F = 7mm and 9mm) are plotted in the same graph. Based on these Pareto fronts, the optimal solutions of a pot core of 9mm (diameter) provides the best performance with low power consumption compared to the 7mm ones. Thus, the optimal solutions {(a_2), (b_2), (c_2), (d_2)} are the dominants solutions. Nevertheless, the solution (a_1) would be interesting to be compared to solution (a_2).

Amongst these four solutions, the power consumptions are nearly the same based on the value of i_{mos}. Thus, as the secondary power electronic devices require the supply voltage around 5V, the solution (d_2) is the best choice by reserving a little voltage drop over the system. The optimization results of the selected solution (d_2) are presented in Table 2. Capacitor C_1 is equal to 108pF and C_2 to 316pF. The parallel resistance R_{out} = 30kΩ is needed. The characteristic of the optimal transformer are: 2 double layers per side, 2 turns windings on PCB, and distance between the coppers x_1 = 0.32mm. From the FEMM simulation; $L_{pr} = L_{se}$ = 2.03µH, $R_{pr} = R_{se}$ = 0.26Ω and coupling value k=0.776 are the electrical values of the optimal transformer.

Table 2: Optimization results of solution (d_2)

Opti. obj.	**Solution (d_2)**		
V_{out} / i_{mos}	5.8V / 0.15A (see Fig. 6)		
ep_1/D_F	0.5 mm/9 mm		
C_1 / C_2	108.64 pF/ 316 pF	L_p / R_p	2.03 µH / 0.26Ω
R_{out}	30 kΩ	L_s / R_s	2.03 µH / 0.26Ω
x_1	0.32 mm	M	1.57 µH
n_1/ n_{layer}	2 turns / 3 layers	k	0.776

Fig. 5e and 5f show the simulation waveforms of output voltage (V_{out}), primary side current (i_{mos}) of the proposed circuit for the chosen solution (d_2).

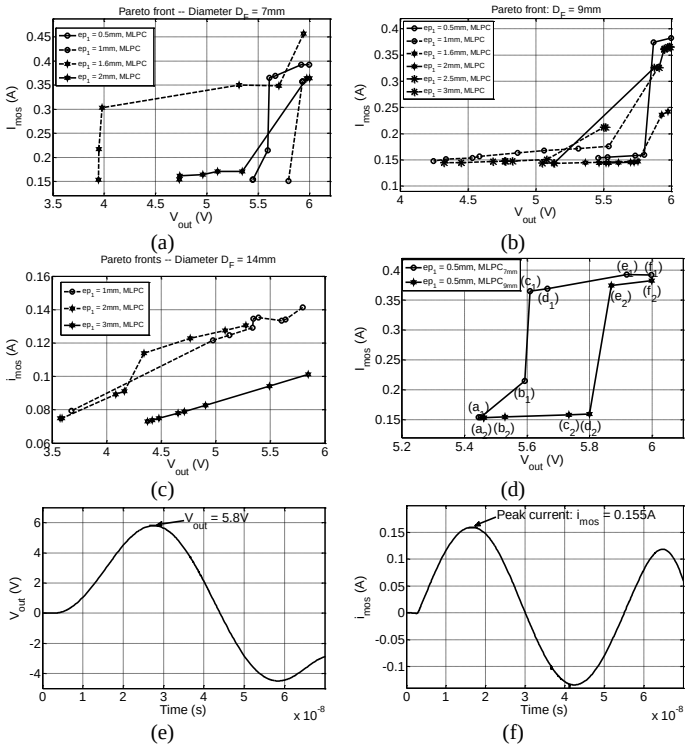


Fig.5 Pareto fronts' results: (a) for D_F = 7mm, (b) for D_F = 9mm, (c) for D_F = 14mm, (d) for our design target. (e) output voltage V_{out} waveform, and (f) primary side current waveform i_{mos} for solution (d_2)

4.1.2. Power transmission function

The Pareto fronts are proposed: the converter efficiency (η_{con}) as function of the converter's output power. The parameters of the GA are: 30 individuals and 100 generations which require 4 hours of computational times. Fig. 6 shows the Pareto fronts' results for the set of diameter and air gap length ep_1. Theoretically, for the same ferrite diameter and the same winding configurations, the lower air gap length leads to have a higher coupling coefficient (k) and higher inductor values (k_{ep1}=0.5mm>k_{ep1}=1mm and L_{ep1}=0.5mm>L_{ep1}=1mm). Moreover, from the FOM (Figure Of Merit) factor analysis in [17], the converter efficiency is expressed as: $\eta \approx 1 - 2/(kQ)$. Where, the inductive quality Q is proportional to the inductance and frequency, but inverse to the winding resistance. So, the higher magnetic coupling k, L_{pr} and L_{se} values provide the higher converter efficiency.

The proposed converter is designed to drive a 3.3kV IGBT module in MV converter where the dc-bus is equal to 20kV - 30kV. Hence, the galvanic insulation voltage of each gate driver system is normally higher than the dc-bus voltage. And the required power supply for this system is estimated to around 2W. Thus, as presented in Fig. 6d, the solution (a) is selected to build a prototype with an air gap of 0.5mm. The simulation results of this solution are summarized in Table 3. The converter needs to operate at 266kHz to achieve ZVS conditions and obtain high efficiency. Series capacitors are equal to 68nF. The characteristics of the optimal transformer are: 4 multi-layers, 2 turns per side of layer, 105µm of copper thickness, etc. As a result, L_{pr} = L_{se} =17.24µH, R_{pr} =R_{se} = 0.46Ω and C_{ps} = 6.67pF are the electrical values of this optimal transformer.

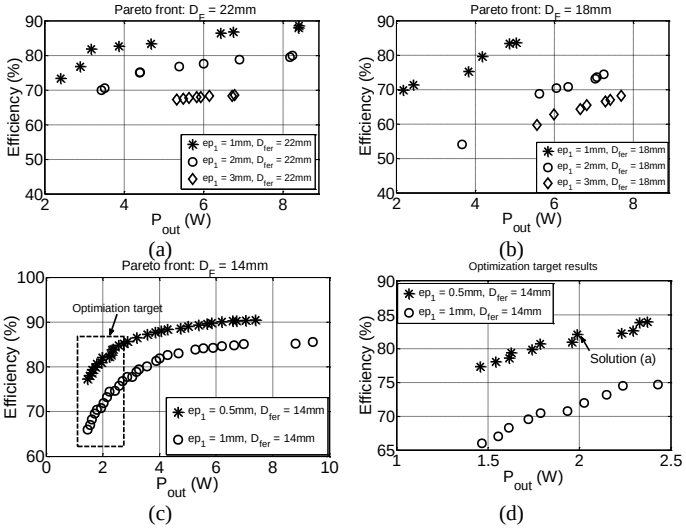


Fig.6 Pareto fronts' results of power supply function: (a) for D_F = 22mm, (b) for D_F = 18mm, (c) for D_F = 14mm, and (d) for our design target.

Table 3: Optimization results of solution (a)

Opti. Obj.	**Solution (a)**		
η_{con}	82 %		
ep_1/D_{Fer}	*0.5 mm/14 mm*		
C_{pr}/ C_{se}	*68 nF/ 68 nF*	P_{out}	*2 W*
f_p	*266 kHz*	V_{out}/ I_{out}	*13.3V/ 0.16A*
R_{out}	*76.9 Ω*	L_{pr} / R_{pr}	*17.24 µH/ 0.46Ω*
x_1 / x_2	*0.25 mm /0.87mm*	L_{se} / R_{se}	*17.24 µH/ 0.46Ω*
n_1 / n_{layer}	*2 turns / 4 layers*	M / k	*10.49 µH / 0.78*
ep_2 / ep_6	*105 µm / 0.4 mm*	C_{ps}	*6.67 pF*

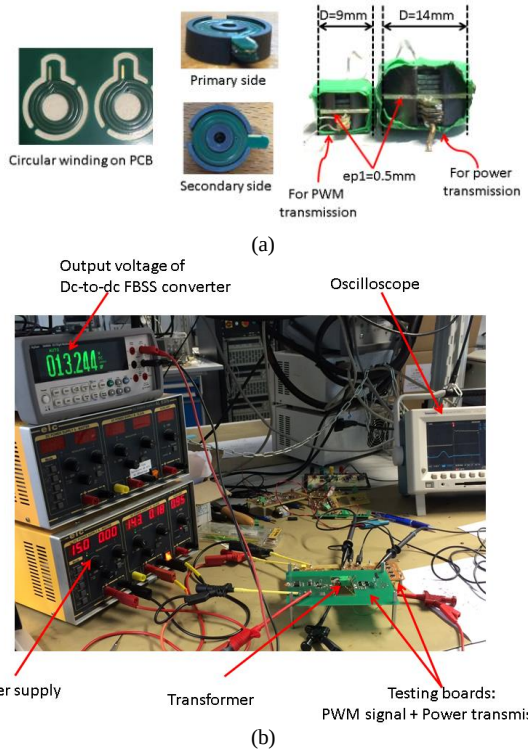


Fig.7 (a) Synopsis of a single channel gate driver. (b) a pot core ferrite planar transformer with winding on PCBs. (c) 2D description of pot core planar transformer geometric.

4.2. Comparison results

Fig. 7 presents the experimental set-up. Two different transformers with different diameters are built. One for the PWM signal transmission function (9mm of diameter) and

another one for the power transmission function (14mm of diameter).

4.2.1. Power transmission function validations

According to Table 3, the characteristics of the dc-to-dc FBSS resonant converter are: P_{out} = 2W, V_{out_power} = 13.3V. As presented in Fig. 7b, the output voltage of the converter is 13.2V with the input voltage of 14.3V. For more comparisons, the voltage transfer ratio G_v of the converter is plotted in Fig. 8a. Then, the comparison waveforms of input voltage V_{in}, primary side current i_{pr} and secondary side i_{se} current at 266kHz between the simulation and experimental works are illustrated in Fig. 8b. Moreover, the efficiencies validations are also plotted in Fig. 8c.

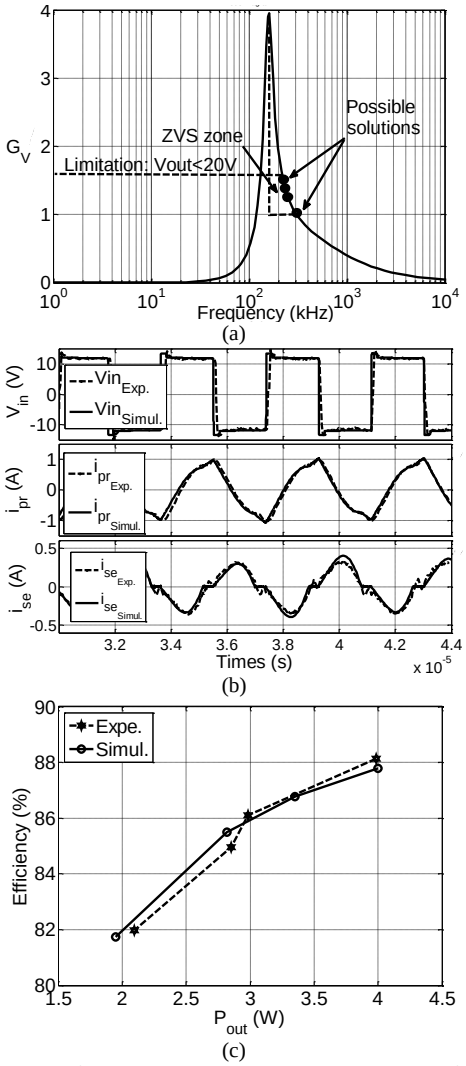


Fig.8 (a) Synopsis of a single channel gate driver. (b) a pot core ferrite planar transformer with winding on PCBs. (c) 2D description of pot core planar transformer geometric.

4.2.2. PWM signal transmission function validations

Fig. 9a presents the experimental results of the output voltage V_{out}, a drain-source V_{ds} voltage of N-MOSFET at primary side and a gate-emitter voltage V_{ge} of an IGBT module. According to this figure, the propagation time measure between the V_{ds} of N_MOSFET and V_{ge} of IGBT is around 70ns. This propagation delay is the same as mentioned in [2], but this proposed solution with pot core ferrite transformer consumes less power compared to [2].

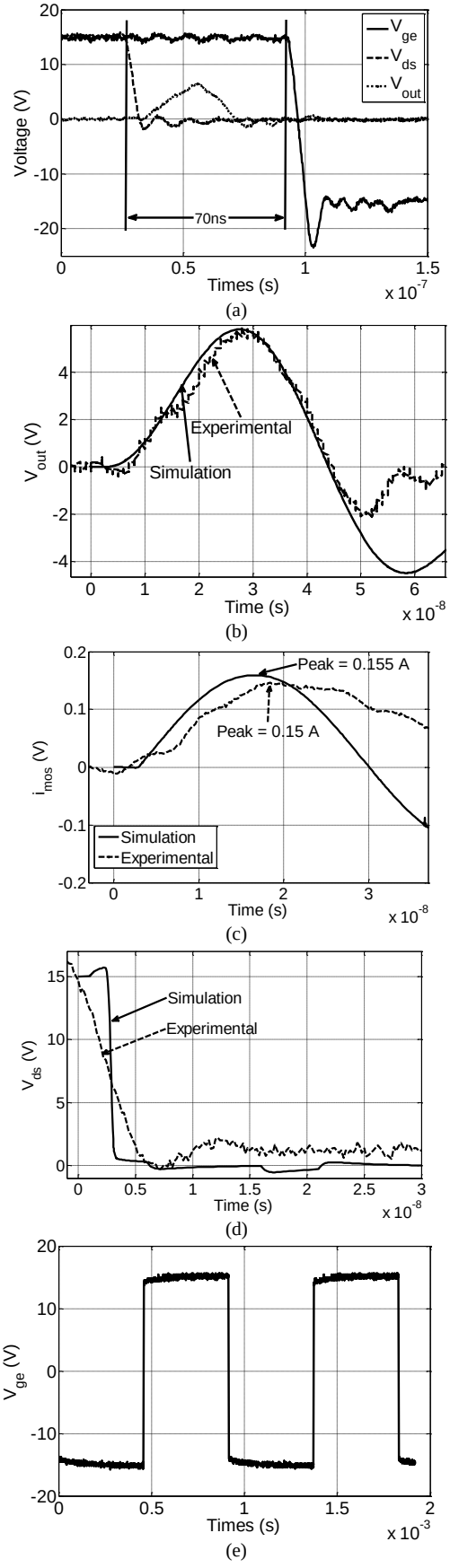


Fig. 9 (a) Synopsis of a single channel gate driver. (b) a pot core ferrite planar transformer with winding on PCBs. (c) 2D description of pot core planar transformer geometric.

To compare the simulation results to the experimental ones, the output voltage V_{out} of the transformer is the most important variable to be considered. As illustrated

in Fig. 9b, $V_{out,max}$ is about 5.8V in both (simulation and experimental) results. And the rise time to the peak is around 20ns. Moreover, for further validation, the comparison of i_{mos} and V_{ds} waveforms between the simulation and experimental results are shown in Fig. 9c and Fig. 9d, respectively. Then, the V_{ge} voltage of IGBT module is equal to -15V or +15V as presented in Fig. 9e.

5. CONCLUSIONS

This paper presents the optimization design methodology for high insulation voltage capabilities PWM signal transmission function and power transmission function IGBT gate drivers. The galvanic insulation voltage level is based on an air gap length of pot core planar transformer and dielectric material. According to the measurements of insulation materials, with 0.5mm thickness of Polysterimide material, the 20kV to 30kV of insulation voltage level can be achieved. This voltage rang is suitable for Medium Voltage converter applications.

For the signal transmission function, the optimization of the transformer and some other electrical components in a circuit is applied by the help of a virtual prototyping tool. Then, after the bi-objective optimization is defined, several Pareto fronts are plotted with a set of barrier insulation thickness. Finally, the optimal solution (d_2) from 9mm of pot core diameter is chosen. The output voltage is around 5.8V is achieved for an insulation thickness of 0.5mm

For the power transmission function, a dc-to-dc FBSS resonant converter is proposed. The optimization of this converter is to optimize the pot core transformer and other electrical devices which can achieve high efficiency. With a set of barrier thickness, several Pareto fronts are obtained from optimization process. As a result, a solution (a) from 14mm of pot core ferrite diameter and 0.5mm of thickness is selected.

Then, these two functions are optimized, the optimal transformers and testing boards are built to process the experimental works. For the signal transmission function, the propagation delay is around 70ns (from the primary side to the gate voltage of the IGBT module). A dc-to-dc FBSS converter board is built to provide a 13V to 15V DC voltage to the secondary side of our gate driver system. This work is also validated by the experimental results by comparing several aspects: input voltage waveforms, input current, secondary side current, efficiency measurement, etc.

The coming steps are to propose gate driver design for a sub-module (an inverter leg with a capacitor) of Modular Multi-level Converter (MMC) for Medium Voltage application.

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