An Adaptive Mesh Refinement Strategy of Substrate Modeling for Smart Power ICs

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***Abstract*—Substrate noise coupling due to minority carriers propagation in smart power integrated circuit becomes a critical issue specially for high voltage applications. Computer-Aided-Design modeling methodology for substrate parasitic-immune design was introduced. It is based on constructing a 3D substrate equivalent network. The substrate equivalent network consists of models of diodes and resistors that are capable of preserving the continuity of minority carriers. In this paper, an optimized meshing topology for substrate modeling is introduced. This meshing topology contributes significantly in the extracted component reduction and hence speeds up the simulation while improving the convergence of the simulator. A typical NPN bipolar transistor is used as case study. Comparing the proposed meshing topology to the basic meshing topology, the number of extracted components is reduced by 78% and the simulation time is lowered by 88%. SPICE-like analysis results confirm the accuracy of modeling approach with an acceptable relevant error (<10%) compared to standard model. With the proposed meshing topology, it is feasible to model the substrate parasitic of more complex smart power integrated circuit.**

I. Introduction

Nowadays, the modern trend is to integrate complex low voltage (LV) and high voltage (HV) circuits. This combination of power stages, analog and digital blocks on a single chip is called Smart Power integrated circuits [1][2]. Unlike traditional integrated circuit, the smart power ICs has to withstand some hostile environment conditions like high voltages (HV), high temperatures (HT), power switching, voltage overshoot and electromagnetic interference (EMI). This new integration approach aims at cost saving and high reliability.

Clearly, the smart power ICs are becoming increasingly attractive to automotive industry. Yet they require to address electronics failures in order to guarantee more robust and reliable products. This kind of electronics failures due to substrate noise coupling are still reported in industrial tests after silicon fabrication. Minority carriers injection and propagation in substrate are the major causes of failure in smart power ICs. Hence, modeling the minority carriers is still necessary in high voltage applications [3]. A novel Computer-Aided-Design modeling methodology for substrate coupling-immune designs has been introduced in [4]. It proposes an automated approach for modeling the substrate. This approach relies on automatically extracting the substrate equivalent model from the layout. The equivalent substrate model consists of a netlist of enhanced diodes and resistors that ensure the continuity of the minority carrier propagation [5].

Substrate modeling is a difficult task because the substrate currents are of three dimensional nature and are strongly layout-dependent. Moreover, silicon design layout for safe circuit operation is complex and depending on the background of designer. Modeling approach for generating 3D mesh network is typically used for physical simulation such as finite element analysis, e.g. Technology Computer-Aided-Design (TCAD) tools [6] of device simulation. Previous works in [7] provide an efficient solution compared to TCAD in terms of fast layout extraction and circuit simulation. This paper provides an optimized meshing topology for layout-based substrate modeling. Comparing the proposed meshing topology to the basic one, shows significant improvement on component reduction and simulation time. A standard model of NPN bipolar transistor is depicted in Figure 1, which is used as a case study and validate the modeling results.

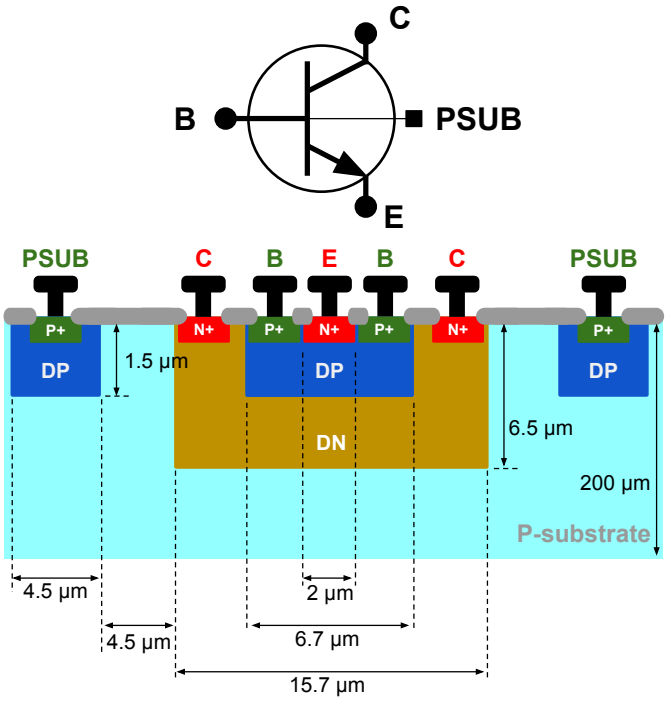

Fig. 1: Typical NPN bipolar transistor (top), and its simplified layout cross-section view (bottom).

The paper is organized as follows. Section II introduces the layout-based substrate modeling methodology and proposed meshing topologies. SPICE-like simulations using the modeling methodology are performed, and results are reported in Section III. Finally, the conclusions are drawn in Section IV.

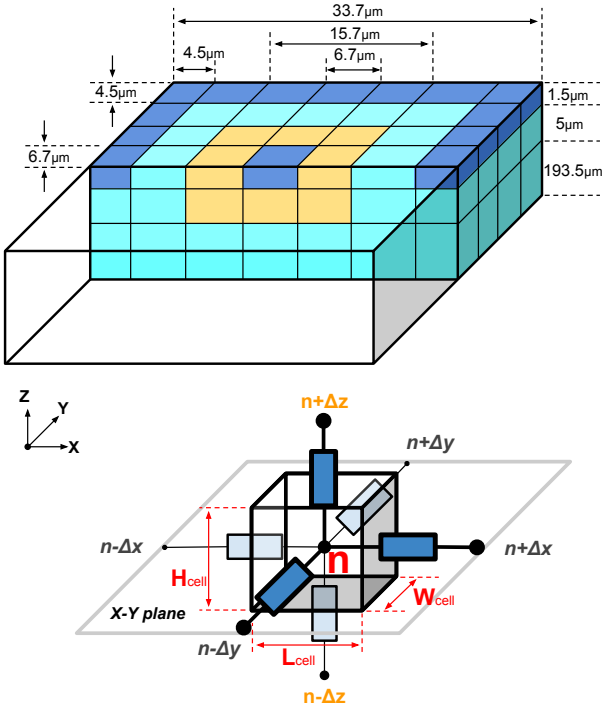

Fig. 2: Representation in 3D of substrate with rectilinear mesh network (top). Illustration of mesh cell inside mesh network and the neighboring connections (bottom).

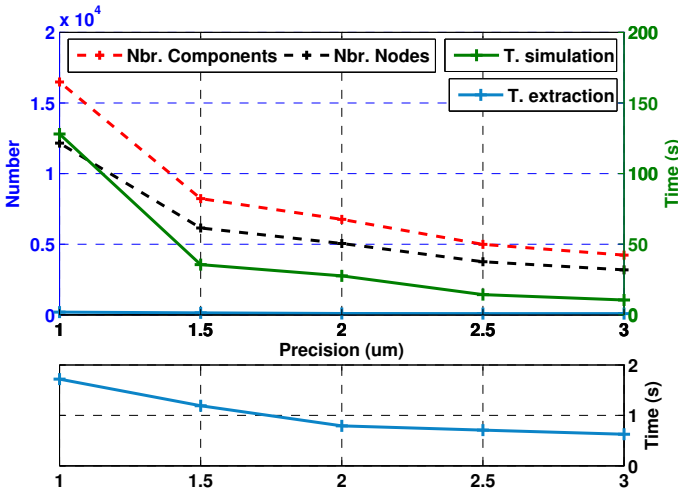

Fig. 3: Relations between size limit (from 1μm to 3μm) of mesh cell, number of extracted components, number of nodes and computational cost (top), a region zoomed for extraction time (bottom).

II. Meshing strategy for substrate modeling

Methodology of 3D substrate modeling requires a feasible mesh generation strategy that respects both simulation accuracy and computational cost (extraction and simulation). We give the main idea to perform a 3D (X-Y-Z space) extraction by focusing on the mesh refinement strategy in 2D (X-Y plane): from the basic meshing topology to the optimized one. To ease the presentation, section II-A and section II-B illustrate the layout extraction without N+ and P+ regions, since full layout extraction will take into account the N+ and P+ regions. Section II-C explains how this method is applied to extract a whole NPN bipolar transistor with its 3 connections (base, emitter and collector).

A mesh network is a series of cells that are efficiently spaced in a combined form. Each cell is a cuboid shaped element, which owns 6 faces, 12 edges and 8 vertexes, as shown at the bottom of Figure2. The extracted cell has additional variables corresponding to the spatial coordinates of its center and its physical parameters, such as doping profiles. The center of a cell represents an electrical node in the extracted netlist. A parasitic component is extracted from 2 adjacent cells, having 2 connections corresponding to the 2 centers of these cells. Considering one node in the extracted netlist, related components are geometrically interconnected to this node, typically in six directions: in the front (n-Δy), at the back (n+Δy), on the left (n-Δx), on the right (n+Δx), on the top (n+Δz) and at the bottom (n-Δz). There are three types of parasitic components: diode (different doping types), resistor (same doping type) and homo-junction (same doping type but different concentration). Related geometrical parameters are described as follows:

- Length: $L_{model} = L_{Cell\ n}/2 + L_{Cell\ n+\Delta x}/2$
- Surface: $A_{model} = W_{Cell\ n} \times H_{Cell\ n}$
- Geometrical ratio: $Rg_{model} = L_{Cell\ n+\Delta x} / L_{Cell\ n}$

Key factors that affect the quality of substrate modeling are the total number of parasitic components. The finer the mesh cell is, the more lumped elements will be extracted, which produces the results that could be more accurate yet time consuming. Moreover simulation accuracy is not directly related to precision of mesh, since a great number of components involved, may cause inaccurate results due to convergence issues. Graphs shown in Figure 3 illustrate the relations between size limit of mesh cell, number of components and computational costs (extraction and simulation). Note that size limits defines the maximum size of extracted mesh cell.

A. Basic meshing topology in 2D

To introduce our meshing strategy, we start with the basic meshing topology. Let us consider the initial mesh network consisting of 49 cells (7x7), as illustrated in Figure 4. The basic mesh network is a rectilinear grid, it is a tessellation by rectangles that are not, in general, all congruent to each other. Each cell can be systematically identified by the indexes: from A to G on the Y-axis and from 1 to 7 on the X-Axis. For instance, A1 and G7 relate to the upper left cell and lower right cell in the mesh network respectively. In view of 2D (X-Y plane), the parasitic components are extracted (or connected) between the center of adjacent cells (or electrical nodes), while each cell has adjacent cells oriented along four directions: the positive and/or negative Y direction, the positive and/or negative X direction. In other words, parasitic components are extracted horizontally and vertically in each X-Y planes. A summary of component extraction is reported in Table I that will be further discussed in section II-B. On the one hand, this

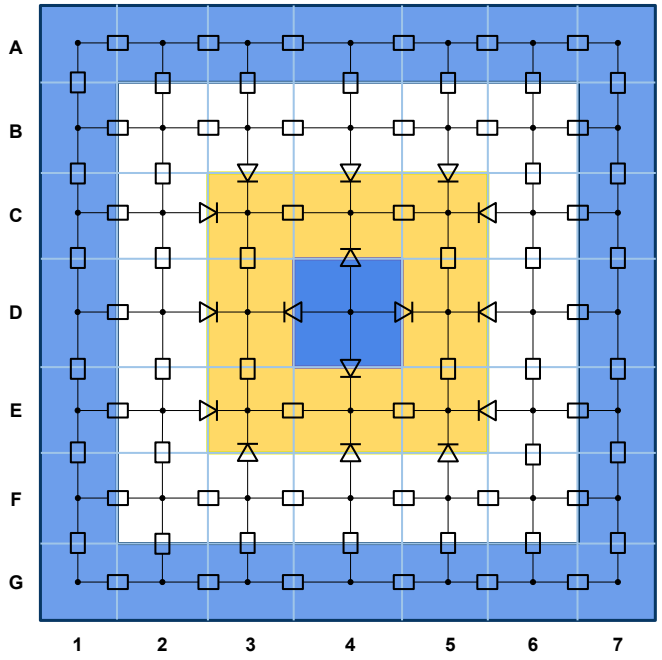

Fig. 4: Modeling part of NPN bipolar transistor structure using basic meshing topology, illustration in X-Y plane (not showing N+ and P+ regions).

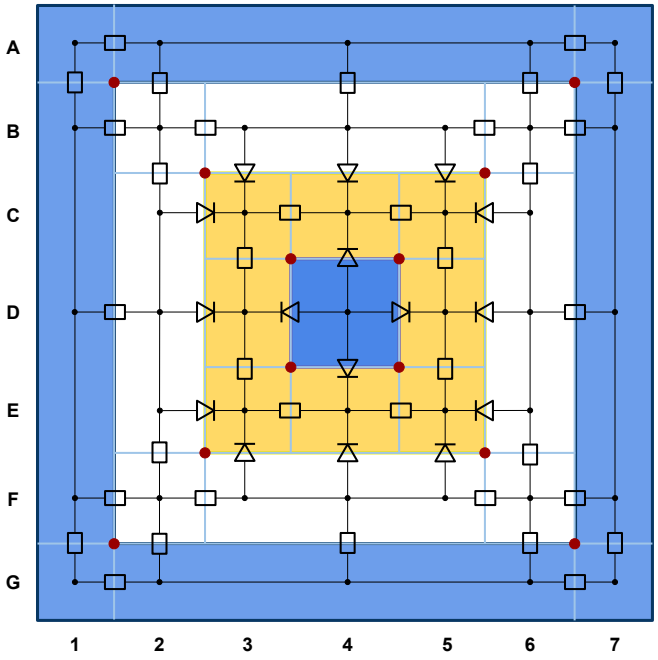

Fig. 5: Modeling part of NPN bipolar transistor structure using non-uniform meshing topology, illustration in X-Y plane (not showing N+ and P+ regions).

meshing topology is simple and easy to construct. One the other hand, the number of extracted components is large and resulting simulation time is long.

TABLE I: Report of component extraction in 2D: extraction of layout without N+ and P+ regions.

Meshing strategy	**'Basic'**	**'Non-uniform'**	Reduction
$Nbr._{\text{nodes}}$	49	25	48%
$Nbr._{\text{components}}$	84	52	38%
$Nbr._{\text{resistances}}$	68	36	47%
$Nbr._{\text{diodes}}$	16	16	0%

B. Non-uniform meshing topology in 2D

We introduce in this section a mesh refinement strategy, called "non-uniform" meshing topology. It applies a merging procedure of cells to decrease the number of extracted components, which translates the netlist of Figure 4 into the one of Figure 5. The resulting mesh network consists of a series of optimized cells where each cell may have more than one adjacent cell facing one side. The construction of the optimized mesh is based on the layout geometry and the doping regions. The new vertex points (red points in Figure 5) are derived from the corner between two regions of different doping. From these vertex points, we generate the merged cells and the optimized mesh network. For instance, the cell resulting from merging cells B1, C1, D1, E1 and F1 is called cell {B,C,D,E,F}1 and so on. Once the mesh network is changed, the resulting netlist is changed also: parasitic components are extracted between adjacent cells according to the intersection area. Then the terminals of extracted component are connected to each adjacent node. For instance, node {B,C,D,E,F}1 connects to neighbor nodes A1, B2, {C,D,E}2, F2 and G1 via five parasitic resistors respectively. The extraction results reported in Table I show that, the number of cells (or electrical nodes) reduces from 49 to 25 (by 48%), and the number of components reduces from 84 to 52 (by 38%, and 47% for resistor only).

C. Extraction of top side component

The top side components are extracted at the edge where substrate and active regions interconnect (e.g. the intersection areas between diffusion regions and N+ or P+ regions). They are vertical components and act as the connectors to circuit netlist. Homo-junction is one kind of top side component and normally extracted at the edge to highly doped region, such as deep P-well to P+ region or deep N-well to N+ region. Diode is another kind of top side component and can be extracted

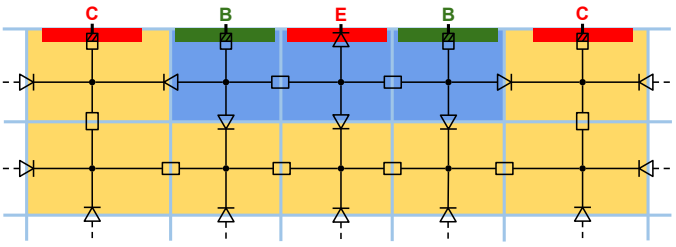

Fig. 6: Cross section view of extracted netlist where we focus on the body of NPN device, including N+ (red) and P+ (green) highly doped region.

between the region of different doping types, such as N+ region to deep P-well. As illustrated in Figure 6, a vertical diode is extracted between emitter to base of NPN bipolar transistor.

III. Simulations and Results

Circuit simulations are performed using extracted netlists of two meshing topologies: complete layout extraction (including N+ and P+ region) using the methods presented in Figure 4 and Figure 5. Results are compared to standard model of NPN bipolar transistor (Figure 1, from ams AG $0.35\mu m$ high voltage technology). A DC sweep analysis is performed from 0V to 10V and biased at the collector while the emitter is grounded and the base is connected to a current source at: $0\mu A$ (red), $10\mu A$ (green), $50\mu A$ (blue) and $100\mu A$ (black) respectively, as depicted in Figure 7. Result shows an error less than 10% compared to standard model. While applying the "non-uniform" meshing topology, the number of components reduces by 78%, the accuracy of simulation maintains the one provided by the basic meshing topology. Moreover, there has been a significant improvement in the simulation cost, about 88% time saving, as reported in Table II. Works were performed with Intel Core i5-3470S Processor (2.9 GHz).

TABLE II: Report of extraction in 3D and computational cost. Modeling and simulation of complete layout from Figure 1.

Meshing strategy	**'Basic'**	**'Non-uniform'**	*Reduction*
$Nbr._{\text{nodes}}$	2650	490	81%
$Nbr._{\text{components}}$	3531	763	78%
$Nbr._{\text{diodes}}$	351	111	68%
$Nbr._{\text{homo-junction}}$	128	24	81%
$Nbr._{\text{resistor}}$	3052	628	79%
T_{Elapsed} (s)	21.5	2.4	88%
T_{CPU} (s)	20.7	1.91	90%

IV. Conclusion

This work provides an optimized meshing topology of layout-based substrate modeling approach for smart power ICs. Layout extraction and 3D mesh generation were implemented for a typical NPN bipolar transistor. SPICE-like simulations confirm the accuracy of modeling results with an acceptable relevant error ($<10\%$) to standard model. For the meshing strategies, comparison between the basic meshing topology and the proposed "non-uniform" meshing topology were illustrated. The number of extracted components were significantly reduced by using the optimized one, even for the large scale circuit with multi-devices. Furthermore simulation time was 9 times faster than the one performed by basic meshing topology. In a word, the CAD tool of substrate modeling provides a feasible and reliable solution for the modeling of more complex power integrated circuits.

Acknowledgment

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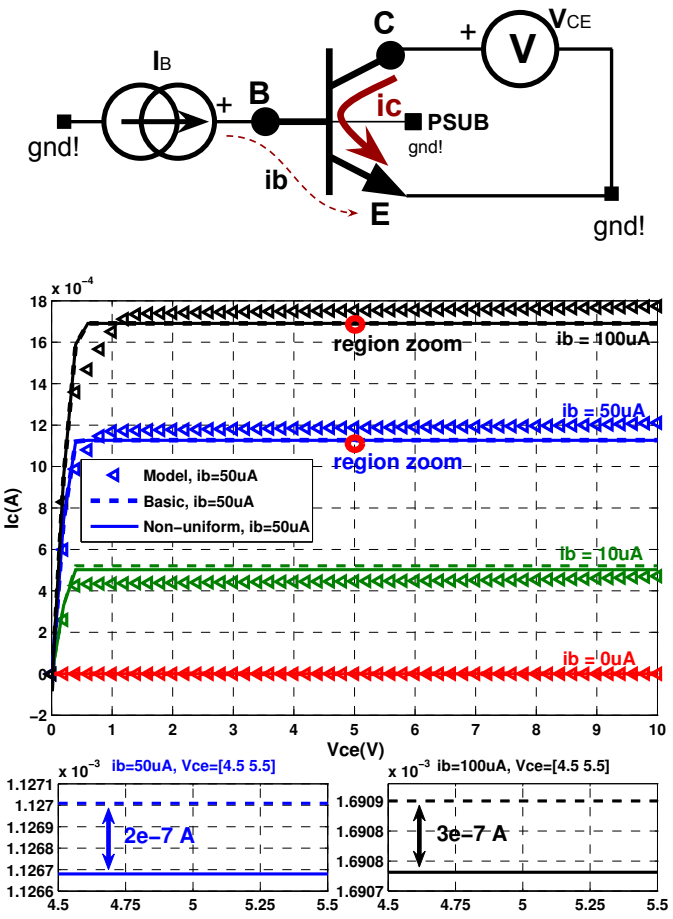

Fig. 7: Simulation testbench (top) and output characteristics curves of NPN bipolar transistor (bottom): model (triangle), extracted substrate model using basic meshing topology (dash line) and extracted substrate model using non-uniform meshing topology (solid line).

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