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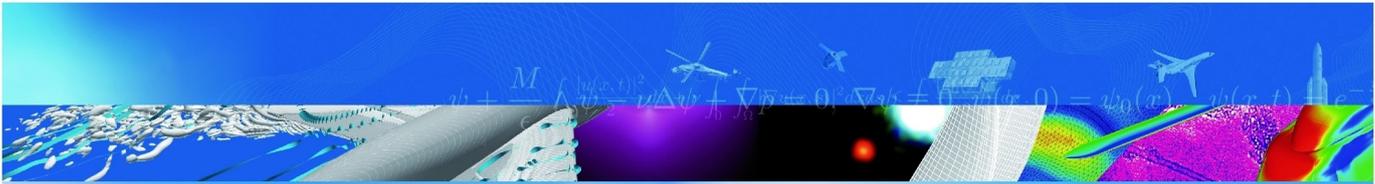
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COMMUNICATION A CONGRES

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Radiation Prediction Tool Dedicated to Analyze and Harden by Design readout circuits of photonic ICs

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Summary

This work presents an SEE prediction tool called MUSCA SEP3 and its interest in failure investigations and in providing a help for designers with the aim to optimize the SEE sensitivity of Sofradir readout circuit. Estimations and a failure analysis at circuit level were presented. Comparisons between predictions and experimental data obtained under heavy ion are consistent. Analyses of critical area of the cell allow to propose a hardening technique which reduces the SEE sensitivity of the D Flip-Flop (D- FF) of the readout circuit without any area penalty and with a power saving.

1. Introduction

Image sensors are widely used in spacecraft for many applications [1] [2]. Photonic imager technology has been developed for wavelength responses that range from ultraviolet, through visible, to infrared. Most radiation effects studies have been made on infrared detectors, and visible/near infrared technologies such as charge coupled device (CCD), charge injection devices (CID) and active pixel sensors (APS). Among many optical applications, like earth or space observation, the guidance system in a spacecraft (launcher or satellite) is particularly critical. Then, the reliability of such guidance systems based on image sensors is essential for the space mission.

CMOS (Complementary Metal Oxide Semiconductor) technology is mainly used in the readout circuit of photonic integrated circuits (ICs). However, CMOS technology is known to be sensitive to single event effects (SEE), such as single event transient (SET) [2]. SETs can be induced by various ionizing particles, i.e., heavy ions, protons, electrons the space radiation environment [3]. SETs can become critical for image devices and ICs boarded in flight because of their critical applications. Actually, SETs in D Flip-Flop can change the logic state and disturb the nominal behavior of the readout circuit.

One of the interests of prediction tools, such as MUSCA SEP3 (MUTi-SCAle Single Event Phenomena Prediction Platform) [4-5], is to anticipate the sensitivity trends with the aim to help the designers to select the best layout considering of performances and reliability. Moreover, these investigations lead to reduce the number of testing runs during the qualifications of electronics under high energy particles such as heavy ions.

In this work is presented the interest of such approach to understand the failure origins at transistor level with the aim to be able to harden circuits of the readout system of photonic device. This work is focus on infrared (IR) device, designed by Sofradir. Therefore, specificity of cryogenic temperatures, down to 77 K, are considered. These temperatures are used with the aim to reduce the dark current and to increase in performances of the device.

2. SEE prediction tool

MUSCA SEP3 is a SEE prediction tool based on a Monte-Carlo approach which allows a complete simulation from the interaction of the radiation particles with the matter to the occurrence of the soft error in the IC [4-5] as shown in Fig. 1. These simulations use nuclear database (GEANT-4) in order to describe in 3D the interactions (nuclear and Colombian) of radiation particle, such as, heavy ions, protons, neutrons, or muons, with the material of the Back-End Of Line (BEOL). The modeling of transport and collection mechanisms is based on dynamic ambipolar diffusion, multi-collection, bipolar amplification. Details of the analytical modeling of transport and collection mechanisms are presented in details in previous works [6] [7]. The effect of bias voltage, the layout, and the fabrication processes are taken into account with the aim to build a realistic SET database. The modeling of the Front-End Of Line (FEOL) is based on the description (dimensions and locations) of implants, i.e., drain and source of each n-MOS and p-MOS transistor directly extracted from GDS files. The process of the extraction of collection areas from the layout file has been presented in previous work [8]. All required layout files and electrical models were provided by Sofradir. Next this SET database is injected on each node at transistor level for an electrical simulation with Spectre simulator with the aim to estimate the soft error response of the circuit. The electrical transient simulations of the parasitic circuit were performed by the Spice simulations [9]. The schematic of the cells and the model cards of n-MOS and p-MOS transistors are provided by Sofradir.

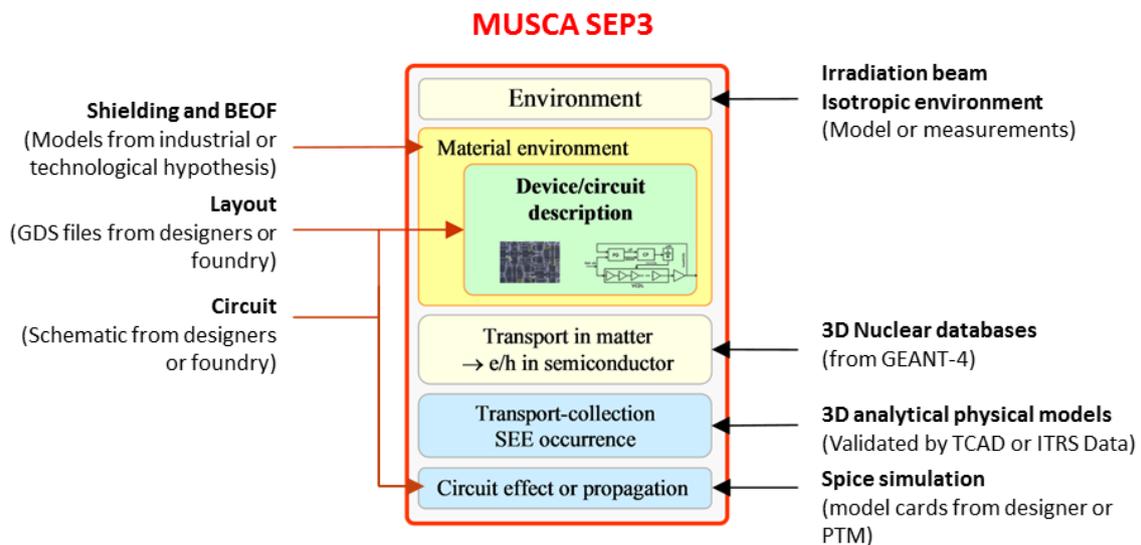


Fig.1 Simulation flow of the SEE prediction tool, MUSCA SEP3

An upset event was considered during the electrical simulation if the output signal Q changed of logic state (“1” to “0” or “0” to “1”). Chronograms of input, output and clock signals illustrate the SEU detection based on the electrical simulations, as shown in Fig. 2. Fig. 2 (a) presents the nominal behavior of the DFF cell synchronized by the clock signal (i.e. Clk) of 20 MHz. On the other hand, Fig. 2 (b) reveals a SEU occurrence on the output signal (Q) induced by an incident heavy ion on the DFF cell. The output signal decreases from 5V (state “1”) down to 0V (state “0”) until the next rising edge of the clock signal.

Based on this simulation framework, MUSCA SEP3 is able to propose an estimation of the

SEU sensitivity (SEU cross section, but also event mapping) of the DFF cells designed by Sofradir.

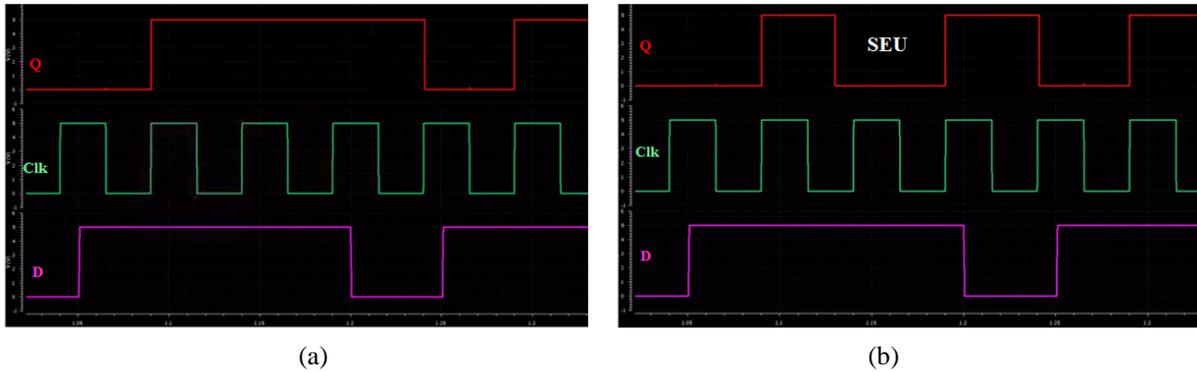


Fig.2 Chronograms of input, D (in pink), output Q (in red), and clock Clk (in green) signal of the DFF in (a) nominal behaviour and (b) impacted by a SEU.

The comparisons of experimental data and MUSCA SEP3 calculations at 300 K have been performed for 2 designs of DFF used in the readout circuit. Good correlations in terms of LET threshold and SEE saturation of cross section are proposed, as presented in Fig. 3 and Fig. 4 for the two design of DFF respectively. Error bars represent the standard deviation.

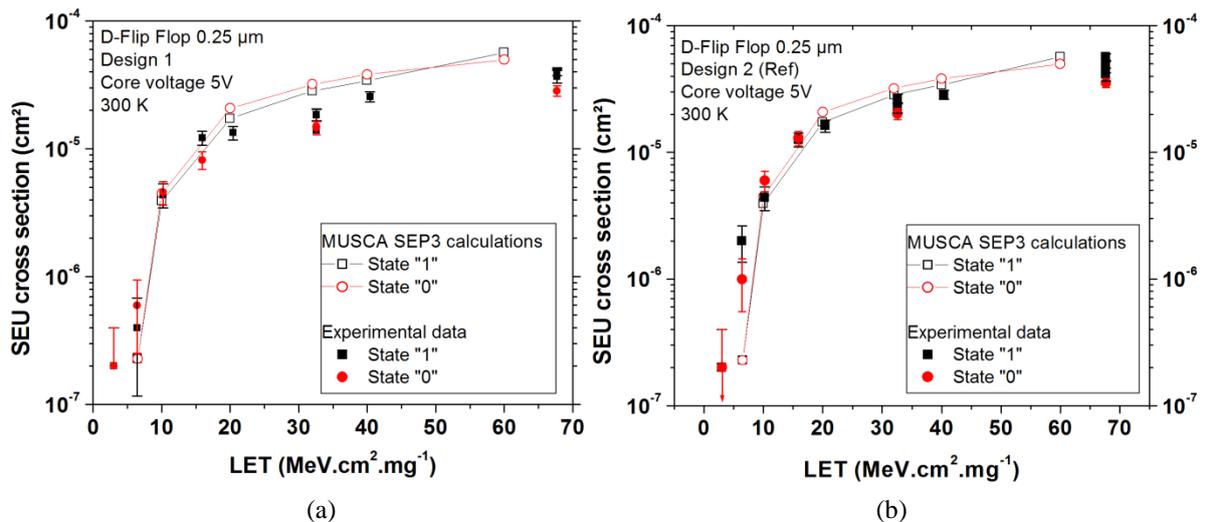


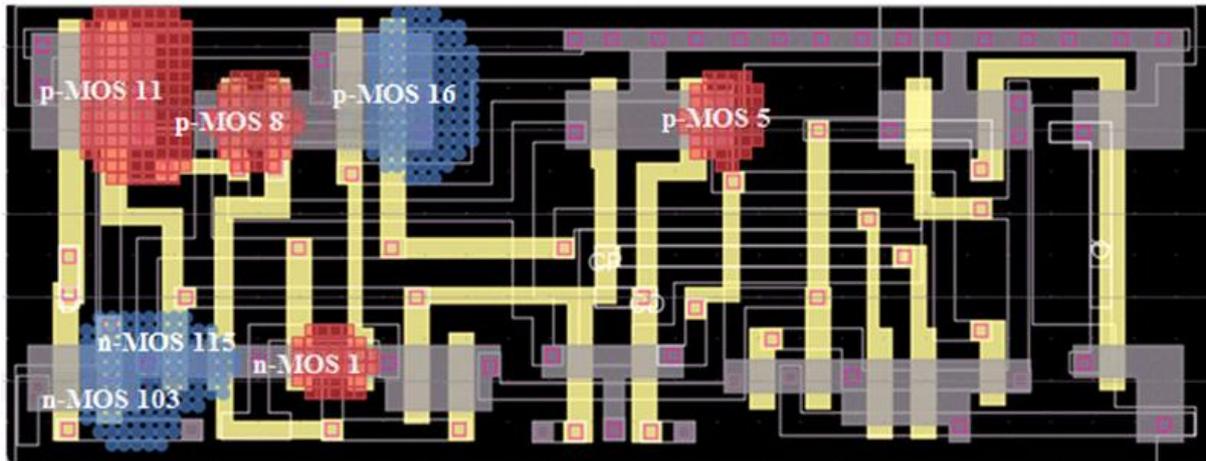
Fig. 4: Comparison of experimental data with MUSCA SEP3 simulations of the SEU cross section of DFF for the design 1 (a) and design 2(b), as a function of logic state, under heavy ion irradiation at UCL facility at 300 K.

After this presentation of the relevance of the prediction tool, the next section will show the failure analysis performed on the DFF cells. Actually, the other main interest of prediction tools is to allow a failure analysis at layout level with the aim to identify critical areas of the circuit.

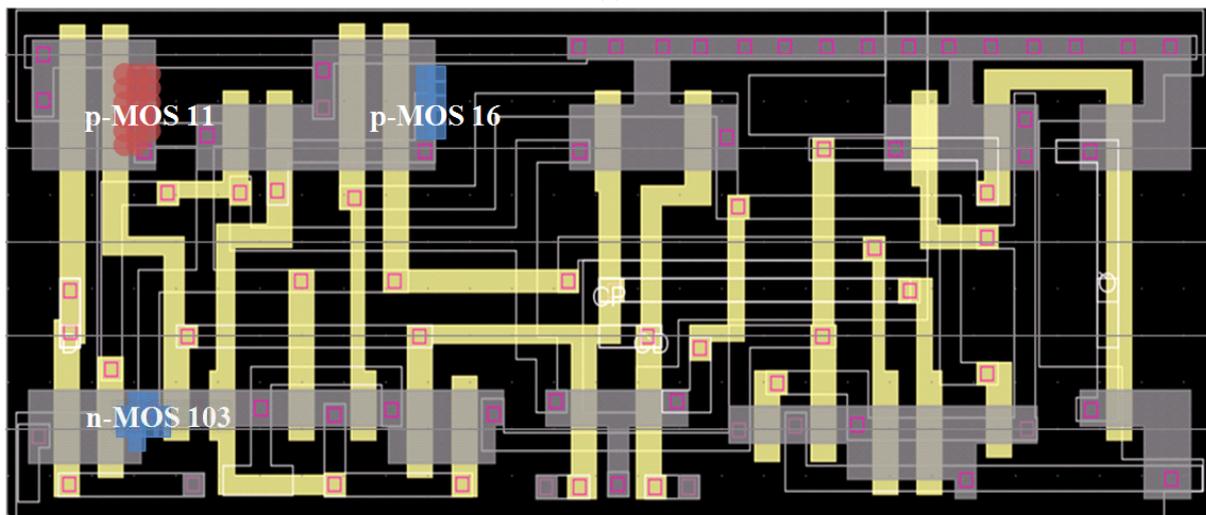
3. Failure analysis

These failure analyses based on sensitivity mappings can be really useful for designers in order to determine which transistors of the cell are critical and to anticipate design optimizations. But, the kind of analysis can be also interesting to improve test plan of

irradiation campaign in order to reduce the cost of space qualification of embedded devices. In previous works, MUSCA SEP3 had already shown the relevance of the estimated critical areas of SEU [10] but also for SEL (Single Event latchup) [11]. In this work, the simulation results highlight that the transistors of the input of the cell are more sensitive than the transistor of the output of the flip-flop cell. It is interesting to note that even if the global SEE cross section is quite equivalent for the two bias condition of the circuit, i.e., state “1” and state “0” saved in the DFF, the locations of critical areas are strongly different.



(a)



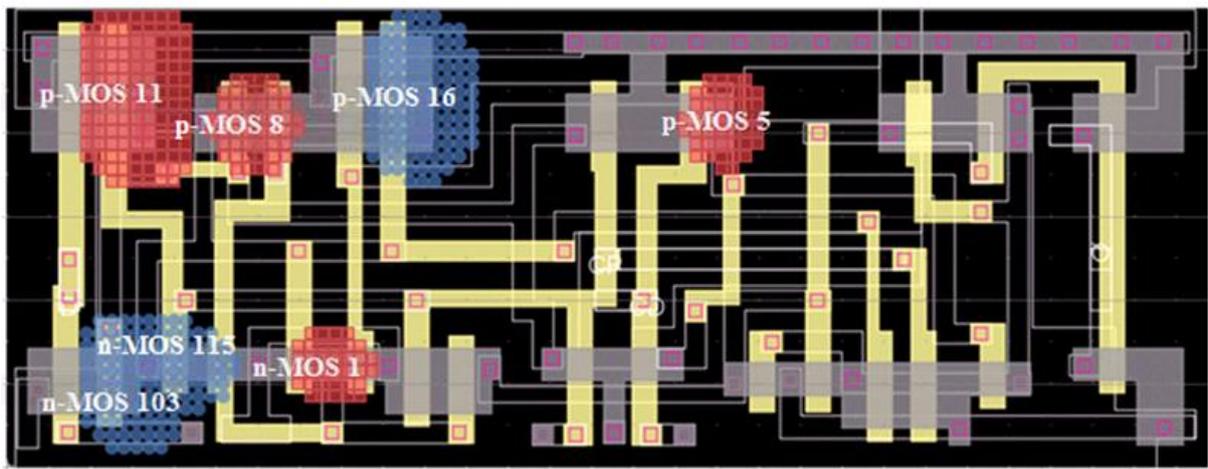
(b)

Fig. 5: SEU sensitivity mappings obtained by MUSCA SEP3 calculations for an ion with a LET of 58 $\text{MeV}\cdot\text{cm}^2\cdot\text{mg}^{-1}$ (a) as a function of stored data: “1” (red squares) “0” (blue dots) at 300 K (a) and (b) for a LET of 10 $\text{MeV}\cdot\text{cm}^2\cdot\text{mg}^{-1}$.

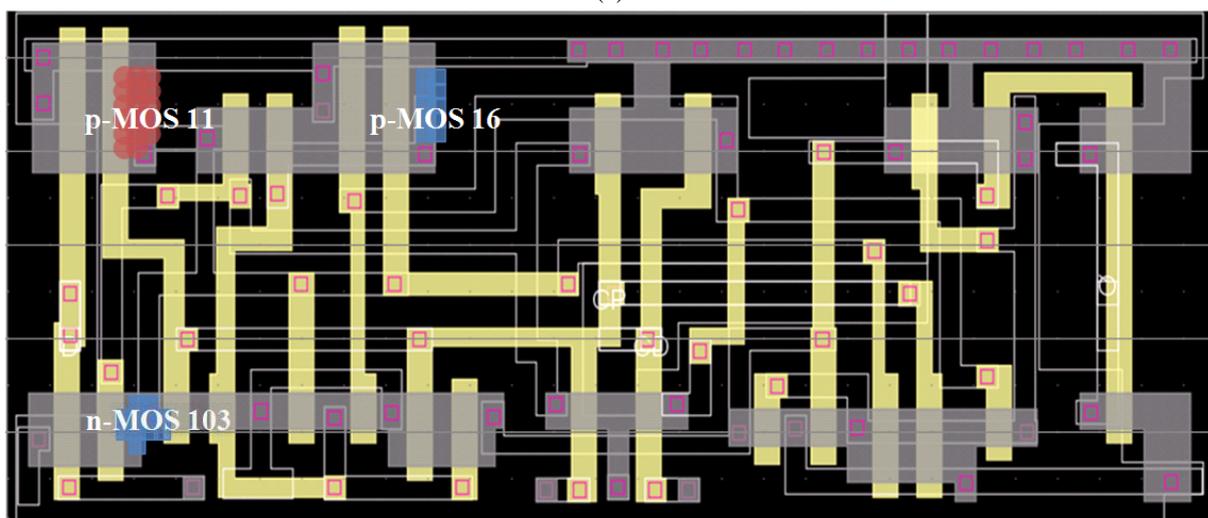
The analysis of this failure mapping at transistor level combined with the monitoring of SET on different internal nodes of the DFF cell allows for proposing design optimization. This optimization of the design cell is focus on the wider sensitive transistors, i.e., p-MOS 11 p-MOS 16, n-MOS 103, and the physical associated transistors. The initial cell area is kept, while the width of 6 transistors (4 p-MOS and 2 n-MOS) is decreased. This optimization allows for reducing the global power consumption of the DFF cell. Actually a decrease in width of this transistor induces a decrease in the drive current and so a decrease in the power consumption of the DFF cell during the transient states.

Fig. 6 presents the SEU sensitivity mapping of the optimized DFF obtained by MUSCA SEP3

calculations for an ion with a LET of $58 \text{ MeV}\cdot\text{cm}^2\cdot\text{mg}^{-1}$ (a) as a function of stored data: “1” (red squares) “0” (blue dots) at 300 K (a) and (b) for a LET of $10 \text{ MeV}\cdot\text{cm}^2\cdot\text{mg}^{-1}$.



(a)



(b)

Fig. 6: SEU sensitivity mappings of the optimized DFF obtained by MUSCA SEP3 calculations for an ion with a LET of $58 \text{ MeV}\cdot\text{cm}^2\cdot\text{mg}^{-1}$ (a) as a function of stored data: “1” (red squares) “0” (blue dots) at 300 K (a) and (b)

for a LET of $10\text{MeV}\cdot\text{cm}^2\cdot\text{mg}^{-1}$.

4. Conclusion and perspectives

This work presents an SEE prediction tool and its interest in failure investigations and in providing a help for designers with the aim to optimize the SEE sensitivity of Sofradir readout circuit. Estimations and a failure analysis at circuit level were presented considering the stored data configuration. Comparisons between predictions and experimental data obtained under heavy ion are consistent. In the final paper, complementary analyses and hardening techniques will be presented

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