



HAL
open science

System-Level Optimization of a DAC for Hearing-Aid Audio Class D Output Stage

Peter Pracný, Ivan H. Jørgensen, Erik Bruun

► **To cite this version:**

Peter Pracný, Ivan H. Jørgensen, Erik Bruun. System-Level Optimization of a DAC for Hearing-Aid Audio Class D Output Stage. 4th Doctoral Conference on Computing, Electrical and Industrial Systems (DoCEIS), Apr 2013, Costa de Caparica, Portugal. pp.647-654, 10.1007/978-3-642-37291-9_70 . hal-01348812

HAL Id: hal-01348812

<https://hal.science/hal-01348812v1>

Submitted on 25 Jul 2016

HAL is a multi-disciplinary open access archive for the deposit and dissemination of scientific research documents, whether they are published or not. The documents may come from teaching and research institutions in France or abroad, or from public or private research centers.

L'archive ouverte pluridisciplinaire **HAL**, est destinée au dépôt et à la diffusion de documents scientifiques de niveau recherche, publiés ou non, émanant des établissements d'enseignement et de recherche français ou étrangers, des laboratoires publics ou privés.



Distributed under a Creative Commons Attribution 4.0 International License

System-level Optimization of a DAC for Hearing-aid Audio Class D Output Stage

Peter Pracný, Ivan H. H. Jørgensen, Erik Bruun,

Department of Electrical Engineering, Technical University of Denmark,
2800 Kgs. Lyngby, Denmark, pp@elektro.dtu.dk

Abstract. This paper deals with system-level optimization of a digital-to-analog converter (DAC) for hearing-aid audio Class D output stage. We discuss the $\Sigma\Delta$ modulator system-level design parameters – the order, the oversampling ratio (OSR) and the number of bits in the quantizer. We show that combining a reduction of the OSR with an increase of the order results in considerable power savings while the audio quality is kept. For further savings in the $\Sigma\Delta$ modulator, overdesign and subsequent coarse coefficient quantization are used. A figure of merit (FOM) is introduced to confirm this optimization approach by comparing two $\Sigma\Delta$ modulator designs. The proposed optimization has impact on the whole hearing-aid audio back-end system including less hardware in the interpolation filter and half the switching rate in the digital-pulse-width-modulation (DPWM) block and Class D output stage.

Keywords: Sigma-Delta Modulator; Digital-to-Analog Converter; Interpolation Filter; Class D; Hearing Aid; Low Voltage, Low Power

1 Introduction

The hearing-aids of today are devices where strict specifications are applied. High audio quality and the need for longer operation time combined with the desire to shrink the size of the hearing-aid devices to make it virtually invisible leaves less space for the battery and integrated circuits. These demands contradict each another, making the current consumption of the electronics inside the hearing-aid one of the crucial parameters for the design. To find the optimum balance between the design parameters in every part of a hearing-aid device is therefore of vital importance. This includes the back-end of the audio signal processing path (see Fig.1). As part of the digital-to-analog conversion a digital $\Sigma\Delta$ modulator is usually used in audio applications. Due to the oversampling nature of the $\Sigma\Delta$ modulator an interpolation filter is needed prior to the modulator. In the case of a multi-bit $\Sigma\Delta$ modulator, to be able to connect the output of the $\Sigma\Delta$ modulator to the input of the Class D output-stage a DPWM block that turns the $\Sigma\Delta$ signal into pulse width modulation, is needed. The Class D output stage is usually implemented as an H-bridge (schematic in Fig.1 is simplified). This paper deals with optimization of such a back-end system resulting in considerable power savings compared to the design of [1]. In Section 2, design specifications for the $\Sigma\Delta$ modulator intended for hearing-aid application are

discussed. A figure of merit (FOM) that allows relative comparison of $\Sigma\Delta$ modulators and estimation of power savings is introduced here too. In Section 3, optimization approach is proposed. In Section 4 two $\Sigma\Delta$ modulator designs are compared as an example of the optimization approach. Finally, the conclusions can be found in Section 5.

2 Contribution to Internet of Things

In the future the Internet will become even more important part of our daily life. Multimedia information will be delivered to our portable electronic devices. This will require audio readout “on the fly” of the internet content, low power digital signal processing and amplification inside an ear-plug. In this work we propose how such signal processing can be done in a more power efficient way.

3 Design Specifications and Figure of Merit

A thorough discussion on hearing-aid audio back-end system specification and the $\Sigma\Delta$ modulator is provided in [1]. The band-width (BW) of high-end hearing aids is a trade-off between ensuring sufficient sound quality and the limited power available and is normally around 10 kHz. In order to fulfill the Nyquist criterion the sampling frequency at the input of the back-end system is $f_{s,in} > (2 * BW) = 20$ kHz. In the case of this work we use $44.1 \text{ kHz} / 2 = 22.05 \text{ kHz}$ [1]. Also in this work we assume ideal 16 bit quantization of the back-end system input signal [2]. This results in signal-to-quantization-noise ratio (SQNR) = 98 dB. The input signal of the back-end is then up-sampled using an interpolation filter [2] and passed to the $\Sigma\Delta$ modulator. The interpolation filter in [2] consists of 4 stages (FIR filter, half-band filter, 1st order Sinc filter, 3rd order Sinc filter) and is used to up-sample the input signal 64 times. Another requirement in this work is the signal-to-noise-and-distortion ratio (SNDR) at the total output of the back-end of 90 dB. The interpolation filter and the $\Sigma\Delta$ modulator are designed to keep the quality of the audio signal at SNDR = 98 dB so that a margin of 8 dB is left for the performance reduction introduced by the output stage. Note that we are dealing with a digital $\Sigma\Delta$ modulator in this work and we treat it as a digital filter. This allows us to adopt the idea for a FOM from [3, 4] by counting the number of adders in the design. Unlike in the case of the interpolation filter the number of bits does not have to be the same for all the adders in a $\Sigma\Delta$ modulator. We have to take this fact into account and propose FOM so that the number of bits of individual adders is included. This leads us to

$$FOM = \sum_i b_i \cdot OSR_i . \quad (1)$$

Where i is the number of adders in the $\Sigma\Delta$ modulator block, b_i is the number of bits used in individual adders and OSR_i is the oversampling used for the individual adders. In the case of the $\Sigma\Delta$ modulator block OSR_i is the same for all the adders. Since this FOM accounts for the majority of the cells needed to implement the $\Sigma\Delta$ modulator it is roughly proportional to the power of the $\Sigma\Delta$ modulator and is a valuable tool when

choosing between designs in early design phase. The lower the FOM the better the design is. The above mentioned specifications and FOM will be used in the next sections when optimizing the back-end system including the $\Sigma\Delta$ modulator and comparing it to previous design of [1].

4 Design Optimization Approach

The idea behind the optimization of the $\Sigma\Delta$ modulator and the entire back-end design compared to [1] is to decrease the OSR of the modulator from 64 to 32 and increase its order from 3 to 6. By performing these changes in the $\Sigma\Delta$ modulator we aim to reduce the switching frequency of the Class D output stage and the DPWM block by 50% as this frequency is the same as the operating frequency of the $\Sigma\Delta$ modulator. With the Class D output stage being the main power consumer in the back-end system due to the large output transistors and low output impedance, this will result in considerable power savings. Moreover these changes will have positive impact on the interpolation filter too as oversampling by 32 only is needed compared to oversampling by 64 in [1]. This saves one stage performing oversampling by a factor of 2 in the interpolation filter of [2]. Using the same idea as in Eq.(1) for the FOM of the interpolation filter we calculate FOM = 113 for the whole interpolation filter out of which FOM = 24 goes for the stage that will be saved by our optimization. This is improvement of hardware/power saving by 21% in the interpolation filter.

With a signal with SQNR = 98 dB at the $\Sigma\Delta$ modulator input any oversampling (OSR) and noise-shaping order in the $\Sigma\Delta$ modulator providing better SQNR than 98 dB is denoted in this work as overdesign. However, just like in the case of FIR filters in [5], overdesign can allow very coarse quantization of the $\Sigma\Delta$ modulator coefficients leading to lower amount of adders used and thus reducing the power consumption. Keeping this in mind we compare two cascade-of-resonator-with-feedback (CRFB) $\Sigma\Delta$ modulator designs with the same performance. We chose the designs so that the same peak-SQNR is achieved in both cases. To ensure a simple interpolation filter, only factors of integer power of two are considered in this work. In Fig.2 peak-SQNR is plotted as a function of OSR for orders $N = 1$ to 8 when 3 bit quantizer is used. This figure shows that the following parameter combinations achieve peak-SQNR of approx. 106 dB: OSR = 64, order = 3, 3 bit quantizer (see [1]), OSR = 32, order = 6, 3 bit quantizer (optimized). With SQNR = 98 dB needed at the $\Sigma\Delta$ modulator output we leave margin for coarse coefficient quantization (as proposed in [5] for digital FIR filters) and we overdesign the $\Sigma\Delta$ modulator to reach 106 dB peak-SQNR. Again, for the sake of comparison both of these designs use 3 bit quantizer. As explained in [1], the number of bits used in the quantizer is one of the factors that decide the clock frequency of the DPWM block. Increasing the number of bits in the quantizer can result in clock frequency that is not available in hearing aids. For this reason we keep the number of bits in the quantizer the same as in [1] and limit the design freedom in this case to OSR and the order of the $\Sigma\Delta$ modulator. Moreover the maximum stable amplitude at the modulator input is the same in both cases, -1 dBFS. The noise-transfer-functions (NTF) of both $\Sigma\Delta$ modulators can be seen in Fig. 3. Having the

same performance in both designs allows us to compare these designs using the FOM of Eq. (1). The only block of the back-end system that remains to be investigated to see whether or not this optimization approach is reasonable is the $\Sigma\Delta$ modulator. We discuss this in the next section.

5 $\Sigma\Delta$ Modulator Optimization

The two $\Sigma\Delta$ modulator structures we used in this work can be seen in Fig. 4. A 3 bit quantizer is used in both cases, the order of the modulator was increased from 3 (Fig. 4a) to 6 (Fig. 4b) and the OSR was decreased from 64 to 32. The $\Sigma\Delta$ modulator performance is the same in both cases. For both designs a model using floating-point arithmetic and a model using fixed-point arithmetic was built and simulated in Matlab. The fixed-point arithmetic model performs digital operations exactly as a VHDL design does. Thus the fixed-point arithmetic model can be directly used to judge the complexity of the filter. The FOM used in this work depends on the number of the adders and the number of bits used in the individual adders. This means that one way to improve the FOM in the 6th order modulator is to keep the number of adders as low as possible. For this reason in this work, we adopt the FIR filter over-design approach from [5] and use it for the $\Sigma\Delta$ modulator designs. Peak-SQNR of 98 dB needed at the modulator output allows us to use the 8 dB margin achieved by the modulator being overdesigned to reach approx. peak-SQNR of 106 dB to coarsely quantize the coefficients. Using coarse quantization of the coefficients reduces the peak-SQNR from approx. 106 dB to 98 dB – still within specification with lower number of adders used than in direct design. To confirm our optimization approach, we design both $\Sigma\Delta$ modulators in two versions: Version 1: with high-precision coefficients and adders to achieve peak-SQNR = approx. 106 dB (see Fig. 4). Version 2: with coarsely quantized coefficients and adders to allow peak-SQNR = 98 dB (see Fig. 4). The list of coefficients used for the 3rd order modulator can be seen in Tab. 1 and the list of coefficients for the 6th order modulator in Tab. 2. The number of bits used for the internal integrators can be seen in Fig. 4 for both Version 1 and Version 2. Taking the Matlab fixed-point models and calculating the FOM according to Eq. 1 gives data and FOM in Tab. 3, clearly showing that the FOM of the 6th the order modulator with OSR = 32 compared to 3rd order modulator with OSR = 64 of [1] remains approximately the same after the back-end system optimization in both high-precision and coarsely quantized case. This can be predicted by looking at Fig. 4. The OSR of the 6th order modulator in Fig. 4a is half compared to the 3rd order modulator in Fig. 4b but the area is doubled. To have lower power consumption in the Class-D output stage and have larger area of the $\Sigma\Delta$ modulator is reasonable tradeoff since the $\Sigma\Delta$ modulator is completely digital and thus easily scales with technology. The same cannot be said about the Class-D output stage. Expressing the current consumption of the back-end as sum of the currents needed in individual blocks we write

$$I_{total} = I_{int} + I_{SDM} + I_{DPWM} + I_{dr} \quad (2)$$

Where I_{int} is the current needed in the interpolation filter (see Fig. 1), I_{SDM} is the current of the $\Sigma\Delta$ modulator, I_{DPWM} is the current of the DPWM block and I_{dr} is the current of the Class-D driver (output-stage). In Section 3 We explained that I_{dr} and I_{DPWM} will be lowered by 50% and I_{int} by 21% by the optimization. Table 3 shows that I_{SDM} will remain approximately the same. Thus in total there are considerable power savings achieved by the proposed optimization approach. In future work, the OSR in the 6th order modulator being halved compared to [1] will allow us to increase the number of bits in the quantizer from 3 to 4 while keeping the maximum sampling frequency in the system. This will help to increase the maximum stable amplitude of the $\Sigma\Delta$ modulator – a crucial parameter in hearing-aid application.

6 Conclusion

In this paper we optimized the back-end of the audio signal processing path in hearing-aid application on system-level compared to the design of [1]. A figure of merit was introduced to decide early in the design process whether or not the optimization approach is reasonable. The optimization approach uses combination of the increase of the $\Sigma\Delta$ modulator order and the decrease of its OSR. Further savings are achieved by peak-SQNR overdesign and subsequent coarse quantization of the $\Sigma\Delta$ modulator coefficients. This approach leads to simplified interpolation filter, reduces the frequency of the DPWM block and the switching-rate of the Class-D output stage by 50%. The power consumption of the $\Sigma\Delta$ modulator is kept as in [1]. Overall the power of the entire back-end system is optimized showing that trading higher order for lower OSR in the $\Sigma\Delta$ modulator DAC is an approach to be considered in low-voltage, low-power, portable audio applications.

Table 1. 3rd order $\Sigma\Delta$ modulator coefficient list.

<i>Quantization</i>		<i>Version 1</i>		<i>Version 2</i>	
<i>Coeff.</i>	<i>Value</i>	<i>Shift/Add</i>	<i>Adders</i>	<i>Shift/Add</i>	<i>Adders</i>
a ₁	1/8	2 ⁻³	0	2 ⁻³	0
a ₂	0.3446	2 ⁻² +2 ⁻⁴ +2 ⁻⁵	2	2 ⁻²	0
a ₃	0.3941	2 ⁻² +2 ⁻³ +2 ⁻⁶	2	2 ⁻² +2 ⁻³	1
b ₁	1/8	2 ⁻³	0	2 ⁻³	0
c ₁	1/2	2 ⁻¹	0	2 ⁻¹	0
c ₂	1/2	2 ⁻¹	0	2 ⁻¹	0
c ₃	1.4063	2 ⁰ +2 ⁻² +2 ⁻³ +2 ⁻⁵	3	2 ⁰ +2 ⁻²	1
g ₁	0.0029	2 ⁻⁹ +2 ⁻¹⁰	1	2 ⁻⁹	0

Table 2. 6th order $\Sigma\Delta$ modulator coefficient list.

<i>Quantization</i>		<i>Version 1</i>		<i>Version 2</i>	
<i>Coeff.</i>	<i>Value</i>	<i>Shift/Add</i>	<i>Adders</i>	<i>Shift/Add</i>	<i>Adders</i>
a ₁	1/16	2 ⁻⁴	0	2 ⁻⁴	0
a ₂	0.1542	2 ⁻³ +2 ⁻⁶ +2 ⁻⁷	2	2 ⁻³	0
a ₃	0.1705	2 ⁻³ +2 ⁻⁵ +2 ⁻⁷	2	2 ⁻³ +2 ⁻⁵	1
a ₄	0.2532	2 ⁻²	0	2 ⁻²	0
a ₅	0.5544	2 ⁻¹ +2 ⁻⁵ +2 ⁻⁷	2	2 ⁻¹ +2 ⁻⁵	1
a ₆	0.6353	2 ⁻¹ +2 ⁻³	1	2 ⁻¹ +2 ⁻³	1
b ₁	1/16	2 ⁻⁴	0	2 ⁻⁴	0
c ₁	1/8	2 ⁻³	0	2 ⁻³	0
c ₂	1/8	2 ⁻³	0	2 ⁻³	0
c ₃	1/4	2 ⁻²	0	2 ⁻²	0
c ₄	1/2	2 ⁻¹	0	2 ⁻¹	0
c ₅	1/2	2 ⁻¹	0	2 ⁻¹	0
c ₆	0.8791	2 ⁰ -2 ⁻³	1	2 ⁰ -2 ⁻³	1
g ₁	0.0044	2 ⁻⁸ +2 ⁻¹²	1	2 ⁻⁸	0
g ₂	0.0168	2 ⁻⁶ +2 ⁻¹⁰	1	2 ⁻⁶	0
g ₃	0.0167	2 ⁻⁶ +2 ⁻¹⁰	1	2 ⁻⁶	0

Table 3. Modulator comparison.

<i>Modulator Order</i>	<i>Quant. bits</i>	<i>OSR</i>	<i>Adders</i>	<i>Peak-SQNR [dB]</i>		<i>FOM</i>
				<i>ideal</i>	<i>quantized</i>	
3	3	64	18	106	106 (Version 1)	296
6	3	32	29	105	105 (Version 1)	303
3	3	64	12	106	98 (Version 2)	193
6	3	32	22	105	98 (Version 2)	192

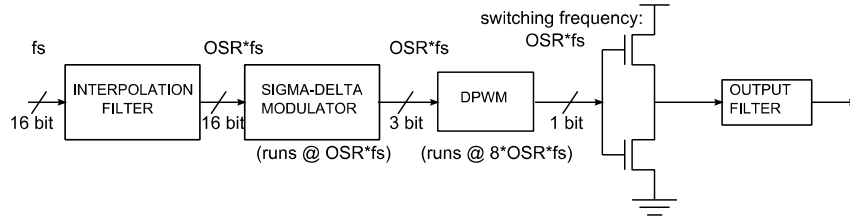


Fig. 1. Simplified schematic of the back-end of audio signal processing chain: interpolation filter, $\Sigma\Delta$ modulator, Class-D output-stage and output filter.

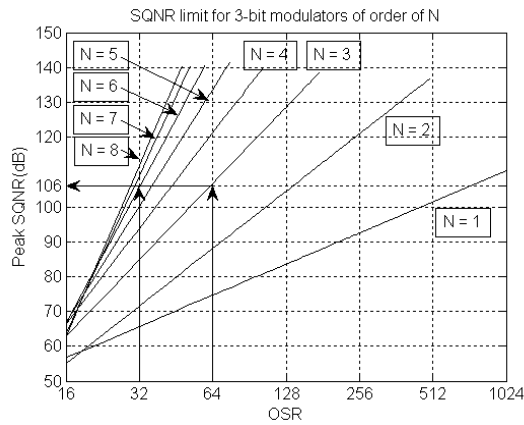


Fig. 2. Peak SQNR versus OSR for $\Sigma\Delta$ modulator orders $N = 1$ to 8 with 3 bit quantizer.

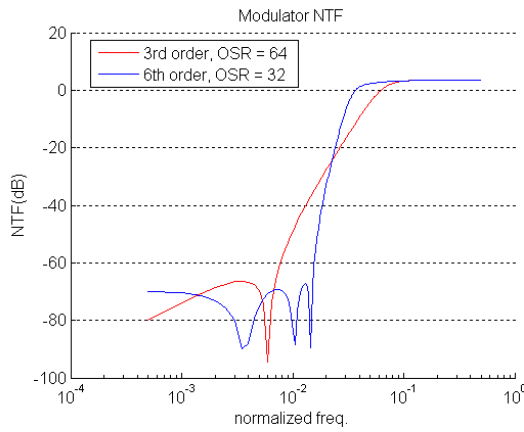


Fig. 3. $\Sigma\Delta$ modulator NTF in the case of (red) 3rd order modulator (frequency is normalized to $64 \times f_{\text{sin}}$) and (blue) 6th order modulator (frequency is normalized to $32 \times f_{\text{sin}}$)

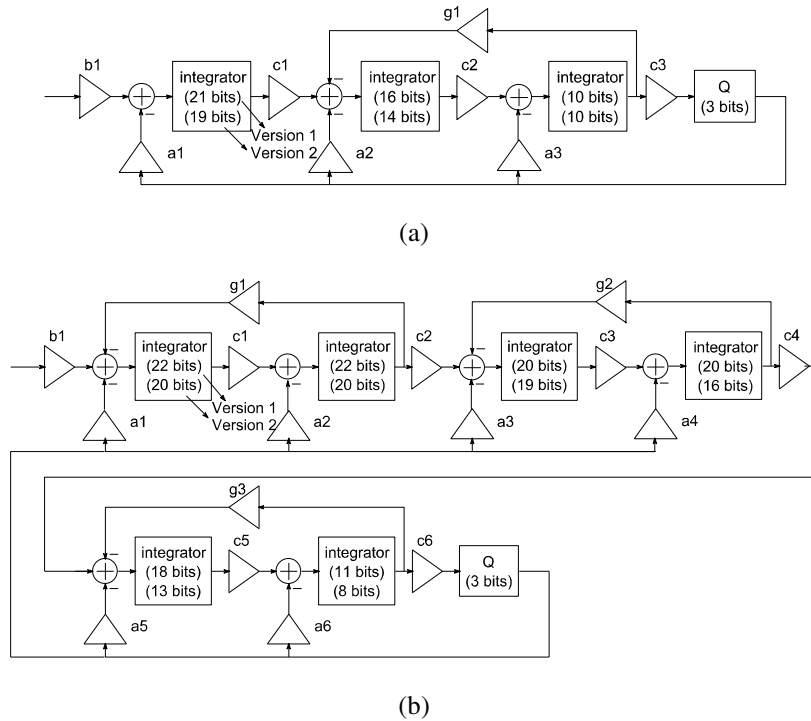


Fig. 4. Simplified $\Sigma\Delta$ modulator CRFB schematic (a) 3rd order modulator, OSR = 64 and (b) 6th order modulator, OSR = 32.

References

1. P. Pracný, E. Bruun, "ΣΔ Modulator System-Level Considerations for Hearing-Aid Audio Class-D Output Stage Application," Proc. 2012 8th Conf. on Ph.D. Research in Microelectronics and Electronics (PRIME), pp. 103-106, Aachen, June 2012.
2. Pracný P., Llimós M. P., Bruun E. : 'Interpolation filter design for hearing-aid audio class-D output stage application', Proc. 19th IEEE Int. Conf. on Electronics, Circuits, and Systems, Seville, Spain, Dec. 2012.
3. Anzova V. I., Yli-Kaakinen J., and Saramäki, T. : 'An algorithm for the design of multiplierless IIR filters as a parallel connection of two all-pass filters', Proc. IEEE Asia Pacific Conf. on Circuits and Systems, Singapore, Dec. 2006, pp. 744-747.
4. Stoyanov G., Nikolova Z., Ivanova K., Anzova V. : 'Design and realization of efficient IIR digital filter structures based on sensitivity minimizations', Proc. 8th Int. Conf. on Telecommunications in Modern Satellite, Cable and Broadcasting Services, Niš, Serbia, Sep. 2007, pp. 299-308.
5. Mehboob R., Khan S. A., Qamar R. : 'FIR filter design methodology for hardware optimized implementation', IEEE Trans. Consumer Electronics, 2009, 55, (3), pp. 1669-1673.