Comparison of Feedback Influence on Ring Oscillator Performance for IR-UWB Pulse Generator in 0.13 μm and 0.18 μm CMOS Technologies

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Abstract. A CMOS three-stage ring oscillator is examined in UMC 0.13 µm and 0.18 µm technologies. The influence of PMOS transistor and resistor, as inverter feedbacks, on the ring oscillator frequency and the peak-to-peak amplitude is investigated in both technologies. Furthermore, as the ring oscillator usually drives a buffer in pulse generator/transmitter chain, dependence of its Figures of Merit on the buffer feedback is presented in the paper. Simulation results showed that the ring oscillator frequency is strongly dependent on the inverter feedback. The presented techniques can be used to increase (resistive feedback) and control (PMOS transistor feedback) the ring oscillator frequency. As the ring oscillator is a part of an IR-UWB (Impulse Radio Ultra Wide Band) pulse generator, its oscillating frequency determines the spectrum central frequency and has significant effect on spectrum fitting within UWB FCC mask.

Keywords: CMOS process, impulse radio ultra wideband, PMOS transistor feedback, pulse generator, resistive feedback, ring oscillator.

1 Introduction

Since the Federal Communications Commission (FCC) allocated the 3.1 – 10.6 GHz unlicensed spectrum for commercial ultra wideband (UWB) application in February 2002[1], several technologies have been developed to satisfy the communication market requirements such as Multi-Band Orthogonal Frequency Division Multiplexing (MB-OFDM), Direct Sequence (DS)and Impulse Radio (IR) [2 – 5]. As a carrier-less approach which makes use of ultra-short duration pulses (pulse duration is less than 1 ns) that can yield ultra-wide bandwidth signals, IR-UWB technology stands out from the rest by providing very simple (without mixer and power amplifier), low-cost and low-power UWB transmitter realizations [6]. Besides wide bandwidth, it offers a great resistance to multipath fading that usually plagues for narrow-band systems, and allows multiple access and robustness to interference [7]. Another advantage of the IR-UWB radios is high precision ranging [8], with a

potential for centimeter accuracy in indoor environments. Consequently, the approach appears to be good candidate for very high data rate short-range communications, low data rate communications related to localization or/and positioning systems, sensor networks, biomedical and many other cutting edge Internet of Things applications.

A pulse generator plays the core role in an UWB system as it produces pulse train which spectrum has to fully comply with and efficiently use the FCC mask. Therefore, it is extremely challenging to design UWB transmitter that satisfies such demanding requirements while achieving wide bandwidth, low-power, low cost and simple architecture. Besides, it is very desirable to provide pulse generator spectrum tuning to enable compensation due to process, voltage and temperature (PVT) variations, and antenna and communication channel performance changes.

As an essential part of analogue-digital pulse generator, a ring oscillator is investigated in this work. In addition to the standard switched three-stage ring oscillator, topologies with resistors and PMOS transistors, introduced as feedbacks in the ring oscillator inverters, are examined in 0.13 μm and 0.18 μm UMC CMOS technologies. A novel approach that uses the resistive feedback in the buffer stage to increase ring oscillator frequency without degrading its peak-to-peak amplitude is proposed. Influence of negative feedback on the ring oscillator performance and comparison of results obtained using considered processes are presented.

2 Relation to Internet of Things

After the computer in the 1940s and the Internet in the 1970s, the Internet of Things (IoT) represents the third revolution in information and communication technology (ICT). With main vision of "Everything connects", its development depends on dynamic technology evolutions in a set of multidisciplinary and interdisciplinary fields, ranging from the material and devices, sensor technology, to electronic system design and wireless communications. To fulfill the IoT demands, future micro-devices must provide a variety of advanced futures such as sensing, processing, communication, positioning, and capability to be integrated into everyday objects. To accomplish this, reliable-operating and maintenance-free wireless networks with low-power and low-cost radio transceivers are essential. Many advantages of the IR-UWB systems provide them leading role in wireless communications and sensor networks, and thus precedence in IoT applications. Wideband signals offer robust communications and high-precision positioning; duty-cycled operations allow link scalability and energy-efficient solutions; and baseband-like architecture facilitates extremely simple and low-power transmitters that can be integrated in various objects.

Thought it is not required, ability of UWB transmitter spectrum tuning represents very desirable quality that allows compensation for PVT variations and communication channel performance changes, and furthermore interference avoidance. Methods proposed in this work provide control and increase in the ring oscillator frequency. Since this parameter determines the center frequency of the ring oscillator-based pulse generator output spectrum, such ideas can be used to enable the IR-UWB transmitter spectrum adjustment.

3 Standard Three-stage Ring Oscillator Design

It is already mentioned that the pulse generator is one of the most important parts of the IR-UWB system. The oscillator-based transmitter that contains a switched ring oscillator represents the most commonly used topology, presented in Fig. 1 [9]. The glitch generator turns on/off the ring oscillator approximately defining duration of its oscillation and so the width of the transmitter output pulse. The pulse generator spectrum center frequency is determined by the ring oscillator frequency. The buffer stage isolates the switched oscillator from the output filter, and improves the UWB transmitter current driving capability. The pulse shaping, usually the band-pass filter additionally accommodates spectrum fitting within the FCC mask.

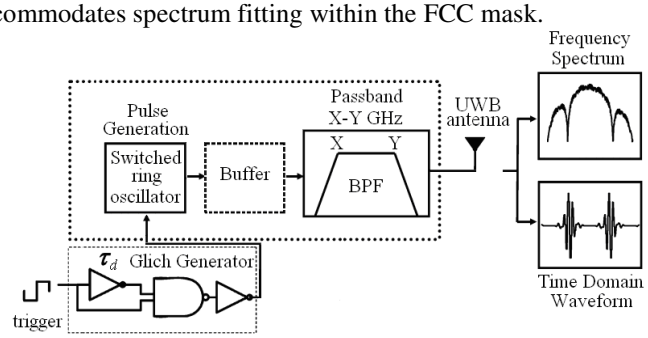

Fig. 1. An IR-UWB transmitter based on ring oscillator as a part of pulse generator.

The switched ring oscillator topology is shown in Fig. 2. It consists of the standard three-stage ring oscillator (inverter stages M_1–M_3) and oscillation-enabling switches (transistors M_4 and M_5). The ring oscillator is turned on by transistor M_4 at the *on-off* signal (produced by the glitch generator) rising edge. The inverter stages output voltage values are determined by the size ratio of the corresponding PMOS and NMOS transistors. During the *on-off* signal low level, the transistor M_4 is switched off, and no signal is generated at the oscillator output. Furthermore, transistor M_5 connects the M_1 transistor output (the M_2 transistor input) to V_{dd} providing the oscillation start from the same initial state at the rising edge the *on-off* signal.

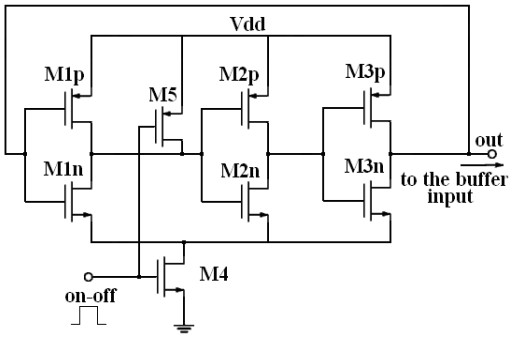

Fig. 2. The standard three-stage ring oscillator architecture.

4 Ring Oscillator in 0.13 μm and 0.18 μm CMOS Technologies

The proposed design has been simulated in mixed mode/RF 0.13 μm and 0.18 μm UMCCMOS technologies using Cadence's Spectre RF Simulator. Supply voltages V_{dd} of these technologies are 1.2 V and 1.8 V, respectively.

The ring oscillator working frequency depends directly on transistors sizes. The period of the oscillation T rises proportionally with increase in transistors sizes, while the oscillating frequency decreases (f_0=1/T). For the same NMOS and PMOS ring transistors size (channel width/length W/L=3.6 μm/0.12 μm) in 0.13 μm CMOS technology, the oscillation frequency of 7.65 GHz has been obtained. However, for the smallest NMOS transistors (W/L=25 μm/0.18 μm) and approximately two times larger PMOS transistors (W/L=45 μm/0.18 μm) in 0.18 μm CMOS technology, the f_0 parameter of 3.77 GHz has been achieved. It should be noted that in inverter topology PMOS transistor is usually equal or two times larger than NMOS transistor to compensate the difference in PMOS and NMOS carrier mobility and set V_{TH} closer to V_{dd}/2. Although former technology allows considerably higher ring oscillator frequency, 0.18 μm technology is much more cost effective [10], and attractive from the IC fabrication costs point of view. Nevertheless, obtained values are not high enough to utilize the UWB higher-band (6 – 10 GHz) more effectively (the center frequency of at least 8 GHz is required).

4.1 Influence of the Inverter Resistive Feedback

To increase the oscillation frequency at a given DC current, the resistive feedback is used in each inverter stage, as proposed in [9]. Resistors were connected between nodes A–A', B–B', and C–C', as shown in Fig. 3. Resistors R influence on the performance (the frequency f_0 and peak-to-peak amplitude V_{pp}) of the ring oscillator

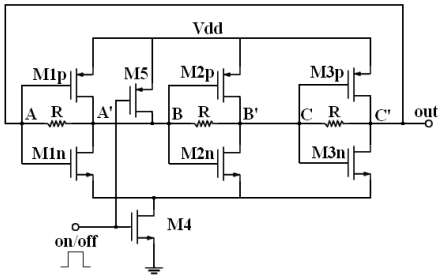

Fig. 3. Architecture of the ring oscillator with the resistive feedbacks.

Table 1. Ring oscillator performance dependence on the inverter feedback resistor value.

Tech.	0.13μm CMOS					0.18μm CMOS				
R (kΩ)	4	6	8	10	∞	0.5	1	2	4	∞
f_0 (GHz)	9.80	9.10	8.60	8.20	7.65	5.60	4.47	4.09	3.92	3.77
V_{pp} (V)	0.44	0.62	0.69	0.73	0.88	0.60	1.18	1.38	1.48	1.57

designs in used technologies is shown in Table 1. It can be noted that with decrease in the resistor value the oscillation frequency increases, but the peak-to-peak amplitude V_{pp} of the ring oscillator output signal is reduced, as expected. This behavior is caused by the reduction of the inverter closed loop gain with decrease in the feedback resistor value. Furthermore, the V_{pp} parameter and the time for reaching the peak signal values are reduced resulting in f_0 parameter increase. Moreover, it can be seen that the oscillation frequency was considerably increased in both technologies, while higher$f_0$valuesare obtained in the scaled UMC technology, as expected. But, the V_{pp} parameter values achieved for the lowest resistors values (4 kΩ in case of 0.13 μm, and 0.5 kΩ in 0.18 μm CMOS process)are not large enough to drive properly the subsequent stage (usually a buffer) in the pulse generator chain. This is the main reason why higher feedback resistor values are used in 0.13 μm CMOS architecture (otherwise V_{pp} values even lower than 440 mV would be obtained). On the other hand, if higher resistor values are used in0.18 μm technology (the same as in 0.13 μm) the ring oscillator frequency would not be increased comparing to the initial value of 3.77 GHz. Therefore, it should be emphasized that the resistor value needs to be selected considering the trade-off between the oscillation frequency and the required V_{pp} value.

Although the f_0 parameter can be significantly increased by proposed technique, this method does not allow the ring oscillator frequency to be tuned. It is already mentioned that even if it is not required in the IR-UWB technology, the ability of the frequency adjustment is very desirable advantage.

4.2 Influence of Inverter PMOS Transistor Feedback

To enable electrical tuning, the topology with PMOS transistors as inverter feedbacks has been proposed, Fig. 4.Influence of the PMOS gate control voltage V_{ctrl} on the performance of the ring oscillator architectures in 0.13 μm and 0.18 μm technologies is summarized in Table 2.

In addition to higher f_0 values, the 0.13 μm technology offers noticeably wider tuning range (3.15 GHz) compared to frequency range (1.46 GHz) available in 0.18 μm CMOS process. For V_{ctrl} parameter value equal to zero, the same situation as in the previous method can be noticed; the achieved V_{pp} values are below acceptable

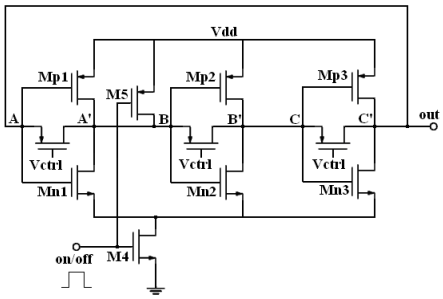

Fig. 4. Topology of the ring oscillator with PMOS transistor feedbacks.

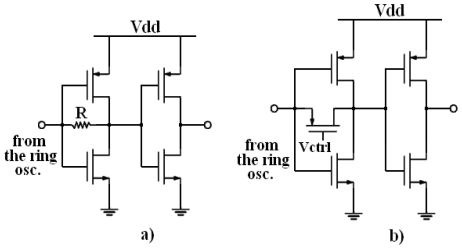

Fig. 5. Two-stage buffer with: (a) Resistive feedback (b) PMOS transistor feedback.

Table 2. Ring oscillator performance dependence on the gate control voltage of the PMOS transistor in the inverter feedback.

Tech.	0.13µm CMOS					0.18µm CMOS				
V_{ctrl} **(V)**	0	0.3	0.6	0.9	1.2	0	0.3	0.6	1.2	1.8
f_0 **(GHz)**	8.75	6.70	5.85	5.60	5.60	4.29	3.40	3.13	2.84	2.83
V_{pp} **(V)**	0.11	0.72	0.90	0.94	0.94	0.46	1.09	1.34	1.56	1.57

limits. This can be explained by the fact that low resistance of PMOS feedback transistor, operating in deep triode region, reduced significantly inverter closed loop gain. As the presented topology has the PMOS transistor feedback in each inverter stage, the effect is much more intense resulting in the unsuitably low V_{pp} value. It should be pointed out that the maximum oscillation frequency and the available frequency range depend on the ring oscillator transistors sizes. Increase in the transistors sizes reduces the observed Figures of Merits (FOM).

4.3 Buffer Feedback Influence

The method of increasing the ring oscillator frequency by using the inverter resistive feedback is already known in literature, [9]. To the best of our knowledge, the influence of the buffer feedback on the ring performance is still not examined. The two-stage buffer topologies with resistive and PMOS transistor feedback are proposed in Fig. 5. The first stage provides control/increase in the ring oscillator frequency, while the second buffer stage prevents this effect to change the output filter shaping characteristics. Dependences of performance of the ring oscillator designs in 0.13 µm and 0.18 µm UMC technologies on the buffer resistive and PMOS transistor

Table 3. Ring oscillator performance dependence on the buffer feedback resistor value.

Tech.	0.13µm CMOS					0.18µm CMOS				
R **(kΩ)**	2.32*	4.0	6.0	8.0	10.0	0.25	0.5	1.0	2.0	4.0
f_0 **(GHz)**	9.05	8.50	8.30	8.15	8.10	4.27	4.11	3.98	3.87	3.82
V_{pp} **(V)**	0.72	0.79	0.82	0.84	0.85	1.19	1.35	1.44	1.50	1.53

*Minimal resistance value for the RNHR resistor model.

Table 4. Influence of the buffer feedback transistor V_{ctrl} parameter on the ring oscillator performance.

Tech.	0.13µm CMOS					0.18µm CMOS				
V_{ctrl} **(V)**	0	0.3	0.6	0.9	1.2	0	0.3	0.6	1.2	1.8
f_0 **(GHz)**	8.90	8.25	7.70	7.45	7.4	3.94	3.74	3.63	3.55	3.55
V_{pp} **(V)**	0.71	0.82	0.87	0.87	0.88	1.17	1.27	1.37	1.47	1.47

Varying R from 10 kΩ to 2.32 kΩ in 0.13 µm technology, the oscillation frequency is increased from 8.10 GHz to 9.05 GHz, followed with decrease in V_{pp} parameter from 0.85 V to 0.72 V. Reducing R from 4.0 kΩ to 0.25 kΩ in 0.18 µm CMOS ring oscillator design, the f_0 parameter rises from 3.82 GHz to 4.27 GHz simultaneously with reduction in V_{pp} amplitude from 1.53.85 V to 1.19 V. This technique uses

feedback resistor values lower than in method presented in section 4.1 because obtained V_{pp} values are higher than $V_{dd}/2$. It can be noticed that comparing to the mentioned approach the proposed technique allows smaller increase in the ring oscillator frequency. However, it should take into account that this method uses only one resistor in contrast to three additional resistors utilized in the inverter feedback architecture, and at the same time provides higher V_{pp} parameter values for the same ring oscillator frequency. The three-stage ring oscillator period T is determined by the propagation time of a signal transition through the complete oscillator chain ($T=6\times t_p$, where t_p is the gate propagation delay). An inverter signal propagation time is largely determined by the strength of the driving gate, and the load presented by the output node itself, which sums the contributions of the connecting gates and the wiring parasitic. Varying the buffer feedback resistor changes its feedback impedance, which further modifies the buffer input impedance (Miller's theorem) leading to the change in the ring oscillator load, propagation time and the ring oscillator period/frequency.

Approach presented in Fig. 5b shows similar influence on the ring oscillator FOM. Reducing V_{ctrl} parameter from V_{dd} to zero the oscillation frequency can be tuned in the frequency ranges narrower than in technique presented in section 4.2 (especially in 0.18 μm CMOS process), but with higher obtainable V_{pp} parameter values. Moreover, the method requires only one resistor. Additionally, it can be noticed that the frequency range available in 0.13 μm CMOS technology is extensively wider than in the other considered process.

5 Discussion and conclusion

Dependences of the three-stage ring oscillator performance on resistors and PMOS transistors, introduced as feedbacks in the oscillator inverters and buffer, are investigated in 0.13 μm and 0.18 μm UMC CMOS technologies. Simulation results in both technologies confirm strong dependency of the ring oscillator frequency and the peak-to-peak amplitude on the inverters and buffer feedbacks. Considering the presented methods, higher f_0 parameter values and wider available frequency range can be obtained with topologies that use feedbacks in the ring oscillator inverters. However, these architectures require additional three resistors/PMOS transistors that occupy more area and thus increase chip cost. The topology with buffer feedback would be the best choice in case of the medium operating frequency range applications as it uses only one additional component and gives higher V_{pp} parameter values. Research presented here shows that the 0.13 μm process offers much more promising performance. Moreover, the layout designs dimensions are approximately two times smaller than in0.18 μm technology. Nevertheless, as the main drawback of the former technology is higher IC fabrication cost, the later process is chosen as optimal solution in this work. The ring oscillator-based pulse generator designs in 0.18 μm technology that combine proposed methods are presented in [11], [12].

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