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Design of Cascode-based Transconductance Amplifiers with Low-gain PVT Variability and Gain Enhancement Using a Body-biasing Technique

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Abstract. A body-biasing compensation scheme based on two proportional-to-absolute-temperature (PTAT) circuits is proposed to reduce the PVT variability of the DC gain of cascode amplifiers. A brief description of a basic PTAT is given as well as its application to cascode-based operational transconductance amplifiers. Simulation results show that the proposed compensated circuit amplifier exhibit a (DC) gain variability smaller than the original (uncompensated) circuit, while reaching a gain enhancement of about 3 dB.

Keywords: amplifier, body-biasing, CMOS analog circuits, PVT compensation

1 Introduction

In order to increase speed and reduce area, MOS devices are scaled down. However, this leads to short channel effects, thus reducing the intrinsic gain. Therefore, due to the supply reduction, high gain OpAmps are harder to design and cascode techniques are more difficult to employ 1.In analog CMOS circuit design, the transistor is preferentially used in saturation. The intrinsic gain of a MOS transistor is given by

$$A_{vi} = g_m/g_{ds} \tag{1}$$

whereg_m is the transconductance and g_{ds} is the output conductance.For a MOS device in saturation, assuming an approximate square law for the drain current, the transconductance is given by

$$g_m = \mu C'_{ox}(W/L)(V_{GS} - V_t)^2 \tag{2}$$

where μ is the carrier mobility, $C'_{ox}$is the oxide capacitance per unit of area, W and L are the width and length of the transistor, $V_{GS}$is the biasing gate source voltage and $V_t$is the threshold voltage. For a short channel, the increase of V_{DS} leads to the decrease ofV_t, thus increasing the drain current. This gives rise to an increase of g_{ds}.So, despite the increase of transconductance with scaling, the intrinsic gain is

reduced 1. This is illustrated in 2.The temperature variation leads to a decrease in both the carrier mobility and the threshold voltage. In regards to the latter, it may decrease from 2 mV up to 4 mV for every 1º C rise 3. These factors will have a direct effect on the transconductance of a transistor, as seen in (2).Also, process corners refer to the variation of fabrication parameters used in applying an integrated circuit design to a wafer. If a circuit running on devices fabricated at these process corners does not function as desired, the design is considered to have inadequate design margin. In this paper we present a circuit technique to reduce gain variability with temperature, supply and process variations in cascode amplifiers using a body-suitable biasing circuitry and at the same time increase the overall amplifier gain by about 3 dB.

2 Relationship to Internet of Things

Operational and transconductance amplifiers are, most probably, the most active building-block in analog and mixed-signal integrated circuits used in wireless and wire line communication systems. The work presented in this paper can contribute to the future development of the Internet of Things, since it can provide improved energy efficient circuit amplifier architectures, robust to temperature, supply and process variations. This ensures that a circuit manufactured to work, will perform as expected, regardless of the environment conditions.

3 Cascode Amplifiers

A single-stage operational transconductance amplifier (OTA) has usually a cascode configuration 4. We consider a traditional cascode amplifier, shown inFig. 1.

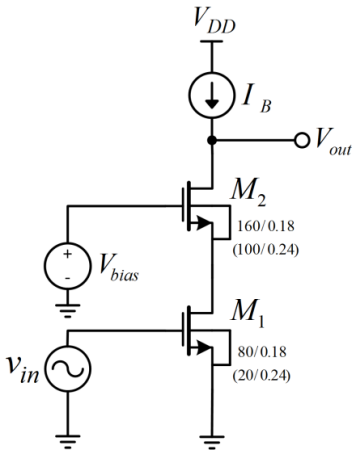


Fig. 1. Cascode Amplifier. All transistor sizes (*W/L*) are in µm. Sizes without brackets are for a 65 nm technology and those within brackets are for a 0.13 µm one.

The gain of this circuit is given by

$$A_v = g_{m1} \cdot \left[\frac{1}{g_{ds1}} \cdot \left(\frac{g_{m2}}{g_{ds2}}\right)\right] || R_B \tag{3}$$

where R_B is the resistance of the biasing current source, whose value is 100 µA and 150 µA for 65 nm and 130 nm technology, respectively. The positive power supply voltage is of 1.2 V.

Fig. 2 shows the variations of g_m, g_{ds}, and gain of transistor M_2 (g_m/g_{ds}) for 65 nm and 130 nm.

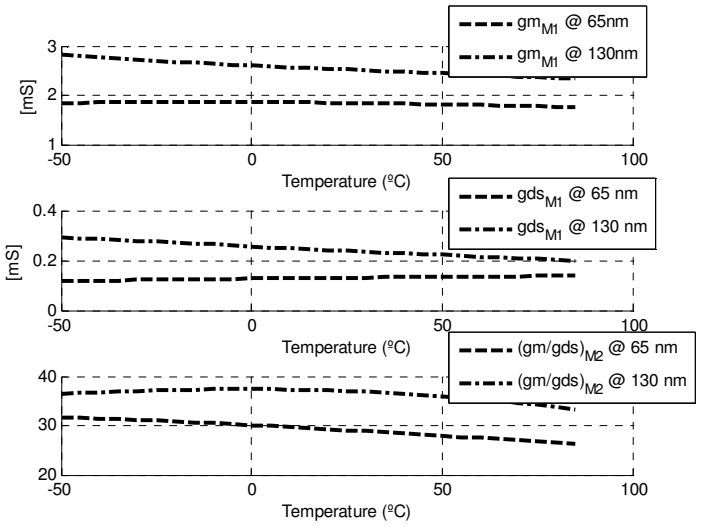


Fig. 2. Parameter variation with temperature for both node technologies.

4 Proposed Solution

Fig. 3 presents the basic proportional-to-absolute-temperature (PTAT) circuit used in this paper, known as "constant transconductance" bias circuit, proposed in 4, 5.

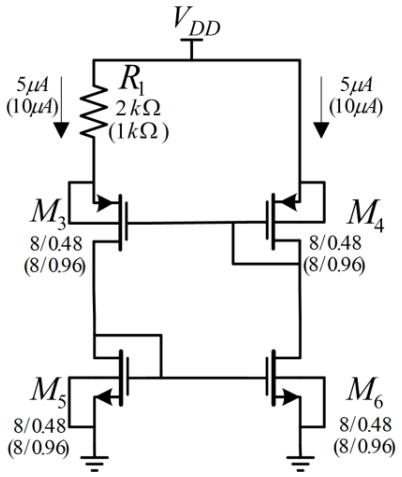


Fig. 3. Constant Transconductance Bias circuit. All transistor sizes (*W/L*) are in μm. Sizes without brackets are for a 65 nm technology and those within brackets are for a 0.13 μm one. The supply voltage is of 1.2 V.

We investigate the variation with temperature of the voltages V_A, V_B, and V_C, when all the transistors are matched.

The variation of V_A is irrelevant, since it varies less than 5 mV for the temperature range (-50 ºC to +85 ºC). For both technology nodes, V_B decreases with temperature while V_C increases, as shown in Fig. 4.

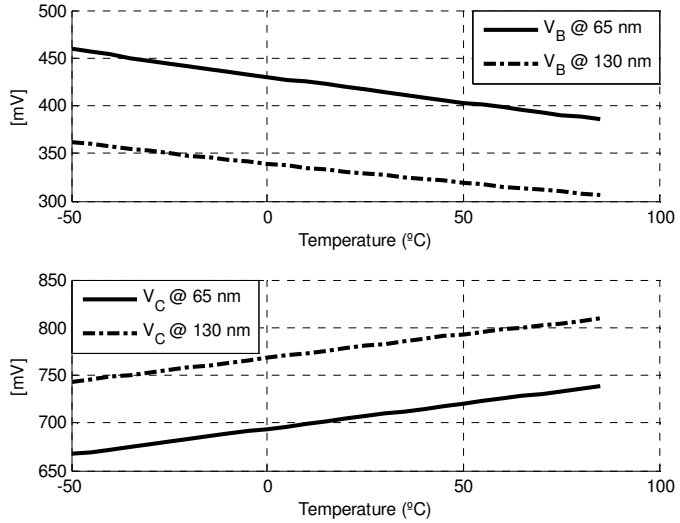


Fig. 4. Voltage variation at nodes V_B and V_C (for both node technologies).

The cascode amplifier (Fig. 1) with body-biasing by the circuit of Fig. 3 is shown in Fig. 5. The I_B current source is replaced with a current mirror, and every biasing voltage source is replaced with a MOSFET in diode configuration.

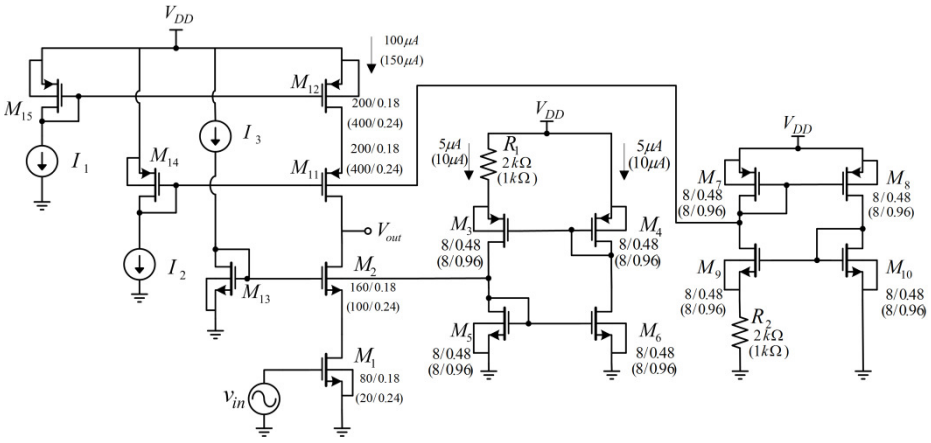


Fig. 5. Telescopic-cascode with body-biasing circuitry. All transistor sizes (*W/L*) are in μm. Sizes without brackets are for a 65 nm technology and those within brackets are for 0.13 μm.

In section III we have plotted the variations of g_m and g_{ds} in 65 nm and 130 nm. The main objective is to choose one of these voltage variations and apply it to the bulk of the M_2 transistor of the cascode circuit, biasing it in order to reduce the variability of the intrinsic gain, thus narrowing the variability of the overall gain, and increase the total gain of the circuit. The voltage V_B is used, since it decreases with temperature (for either technology), as seen in Fig. 4. If it is applied to the bulk of the M_2 transistor, it reduces the amplifier gain variability.

After replacing the current source with the current mirror, the MOSFETS that compose it also needed to have a temperature-independent behavior. Thus, the bulk of M_{11} should be connected to a symmetrical voltage to that applied to the bulk of M_2. In order to do so, a mirrored version of the "constant transconductance" bias circuit was designed.

Fig. 6 presents the variations of the transconductances of the $M_{1,2}$ transistors, when using body-biasing compensation. As it can be seen, the intrinsic gain of the M_2 transistor has a lower variation than that obtained when no body-biasing technique is used (Fig. 2), for both node technologies. Furthermore, the g_{ds} of the M_1 transistor also reduces its value while g_m increases, thus boosting the gain.

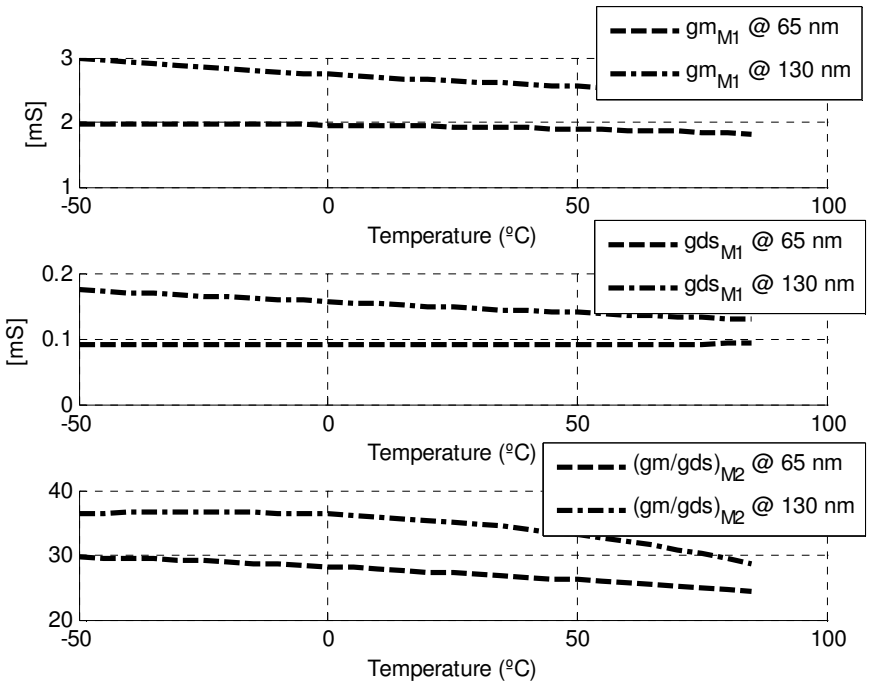


Fig. 6. Parameter variation with temperature with body-biasing compensation for both node technologies.

5 Simulations and Results

All simulations are performed using BSIM3v3 models for standard logic 65 nm and 130 nm CMOS technology. A supply voltage of 1.2 V is used and the process variations considered are slow-slow (ss), typical-typical (tt) and fast-fast (ff). The temperature range is from -50 to +85 ºC.

In Fig. 7, the gain of the circuit is plotted, for both technology nodes, with and without body-biasing technique. For both technology nodes the gain variability is lower when using the body-biasing circuitry. Furthermore, there is an enhancing of the gain by about 3 dB, as expected, as it was explained in section IV.

With regard to supply variation, Fig. 8 shows that with a variation of ± 5% (1.14 V to 1.26 V) of the supply voltage, the body-biasing circuitry leads to a lower variability for the gain (below ± 0.5 dB). Some traces can be superimposed.

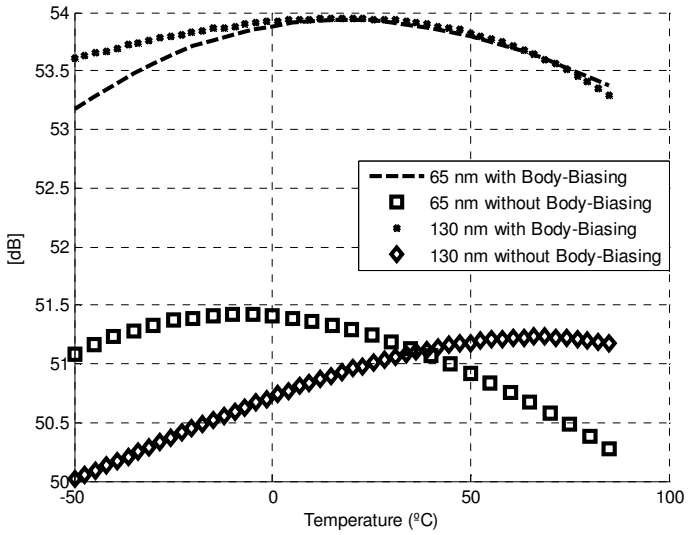


Fig. 7. Overall gain variability with temperature for both technologies node (with and without body-biasing technique).

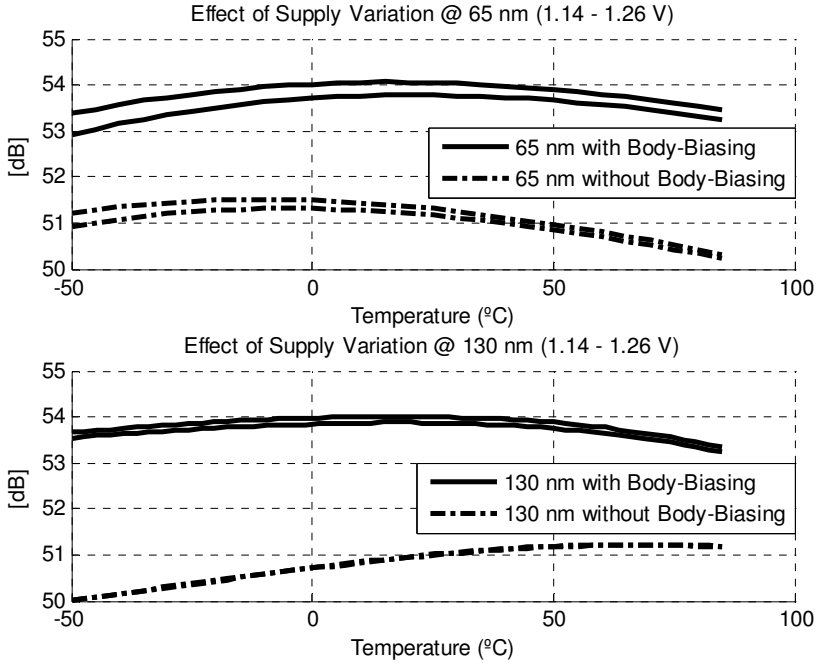


Fig. 8. Overall gain variability with temperature & supply variation for both technologies node (with and without body-biasing technique).

Concerning process variation,Fig. 9and 10 show that for the processes considered (ss, tt and ff), there is always an enhancement of the gain by about 3 dB. For most of the cases, the (DC) gain variability is below ± 0.5 dB (except for process ff, at 130 nm node technology, where the variability is higher than that without body-biasing).

This body-biasing circuitry requires only an extra current consumption of about 5% to 7% (for both technologies) of the total current consumption of the amplifier. This results in low power consumption, for both node technologies, from a 1.2 V supply.

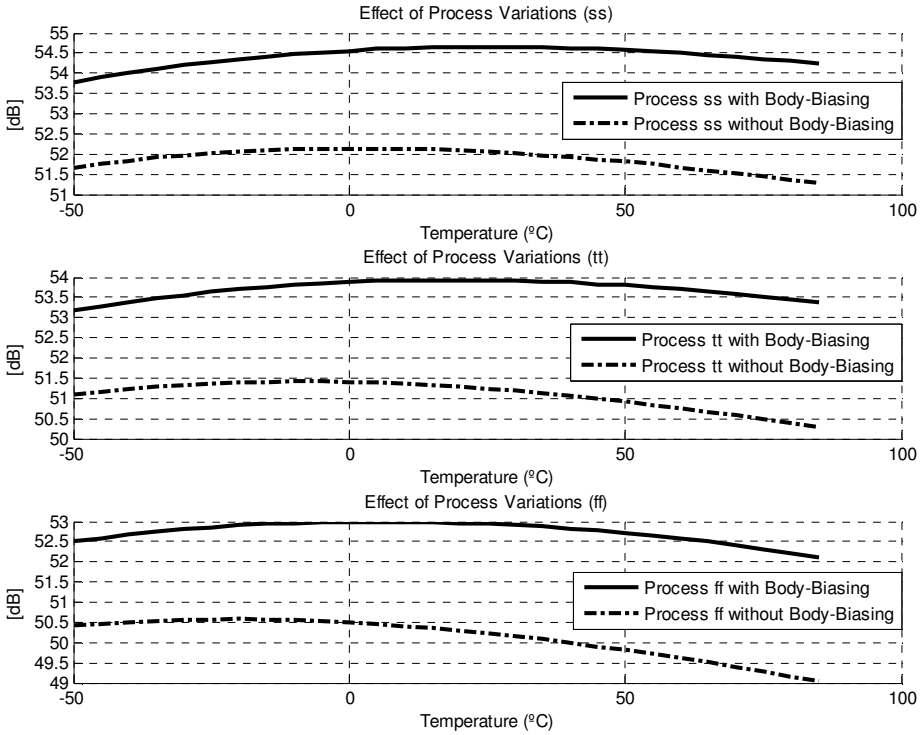


Fig. 9. Overall gain variability with temperature & process variation for 65 nm (with and without body-biasing).

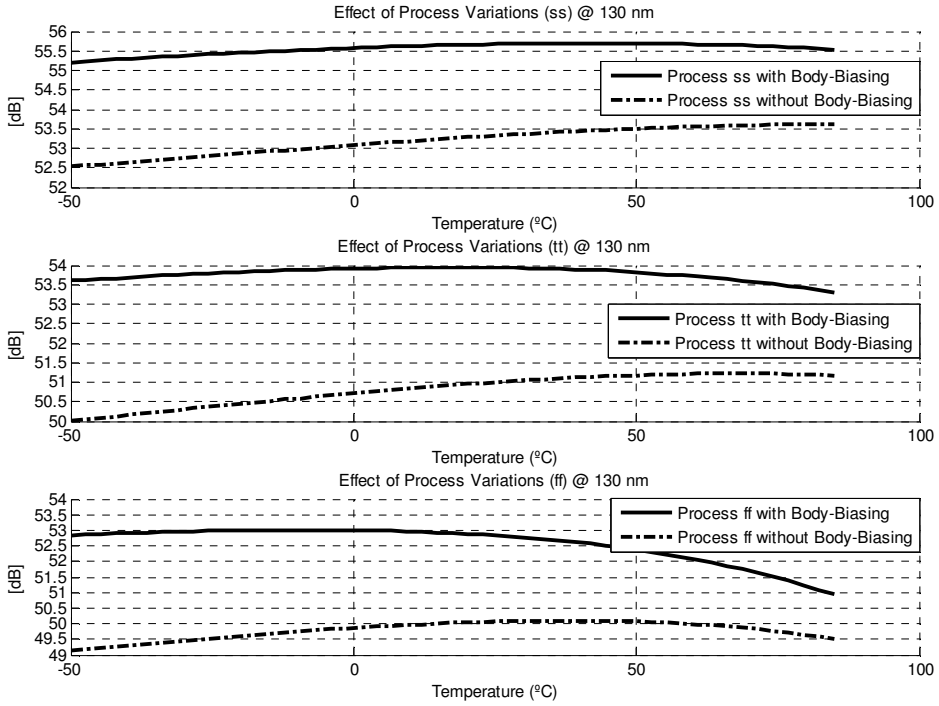


Fig.10. Overall gain variability with temperature & process variation for 130 nm (with and without body-biasing).

6 Conclusions

This paper presented a simple circuit technique to reduce gain variability with temperature, supply, and process variations in cascode amplifiers, using a body-biasing scheme, and at the same time, enhance the overall gain of the amplifier.

Simulation results of a standard telescopic-cascode amplifier, in two different nanoscale CMOS technologies (130 nm and 65 nm) have shown that it is possible to obtain process-supply-and-temperature-compensation.

The simulated DC gain has low variability (below ± 0.5 dB for all supply-and-temperature variations) while it is enhanced, over all PVT corners by 3 dB.

The authors are unaware of the existence of similar body-biasing compensation schemes to reduce the PVT variability of the DC gain, up to this date. Therefore, it was impossible to perform a comparison with other body-biasing schemes.

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