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New Approach for an Accurate Schottky Barrier Height's Extraction by I-V-T Measurements

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Abstract — This paper proposes a diagnostic tool dedicated to the analysis of the Schottky Barrier Height (SBH). The proposed method is mainly relevant for studying gate related failure mechanisms in electronic devices. In this case, the SBH of gallium nitride High Electron Mobility Transistors (HEMTs) is investigated in terms of mean SBH's value and dispersion. It is shown that according to given temperature and gate current ranges, linear relationships can be extracted between the mean SBH and the inhomogeneities that appear in forward-biased diode. These behaviors are able to highlight different kind of defects, revealing possible weaknesses of the devices.

Index Terms — Energy barrier, gallium nitride, reliability, Schottky gate field effect transistor, semiconductor-metal interfaces, thermal analysis.

I. Introduction

AlGaN/GaN HEMTs devices are already known for their high performances in microwave field. Yet, issues of reliability still represent a challenge as the increase of the junction temperature can open the way for new high power and high frequency applications. The mastering of reliability represents a challenge for large volume production dedicated to base stations but also to defense and space applications. However, reliability investigations are tricky because of the complex electro-thermo-mechanical mechanisms induced in the transistors; these studies can only be carried out by using several cross-experiments or by using destructive techniques in order to evidence the presence of defects. Nevertheless, destructive techniques definitely do not allow concluding about the real impact of the revealed defect on the electrical behavior of the device. The development of new non-invasive (and so non-destructive) experimental techniques can thus bring information about the evolution of electrical signatures before (during) and after application of a stress.

For this study, a High Temperature Operating Life (HTOL) stress test has been applied on different batches of AlGaN/GaN HEMT devices featuring 8x125µm gate width (technology 0.25µm gate length). The measurements reveal a drop on I_{DS} of about 45% (@ V_{GS}=1V and V_{DS}=8V), an increase of 130% on R_{ON} and about 1-decade variations on I_{GS} over 105 hours of stress at 175°C ambient temperature (320°C junction temperature).

It is now largely assumed that the gate terminal is one of the key points impacting a large number of failure mechanisms or at least impacting the performances of the device (shift of V_{th}, reduction of the transconductance gain and of the carriers' density in the two-dimensional electron gas - 2DEG, accumulation of charges between gate and source/drain that reduces the linearity, back-gate effect, etc.). From previous studies [1], [2], different methods have been developed in order to investigate the Schottky Barrier Height (SBH) leading to a better comprehension of its representation. The approach from [3] brings information about the mean barrier height and its relative dispersion (inhomogeneity of the Schottky barrier height). This technique is non-destructive as it is based on an electro-thermal characterization of the device in open drain configuration (no dissipated power in the 2DEG). In this way, new domains of application such as reliability purposes can be explored through the study of virgin and stressed devices. Fig. 1 presents the gate current versus the gate-source voltage plots at different temperatures for a stressed device $S_{\#2}$ (the virgin device $V_{\#6}$ is plotted in the inset caption):

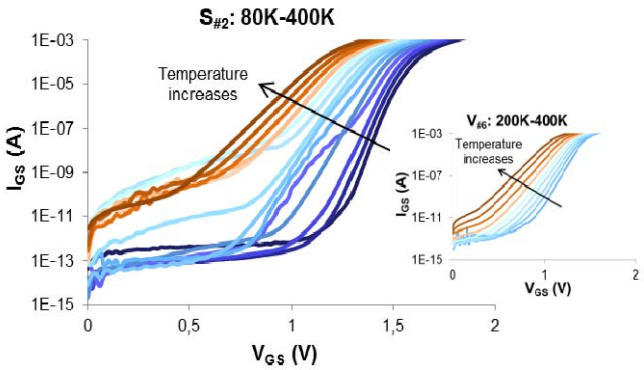

Fig. 1. I_{GS}-V_{GS} measurements vs temperature, with 25K step, for $S_{\#2}$ (stressed) and $V_{\#6}$ (inset, virgin) devices. Dark blue is represented as the lowest temperature towards dark brown as the highest temperature.

This paper is divided in three main sections: the first paragraph briefly presents the method and the second part develops an original approach using the variations of the extracted mean barrier height ($\overline{\Phi_B}$) and dispersion (σ_S) versus the gate current level (I_{GS}), for different temperature ranges. Results are discussed in section three for virgin and stressed devices, before drawing conclusions of the work.

II. Method

As specified earlier, this study focuses on the Schottky contact, formed by a stack of 3 metals (Ni/Pt/Au) in this case. The aim is to investigate the Schottky diode through an accurate evaluation of the SBH and at term to incriminate or to exclude gate conduction mechanisms or defects. The most common approach consists in modeling the gate current by using the thermionic equations (1a) and (1b) [1], [2]:

$$I_{GS} = I_S exp\left(\frac{qV_{GS}}{nkT}\right) \qquad (1a)$$

$$\text{with} \quad I_S = SA^*T^2 exp\left(\frac{-q\Phi_B}{kT}\right) \qquad (1b)$$

The method on which is based this work also uses the thermionic model, applied for each temperature (between 80K and 400K). It can be seen in Fig. 1 that for low V_{GS}, the thermionic model does not fit all the different behaviors and hardens the exploitation of the model. However, the relative flat current contribution (low V_{GS}) is above the measurement setup floor of the experimental setup used for the electrical characterization of the devices (Agilent 4156C – sensitivity 1fA). All the specific behaviors related to the experimental sensitivity and to the method robustness have been previously studied, so that all the exploited measurements are reliable for analysis, as discussed in section III.

Further, the thermionic model used for the method developed in [3] is focused here on a 2-decade gate current range (in open drain configuration) for each temperature; then, the evolution of the mean SBH and standard deviation can be extracted for the studied samples.

III. Measurements and Results

The samples under test are AlGaN/GaN HEMTs. Devices feature a gate length of 0.25 µm and the analysis is carried out for 2 batches of devices (4 stressed samples labeled $S_{\#index}$ and 2 virgin samples labelled $V_{\#index}$). Hereinafter results are presented and discussed only for a witness transistor ($V_{\#6}$) and for a stressed device ($S_{\#2}$). Current leakages of these samples are also specified (in open drain configuration, @ V_{GS} = -9V and ambient temperature): $I_{GLEAK,V\#6}$ = -17 nA/mm and $I_{GLEAK,S\#2}$ = -66 nA/mm.

In the previous model from [3], only the higher ranges of temperature (above 200K) and higher current decades are considered, as the ideality factor n can be largely overestimated from a thermionic model formulation at lower temperatures and/or at lower gate current levels. For this study, all the temperatures are considered and analyzed over each set of 2-decade gate current (i.e. also considering possible contributions of trap assisted tunneling, impact ionization phenomena etc.). Fig. 2 plots the extracted SBHs versus temperature:

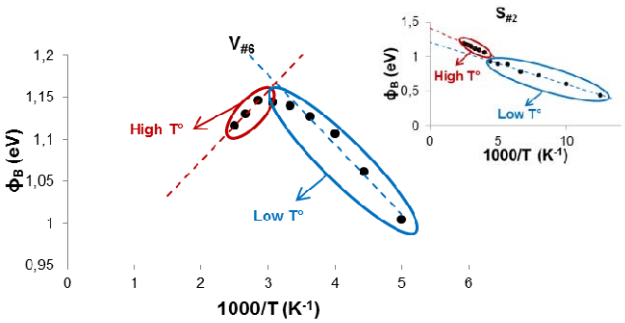

Fig. 2. Plot of the SBHs for all temperatures (200K-400K) for the witness device $V_{\#6}$ (stressed device $S_{\#2}$ in insight) and within $10^{-6} \div 10^{-4}$ A 2-decade current range. The points encircled in blue delimit the low temperature range and those encircled in red the high temperature range.

It can be noticed that 2 linear trends can be extracted: an inflexion point is distinguished for each device (325K for $V_{\#6}$, and 225K for $S_{\#2}$). For the virgin device, an inversion of the slope is also revealed at higher temperatures, whereas only the slope value changes for the stressed device $S_{\#2}$. Hereinafter, these 2 temperature ranges identified above are considered, indicated in figures by Low T° (low temperature) and High T° (high temperature).

By following the same procedure than the one proposed in [3], each 2 decades of the gate current (hereafter denoted by 'x') are systematically characterized by an ideality factor (n_x) and a SBH (Φ_{Bx}). For each temperature range (Low T° and High T°) of the 'x' gate current interval under study, a set of mean SBH $\overline{\Phi_{Bx}}$ and its associated standard deviation σ_{Sx} are extracted. From this systematic study versus the current range (each 'x' range), data ($\overline{\Phi_{Bx}}$, σ_{Sx}) are evolving largely out of the uncertainty range: the mean SBHs are between 0.9eV and 1.5eV, interval which is largely out of the method's extraction accuracy (less than 7% on $\overline{\Phi_{Bx}}$ for more than 50% variation on initial conditions for Richardson constant A* and effective mass m*). Therefore, these variations can be considered as specific appreciations of the mean barrier height and its associated inhomogeneity (standard deviation) over the exploited current range 'x'. These largely dispersive values are different from the expected theoretical values (around 0.9eV for a metal compilation Ni/Pt/Au [4]).

Next, a reinterpretation of the results ($\overline{\Phi_{Bx}}$, σ_{Sx}) is proposed by plotting $\overline{\Phi_B}$ versus σ_S for all the extracted values (Fig. 3 and Fig. 4). Therefore, the variation of the mean SBH versus the standard deviation (inhomogeneity) can be interpreted as the sensitivity of 'ideal' SBH's value to the defects of the barrier height (inhomogeneities at the metal-semiconductor interface). Thus, the x-axis extrapolation at σ_S=0 represents

the Φ_B value of the ideal Schottky diode without considering defects (a homogeneous SBH).

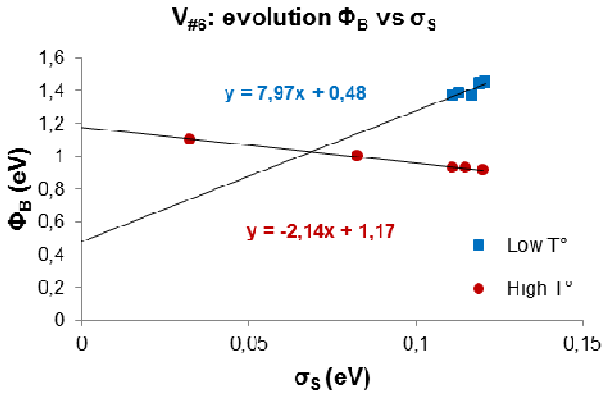

Fig. 3. Variations of $\overline{\Phi_B}$ vs σ_S for the virgin device ($V_{\#6}$), under different gate current ranges. Blue squares represent the values of $(\overline{\Phi_B}, \sigma_S)$ at low temperature and red circles are the values at high temperature.

Results from Fig. 3 (respectively Fig. 4) feature different sets of $(\overline{\Phi_{Bx}}, \sigma_{Sx})$ in each low and high temperature ranges, for the virgin device (respectively stressed device). Linear trends can be extracted for each device and for each specific temperature range:

- two different trends are identified for $V_{\#6}$ in low and high temperature range (Fig. 3) and can be related to the behavior revealed in Fig. 2 (inversion of slopes);
- for the stressed device $S_{\#2}$, the two temperature ranges seem to provide the same behavior as shown in Fig. 4 (also convenient with the identical slopes trends in the insight caption of Fig. 2).

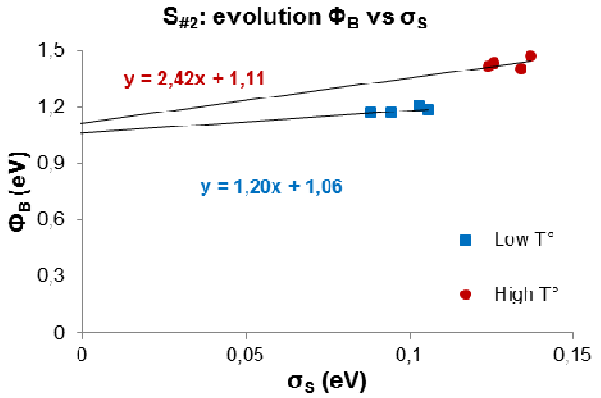

Fig. 4. Variations of $\overline{\Phi_B}$ versus σ_S for the stressed device ($S_{\#2}$), under different gate current ranges. Blue squares represent the values of $(\overline{\Phi_B}, \sigma_S)$ at low temperature and red circles are the values at high temperature.

IV. Analyze

With this original representation, the x-axis extrapolation at σ_S=0 (no inhomogeneity) gives the ideal SBH value. For the stressed device $S_{\#2}$ featuring a large leakage current (-66 nA/mm), this SBH is extrapolated around 1.1 eV for each temperature range. The virgin device analysis gives rise to two different SBHs at 0.5eV and 1.2eV respectively for low and high temperature ranges; because the high temperature SBH (1.2eV) is close to the one of the stressed device, the low temperature SBH (0.5eV) could sustain the hypothesis that several secondary diodes are activated and form the 'global' Schottky diode.

The high temperature value of Φ_B, which is convenient to the one of the stressed device, is associated to the main barrier height of the Schottky diode. Nevertheless, in the high temperature range, the extrapolated value for stressed and virgin devices is slightly above the theoretical value of a Ni/Pt/Au Schottky contact (0.9eV [4]). However, it must also be considered that in nitride technologies, the presence of a large density of charges between gate and source terminals (at interlayers) could affect the intrinsic potential. This fact could explain the shift in the extracted SBH at 1.15eV (average over 5 devices under test). Only one device between the batch of 6 transistors feature a unique SBH value (still taken at zero inhomogeneity) for the entire temperature range (100K-400K), which is very close to the theoretical value of a Ni/Pt/Au Schottky contact [4]: 0.8eV. It is assumed that this specific device is not very sensitive to the presence of charges, in comparison with the other samples from the batch.

Considering the lower temperature range for the virgin device, the extrapolated SBH is 0.5eV, i.e. largely below the theoretical value; it seems that low temperature analysis brings different information about the SBH than the one issued from high temperature for the virgin 'low leakage' device. The assumption is that at low leakage currents, different mechanisms can contribute to I_{GS}. If considering defects at the metal-semiconductor interface (voids, Au diffusion, charges …), then different diodes can operate, featuring specific barrier heights. In the case of the virgin transistor $V_{\#6}$, the extrapolation at σ_S=0 at low temperatures reveals a diode with a lower barrier height (i.e. the diode that needs lower energy to overcome the barrier).

This behavior is also supported by the change of slope in Fig. 2: two different slopes are identified for high and low temperatures, i.e. different thermal dependencies of ϕ_B for the main diode at high temperature (red dashed line) and for the 0.5eV-diode at low temperature (blue dashed line). Furthermore, the inflexion temperature in Fig. 2 discriminates between two different behaviors of these diodes: ϕ_B increases with temperature (decreases with 1000/T) for the lower 0.5eV-diode, whereas ϕ_B decreases with temperature (thus, increases with 1000/T) for the main diode. Consequently, the lower barrier height will systematically be the one which dominates, according to temperature range (main diode at high temperature and 0.5eV-diode at low temperature, respectively). In addition, the value of 0.5eV for the SBH revealed at lower temperature for the virgin device can be associated to Ni, Pt or a Ni/Pt stacked metals [4], [5].

Lastly, it can be noticed in Fig. 2 that the sign of the slopes differs between stressed and virgin devices at high

temperature. In spite of these different trends, the σ_S=0 extrapolation in Fig. 3 and Fig. 4 (still at high temperatures) features the same SBH: at 1.17eV and 1.1eV, respectively (the sign of the slope is correlated to those of Fig. 2 between $V_{\#6}$ and $S_{\#2}$ at high temperature).

The analysis carried out for the other transistors only comes to strengthen the previous assumptions. Both virgin samples feature the same behavior, with exactly the same values for Φ_B at σ_S=0 (no inhomogeneity) for high and low temperature ranges. On the other side, one of the aged devices featured an anomalous value of the 'ideal' SBH in low temperature range, at 0.1eV. Since Φ_B of the Schottky contact is an energetic barrier which prevents the gate current from passing through, and since the obtained value for the Schottky barrier height is almost close to the value of a 'short-circuit', we are inclined to believe that the 0.1eV effective barrier height is in fact due to a lowering (or bypassing) the main SBH of the diode. It is important to notice that this 0.1eV value is only appreciated by the σ_S=0 extrapolation: this defect is then identified even if not sensitive on the overall value extracted at each temperature, certainly due to a low weighted contribution of this defect! This hypothesis is reinforced by the prior argument assessing that the extracted barrier height will be associated to the lowest energetic path (between all possible solutions) between the gate foot and the semiconductor. However, if this particular case cannot be directly linked to previously published results in the literature, some works have evidenced the presence of gold that appear near the gate foot edge [6], which could be convenient to explain such a low energetic value on a small area of the Schottky diode.

V. Conclusion

A new approach of Werner's improved model is proposed. While the previous model [1] and the improved method [3] are limited in temperature range or gate current level confidence interval, this work provides a new understanding in terms of SBH's inhomogeneity at metal-semiconductor interface. It has been shown that the study at different temperatures with a systematic analysis versus the gate current range can lead to the observation of inhomogeneities for the main Schottky diode, as well as the occurrence of lower barrier diodes under specific temperature ranges.

This study has been applied on virgin and stressed HEMT devices; from representation of the mean barrier height $\overline{\Phi_B}$ versus the standard deviation σ_S (i.e. inhomogeneity of the SBH), the extrapolation at σ_S=0 eV is stated as the 'zero-defect' diode's barrier height (homogeneous). The same value (1.15eV) is featured for aged and virgin devices (set of 5 transistors) at high temperature. This value of the SBH is quite convenient to the one issued from literature (given at 0.9eV). Though, it is important to bear in mind that AlGaN HEMT devices may feature many parasitic mechanisms, such as activated charges, which can add an intrinsic voltage generator to the applied gate voltage. Thus, the slightly increase of the SBH compared to the expected theoretical values can be justified by the presence of intrinsic charges.

Some devices (virgin transistors) also reveal a lower SBH at lower temperatures, as a consequence of the lower leakage current, where at least two Schottky diodes seem to contribute. Furthermore, these lower values of the SBH can be correlated with an imperfection of the Schottky contact (pits, cracks with activation energies ranging from 1.05eV to over 2.2eV [6]), as the gate stack is composed by 3 metals (Ni/Pt/Au) which can mix and form intermediate mixtures [4], [5]. On the other hand, unrealistic low values are also obtained from the analysis (~ 0.1eV) which cannot be associated to a SBH. Therefore, we believe that the proposed method is appropriate to accurately study the SBH and its relevant defects. Still, more investigations need to be carried out in order to identify the nature of each defect, and to overcome its contribution for improved reliability of AlGaN/GaN HEMT transistors.

This non-invasive and robust method stands as a powerful diagnostic tool for the specific study of the Schottky diode's contribution to failure modes in reliability studies, as the control of the barrier height (and its stability versus time) is one of the key challenges for high performance devices.

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References

[1] J. H. Werner and H. H. Guttler, "Barrier inhomogeneities at Schottky contacts," *J. Appl. Phys.*, vol. 69, no. 3, p. 1522, 1991.

[2] S. Chand and J. Kumar, "Evidence for the double distribution of barrier heights in Schottky diodes from I-V-T measurements," *Semicond. Sci. Technol.*, vol. 11, no. 8, p. 1203, 1996.

[3] S. Karboyan, J. G. Tartarin, and B. Lambert, "Analysis of barrier inhomogeneities in AlGaN/GaN HEMTs' Schottky diodes by IVT measurements," in *Microwave Integrated Circuits Conference (EuMIC), 2013 European*, 2013, pp. 240–243.

[4] N. Miura, T. Nanjo, M. Suita, T. Oishi, Y. Abe, T. Ozeki, H. Ishikawa, T. Egawa, and T. Jimbo, "Thermal annealing effects on Ni/Au based Schottky contacts on n-GaN and AlGaN/GaN with insertion of high work function metal," *Solid-State Electron.*, vol. 48, no. 5, pp. 689–695, mai 2004.

[5] B. Ofuonye, J. Lee, M. Yan, C. Sun, J.-M. Zuo, and I. Adesida, "Electrical and microstructural properties of thermally annealed Ni/Au and Ni/Pt/Au Schottky contacts on AlGaN/GaN heterostructures," *Semicond. Sci. Technol.*, vol. 29, no. 9, p. 095005, Sep. 2014.

[6] R. Stevenson, "Understanding Imperfections in GaN HEMTs," CS Mantech, Denver (USA) , May 2014.