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A novel active variable gain X-Band amplifier in SiGe technology

Rémi Corbière^{1,2}, Bruno Louis¹, Jean-Guy Tartarin²

¹Thales Systèmes Aéroportés, 2 avenue Gay Lussac, 78851 Elancourt, France CN/215

²LAAS-CNRS, Université de Toulouse, 7 avenue du Colonel Roche, 31077 Toulouse, France

Abstract — In this paper, a new structure based on variable gain amplifiers (VGAs) in SiGe technology with high linearity ($\text{Pin1dB} > 8 \text{ dBm}$) and high dynamic range ($> 30 \text{ dB}$) under 3.3 V is presented. In this proposed technique, two VGAs and a passive attenuator are used to improve the linearity especially at high attenuation. The simulated gain errors are less than $\pm 0.1 \text{ dB}$ for a 0.5 dB step over the whole dynamic gain range (31.5 dB). The Pin1dB is better than 8 dBm at the maximum gain of 8 dB and better than 22 dBm above 16 dB of attenuation.

Index Terms — High linearity amplifiers, Monte-Carlo simulations, RF analog circuits, Silicon bipolar/BiCMOS process technology, Variable gain amplifiers (VGAs).

I. INTRODUCTION

Nowadays, RF building blocks used in “radars equipments” and “electronic warfare” are essentially based on GaAs technology. This technology takes advantage on his good intrinsic linearity and noise figure, but suffers from its high cost and the poor integration which doesn’t allow to make easy the implementation of control interfaces and bias circuits. Now SiGe technology, firstly developed for the growth of civil applications as GPS, cellular phones (GPRS, EDGE, UMTS, ...) and wireless applications, is able to replace GaAs in high frequency applications to satisfy both cost reduction and integration needs.

For the system key parameters of a receiver are noise figure and linearity. The LNA is important but the VGA is a key building block as well. The main difficulty is to guarantee the linearity in the whole signal power dynamic range.

Since VGA function has to maintain a constant output signal power level, this work propose a solution that improves the input linearity to reduce the degradation effect caused by large signal input swing.

First the architecture and principle of this new VGA is discussed in section II, and the performances are presented in section IV. Then an original technique to improve the bandwidth of the function is depicted in section III. Furthermore a dispersion analysis, using Monte-Carlo simulations is introduced in section IV.

II. ARCHITECTURE / PRINCIPLE OF THE ATTENUATOR

The Silicon Germanium (SiGe) BiCMOS technology of STMicroelectronics (BiCMOS7RF – 0.25 μm) is used for this work. The study has been performed to get at least 30 dB dynamic range in X-Band (10 GHz), with the best linearity achievable.

A. Device architecture

The architecture is based on two parallel elementary VGA blocks. Each VGA is built from two stacked differential pairs, which form an original cascode structure. The block diagram of the global VGA is shown in Fig. 1.

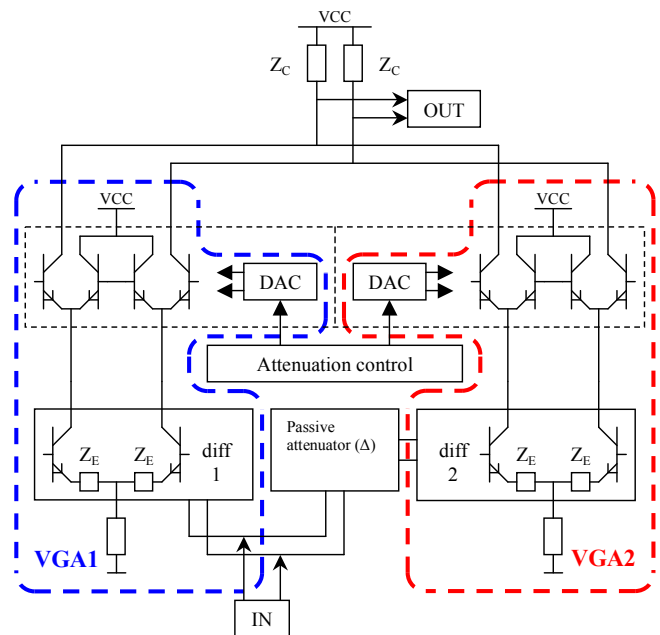


Fig. 1 Conceptual block diagram of the differential VGAs attenuator

For each VGA (depicted as VGA1 and VGA2 in Fig. 1), the lower differential pair is driven by the differential input signal and forms a common emitter pair. Its output is connected to the upper differential pair, which forms a multiplier cell structure. This latter multiplier is used, thanks to the DAC command, to monitor the gain through the g_m of the active devices (HBT).

The attenuation command is achieved by monitoring two complementary currents with an 8-bit DAC, which controls the multiplier cells. The aim is to drive a portion of the signal from the input to the load, while the remaining signal is driven to the power supply in order to get the expected attenuation.

To achieve the dynamic attenuation range, an identical stage (VGA2) is added as depicted in Fig. 1. This second stage is preceded by a differential passive attenuator set to 16 dB for this work, in order to achieve a good transition from the structure VGA1 to VGA2.

The differential gain of the VGA structure set to the maximum gain is given by the equation below:

$$G_o(dB) = 20 \log \left(\frac{g_m}{1 + g_m \cdot Z_E} \cdot Z_C \right) \quad (1)$$

Where g_m is the transconductance, Z_E the emitter impedance of the lower differential pairs, and Z_C the load impedance.

If we assume that all transistors, impedances and transconductances are identical for each VGAs, we can write that $g_{m1} = g_{m2} = g_m$ and $Z_{E1} = Z_{E2} = Z_E$.

So the differential gain of the global VGA structure with the weighting gain C_i is given by:

$$G_d(dB) = G_o(dB) + 20 \log[C1 + (\Delta \cdot C2)] \quad (2)$$

Where $C \in [0:1]$, and Δ represents the value of the passive attenuator placed between VGA1 and VGA2: here Δ is $10^{-16/20}$.

For low attenuation levels (< 16 dB), both VGAs are biased according to the following configuration: VGA1 is tunable and VGA2 is set to its maximum gain. Then for higher attenuation values VGA1 is switched off while only VGA2 (with the passive attenuator) is biased to control the gain.

So the differential gain can be written as following:

$$ATT \leq 16 \text{ dB: } G_d(dB) = G_o(dB) + 20 \log[C1 + \Delta] \quad (3)$$

$$ATT \geq 16.5 \text{ dB: } G_d(dB) = G_o(dB) + 20 \log[\Delta \cdot C2] \quad (4)$$

B. Control interfaces

The full block diagram of the proposed VGA with its control interfaces is shown in Fig. 2. On the right side we can see both VGAs with multipliers structure while on the left side the DAC command is displayed. A single ended RF input is sourced to a passive split “balun” to present a balanced signal at the VGA input structure.

The attenuation is programmable thanks to a control interface, which consists of a DATA input, a clock CLK, and a LATCH to synchronize data. Each VGA is controlled by two 8-bit DACs. One is used for the multiplier and the other is used to set the current and so the transconductance value g_m .

III. PERFORMANCES OF THE STRUCTURE

A. Gain and gain errors

The maximum gain available is shown in Fig. 3 (8 dB at 10 GHz). This can be achieved for weighting gains $C1 = C2 = 1$. The 1 dB bandwidth is slightly higher than 2 GHz (20%).

We can control the gain, over a 31.5 dB dynamic range with 0.5 dB resolution step thanks to a dB-linear-scaled law applied to the DACs [1].

The simulated maximum peak error remains below 0.1 dB in the whole dynamic of attenuation.

It confirms the excellent resolution achieved through the original configuration featuring two VGAs stages and a fixed attenuator.

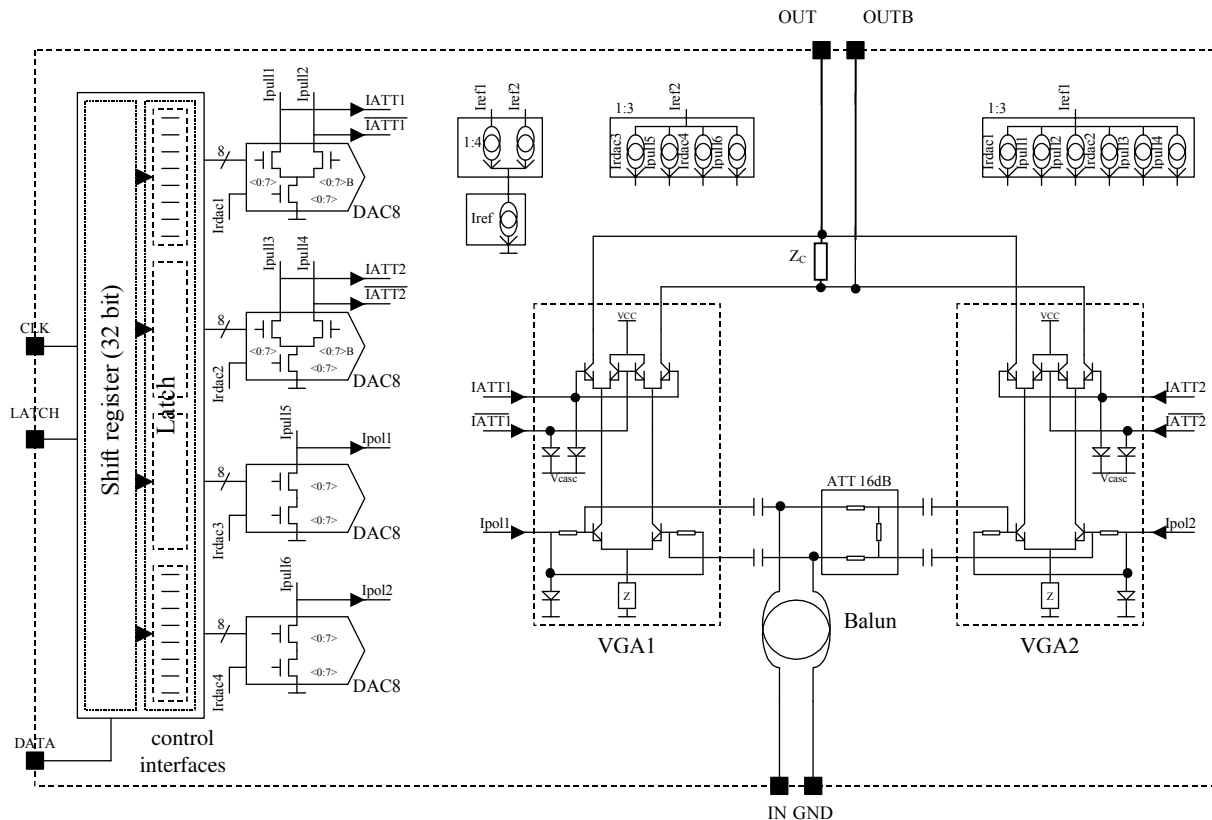


Fig. 2 Full diagram of the differential VGA and its control interfaces

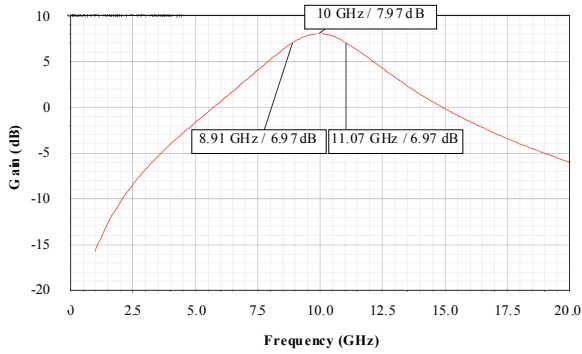


Fig. 3 Maximum gain centered around 10 GHz

B. Linearity

The use of both VGAs with the passive attenuator set to 16 dB allows some linearity improvement (Fig. 4). Linearity of a single VGA is reported in dashed line in Fig. 4; it is constant in the whole dynamic range (with a compression at $P_{in,dB} \# 9$ dBm). Furthermore the structure drastically improves the input linearity for high attenuation (i.e. high input powers) compared to the single VGA structure.

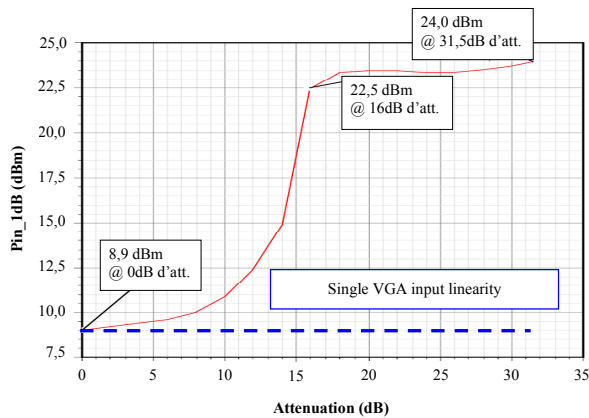


Fig. 4 10 GHz linearity improvement

The input linearity becomes 22.5 dBm at 16 dB against 9 dBm for the single structure; this difference (22.5 dBm-9 dBm) is mainly attributed to the passive 16 dB attenuator. Moreover for higher attenuation levels, compression point remains above this 22.5 dBm value. Thus, this improved linearity is very attractive for high attenuation levels, which correspond to large signal swings at the input.

IV. BANDWIDTH CONSIDERATIONS

Ultra-wideband (UWB) technique is a promising and strongly evolving technique in nowadays Active Electronically Scanned Array (AESA) radars. One of the more commonly used structures is the distributed one to deal with such a signal. Different silicon-based distributed amplifiers have been published in the past decade [2] but suffer from low quality factor of passive elements (spiral inductors), which reduces gain, from an increasing chip size especially due to passive devices, and from an increasing of the power

consumption. Moreover this technique is well suited for fixed gain amplifiers but is critical for VGA due to its control gain complexity.

A. Bandwidth limitation location

Firstly, it is essential to identify the devices, which contribute to the bandwidth limitation:

-The output load formed by a parallel RLC network. This structure can be replaced by a series RL network which acts as a second order filter with output HBTs parasitics capacitors. This technique is known under the term of “peaking” [3].

-The resonator formed by a parallel LC network at the lower differential pairs. Its aim is to drastically increase the Common-mode rejection ratio (CMRR) at the frequency of study (10 GHz). This structure can be replaced by a bipolar current mirror (Fig. 2, I_{pol1} and I_{pol2}) which controls bias of each VGA instead of its use at the transistors bases of the differential pair. These two changes require an increase of the power supply for correct Vce on bipolar mirror and voltage fall across the load resistance. For these two reasons power supply is now set to 4.3V.

-At last the split input balun is removed and the single-ended input is only applied to one transistor base of the lower differential pair. The other base is set to an AC ground.

B. Original Balance technique for the lower differential pair

The relative low output impedance (about 100 Ω) of the bipolar transistor at 10 GHz doesn't allow a high quality current mirror and so degrades the CMRR.

If we focus on the current through the impedance of the bipolar mirror (Fig. 5) we can assume that it can be written as the simplified equation:

$$i = \frac{v1}{2} \cdot \frac{1}{\frac{h_{11E}}{2} + \frac{Z_E}{2} + Z_G} \cong \frac{v1}{2Z_G} \quad (5), (6)$$

Where $v1$ is the single-ended input, h_{11E} the bipolar transistor input impedance of the lower differential pairs, Z_E the emitter impedance and Z_G the bipolar mirror impedance. Neglecting h_{11E} and Z_E according to the high Z_G impedance in (5) the current becomes (6).

Applying this result to the single lower differential pair we can assume that the current through the impedance of the bipolar mirror can be compensated by a feedback between the base of transistor Q1 and the collector-base of transistor Q2 (Fig. 5). In this case, the value of this feedback must be set to $2Z_G$.

By using this original approach only on VGA1 structure, and thanks to the dB-linear-scaled law computed up to 16 dB of attenuation, the maximum gain available and the different gain attenuation states is shown in Fig. 6.

The new 1 dB bandwidth is now increased up to 8.35 GHz (versus 2 GHz in the previous case in Fig. 3). Maximum gain available is increased due to higher power supply and impedance load.

An important point is that the low-frequency cut-off is only set by the input AC coupling capacitors values. In Fig. 7 they are set to 4 pF by on-chip capacitors.

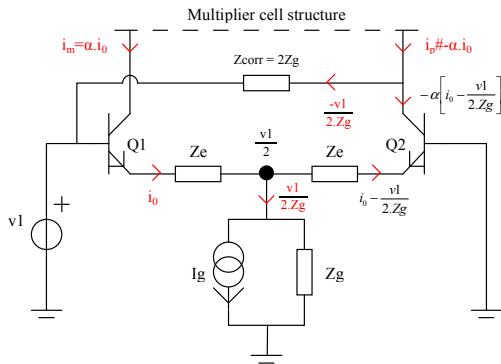


Fig. 5 Local feedback in the single lower differential pair

Increasing these values or using out-chip capacitors allow lower down-frequency cut-off.

Moreover high-frequency cut-off is mainly set by the transition frequency f_T of the bipolar transistors. Furthermore we can verify from Fig. 6 the good agreement between each different gain and attenuation values over the wide frequency range. This original technique is part of a THALES patent pending.

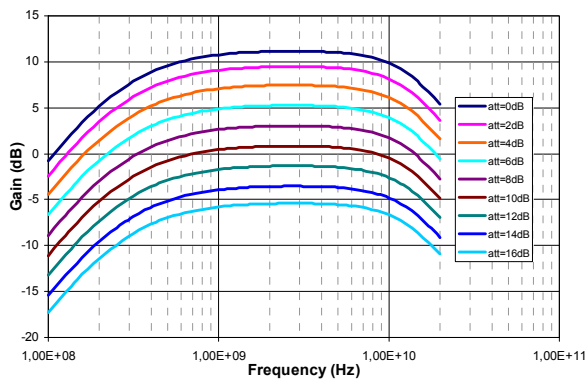


Fig. 6 Different gain available in the frequency range

V. DISPERSION ANALYSIS

As such circuits are devoted to radar systems, requiring numerous circuits, another key performance concerns its good reproducibility. To evaluate such a performance, Monte-Carlo analysis is performed. The higher contributor is located at the last bipolar current mirror: this mirror generates at the same time the dual current for attenuation (Fig. 2, I_{pull1} and I_{pull2}) and the reference current for its DAC (I_{rdac1}). Process variations are not critical because they only contribute to absolute gain variation. Thus, the dB-linear-scaled response is not affected. Mismatch variations are more critical because they affect the fundamental laws on which is based the structure. The reference current (I_{rdac1}) is not critical because it sets the transconductance g_m and so on, impacts absolute gain variation like process variation. In contrast, the dual current for attenuation affects the dB-linear-scaled response. So, gain variation increases with attenuation to reach ± 0.6 dB at 1σ for 16 dB of attenuation (Fig. 7).

To improve the dB-linear-scaled response, an original technique based on the control of the current-diodes multiplier

cells (Fig. 2) is developed. According to the dB-linear-scaled law, current through the diode must be zero on $\overline{I_{ATT1}}$ at the maximum gain available. On the other hand, at the maximum attenuation, current through the diode $\overline{I_{ATT1}}$ must be also zero. In order to be independent of current-direction, the “pump” current of the DAC command ($\overline{I_{rdac1}}$) is lowered to have positives currents through $\overline{I_{ATT1}}$ and $\overline{I_{ATT1}}$ (respectively at the maximum and minimum attenuation). There typical values (I_{typ}) are identical due to symmetrical structure.

In order to derivate these new currents, a shift register drives a current source whose role is to cancel currents through the diodes. The offset dynamic range is so set from 0 to $2I_{typ}$. Once the diode current $\overline{I_{ATT1}}$ is cancelled at the minimum gain, its value is saved and the control interface switches the gain to its maximum value to save its second value when $\overline{I_{ATT1}}$ is cancelled.

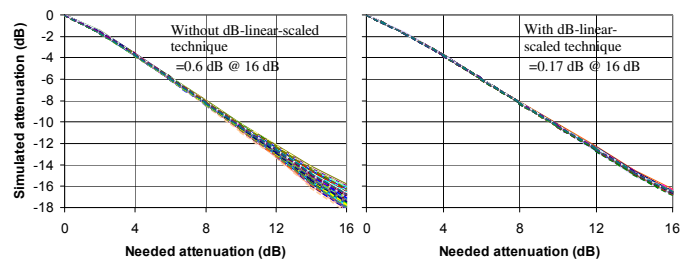


Fig. 7 Attenuation level at 10 GHz for 100 Monte-Carlo runs

By using this original technique, gain variation is lowered to ± 0.17 dB at 1σ for 16 dB of attenuation with a 4-bit shift register (Fig. 7). This value is almost two times smaller with a 6-bit shift register and a little more with an ideal one. This original technique is part of a THALES patent pending.

VI. CONCLUSION

An original structure based variable gain X-band amplifier (VGAs) in SiGe technology is presented. Thanks to the use of two VGAs and a passive attenuator, both linearity ($P_{in,dB} > 8$ dBm) and high dynamic range (> 30 dB) are achieved. Moreover peaking technique and an original approach based on feedback are introduced to drastically improve frequency bandwidth to 8.35 GHz with good attenuation response. Finally, an original technique to improve reproducibility versus attenuation is presented.

REFERENCES

- [1] Kyu-Sung Chae and Chang-Woo Kim “Monolithic SiGe HBT Variable Gain Amplifiers with a Feedforward Configuration for 5-GHz Applications” IEEE SiRF 2006.
- [2] Benjamin Sewiolo, Georg Fischer and Robert Weigel “A 15GHz Bandwidth High Efficiency Power Distributed Amplifier for Ultra-Wideband-Applications Using a Low-Cost SiGe BiCMOS Technology” IEEE SiRF 2009.
- [3] Kenichi Ohhata, Totu Masuda, Eji Ohue, Katsuyoshi Washio “Design of a 32.7-GHz Bandwidth AGC Amplifier IC with Wide Dynamic Range Implemented in SiGe HBT” IEEE Journal of Solid-State Circuits, VOL. 34, NO. 9, August 1999.