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# Design of a X-band GaN oscillator: from the low frequency noise device characterization and large signal modeling to circuit design

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**Abstract** — Although GaN technologies were initially developed for solid state source amplifiers, it was recently demonstrated that AlGaIn/GaN HEMT transistors were also suitable for low noise applications such as LNA [1]. The frequency synthesis is not yet widely explored for these technologies. In this paper the design of a low phase noise X-Band oscillator is proposed. The low frequency noise performance and the residual phase noise, as well as dynamic S-parameters were carried out on AlGaIn/GaN HEMT grown on SiC. A large-signal modeling technique is also presented. The reduced complexity and the good accuracy of our large signal model permits an efficient circuit design, without intensive knowledge of the technological device parameters. These characterization and modeling tools are used for the design of an 1-stage oscillator working at 10 GHz delivering 20dBm.

**Index Terms** — AlGaIn /GaN HEMT large-signal modeling, Low Frequency Noise, Low phase noise oscillator.

## I. INTRODUCTION

AlGaIn/GaN field effect transistor offers excellent potential for microwave applications. The high band-gap of GaN (3.4eV) gives to AlGaIn/GaN devices a high robustness against external RF aggressions, thanks to their high breakdown voltage and good thermal conductivity. Moreover, high microwave output power levels are useful to reduce the PA's design complexity, while these devices also take benefit from low noise figures at high frequency for LNA's design. This high power levels handling can also avoid the integration of any amplification buffer at the oscillator output to optimize the mixer compression gain. Moreover the devices good layer quality was reported in numerous papers thanks to low frequency noise (LFN) characterization. Therefore these devices can be used to design low phase noise non-linear circuits such as oscillators.

This paper presents the design of a hybrid oscillator at X-Band based on the study of noise mechanisms in the transistor and the large signal modeling of the device. LFN characterization of the devices was used to identify the impact of structural defects in devices grown on sapphire, Si and SiC substrates [2]. In section II the LFN performance of AlGaIn/GaN HEMT on SiC substrate is investigated, as well

as the residual phase noise. The best bias conditions are defined to design the low phase noise oscillator circuit. Our criterion is to minimize the LFN, which is afterwards converted around the carrier signal. The section III is dedicated to the development of an original method for large signal modeling of GaN devices, allowing a fast model implementation. Then, these two former tools are used in section IV dealing to the design of a low phase noise oscillator.

## II. LOW FREQUENCY NOISE AND RESIDUAL PHASE NOISE IN ALGAN/GAN HEMT ON SiC SUBSTRATE

HEMT devices are grown by MOCVD on silicon carbide substrate. The aluminum content in the barrier layer is 24%. The devices are processed using the AlGaIn/GaN HEMT TIGER usual process [3]. Static and pulsed measurements are performed respectively with HP4142 modular source and DIVA D225 system over a large number of devices. A good manufacturing yield and homogeneity of the electrical performances is noted over the wafer with a dispersion lower than 15% on all the parameters.

Substrate type	SiC
$I_{DSS}$ (saturation drain current, mA/mm)	1000
$V_T$ (threshold voltage, V)	-5.5
Gm max (transconductance, mS/mm)	250
$I_G$ (gate leakage currents, $\mu$ A)	<0.1
$R_{ON}$ resistance (@ $V_{GS}=0V$ , ohmic regime, $\Omega$ )	25
Ft and Fmax (GHz)	40-100

TABLE 1: HEMT (0.25x2x75  $\mu$ m<sup>2</sup> gate area) static and dynamic parameters (mm unit refers to the normalization versus the gate width of the devices).

Scattering parameters measurements are performed with HP8510 network vector analyzer. Table 1 shows the main electrical parameters of 0.25x2x75  $\mu$ m<sup>2</sup> devices. These HEMT on SiC exhibit high drain current, high transconductance and low gate leakage current as well as reduced contact and  $R_{ON}$  channel resistances highlighting the good process maturity.

A and B next sections present the low frequency noise performances in ohmic and saturated regimes respectively. Section C reports the residual phase noise measurement.

### A. Technological maturity

The  $\alpha_H$  Hooge parameter is obtained using Peransin's technique [4]. This figure of merit can only be extracted from devices that exhibit close to perfection  $1/f$  spectra [1] and is useful for technological comparisons. A maximum value of  $\alpha_H=5.10^{-5}$  is found for our AlGaIn/GaN HEMTs grown on SiC substrate [1]. This figure of merit for devices on SiC substrate is better compared to measurement of devices grown on sapphire and silicon substrates (resp.  $\alpha_H=1.10^{-4}$  and  $\alpha_H=5.10^{-3}$ ). The measured  $\alpha_H$  on silicon carbide involves that this technology is close to the state of the art even for more mature device technologies.

### B. Low frequency noise under saturated regime.

The low frequency noise (LFN) behavior under saturated bias conditions is similar to the corresponding oscillator phase noise. This measurement is therefore determinant for the oscillator design.

The measurement is performed in the 10 Hz-1 MHz frequency range using the trans-impedance amplifier technique. This setup allows simultaneous drain and gate spectral density measurement (resp.  $S_{ID}$  and  $S_{IG}$ ), as well as cross-correlation measurement. The correlation between the input and output noise sources is found to be null.  $S_{IG}$  contribution is very low due to weak leakage currents. Hence  $S_{IG}$  does not impact on the overall noise in circuits such as oscillators.

Figure 1 shows a typical noise spectrum that evidences the presence of numerous trapping-detrapping centers i.e. generation-generation (GR) phenomenon and a flicker  $1/f$  contribution. The closeness of the GR hinders their extraction. Analytical extraction procedure (using MatLab software) was developed to get the different contributions of the noise parameters. Then two kinds of GR centers are found.

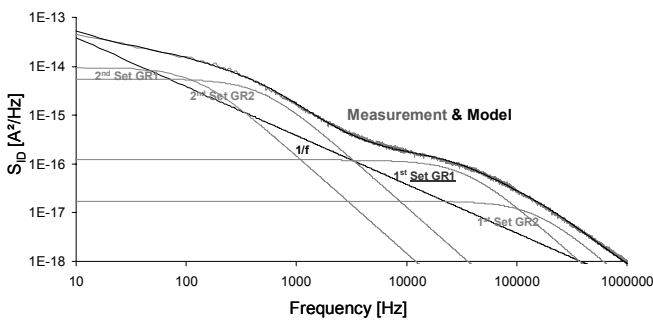


Fig. 1. Extracted low frequency noise sources and overall spectrum ( $0.25 \times 2 \times 75 \mu\text{m}^2$  HEMT @  $V_{GS}=-2$  V,  $V_{DS}=16$  V)

The first set of GR centers is due to defects at the AlGaIn/GaN interface under the gate. The figure 2 shows that their cut-off frequencies and magnitudes depend on the DC power (and so, with the channel's temperature).

The second set of GR centers is activated with the gate voltage  $V_{GS}$  bias. Once removed the GR contribution from the first set this second trapping phenomenon originates from defects in the GaN volume. Physical simulations of the devices show that decreasing  $V_{GS}$  from zero down to the pinch-off voltage (the Fermi level decreases) induces the quantum well zone to widen in the GaN layer (the conduction band bows down). Moreover when  $V_{GS}$  decreases the piezoelectric field (from AlGaIn to GaN at the interface) is strengthened by the electric field due to  $V_{GS}$  bias. The carrier distribution is swept away from the AlGaIn/GaN interface. The trapping-detrapping centers are then located in the GaN volume.

This LFN study enables to adjust the quiescent point of the transistor to get the appropriated low frequency noise and dynamic gain performance for the oscillator design.

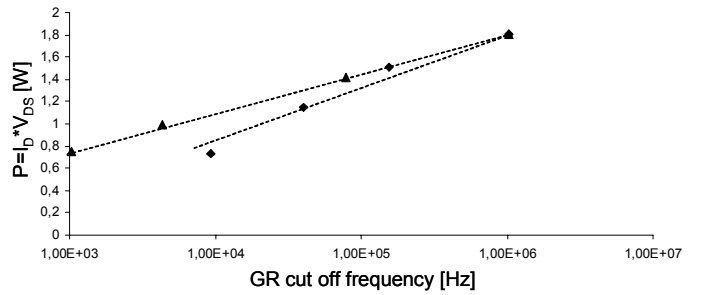


Fig. 2. Evolution of the cut-off frequency of the first GR set (here GR1 from figure 1)  
▲:  $V_{GS}=0$  V and  $V_{DS}$  varies; ◆:  $V_{GS}$  varies and  $V_{DS}=10$  V

### C. Residual phase noise

The LFN conversion around the carrier is a well known phenomenon, even if the RF noise floor can also play a strong contribution to the overall converted noise, especially for frequencies far from the carrier. The following graph (figure 3) is related to the residual phase noise measured at 10 GHz on a  $0.25 \times 2 \times 75 \mu\text{m}^2$  device. The transistor is used in its amplification mode. The input power issued from the high spectral purity source is -10 dBm, and the HEMT runs in its small signal regime.

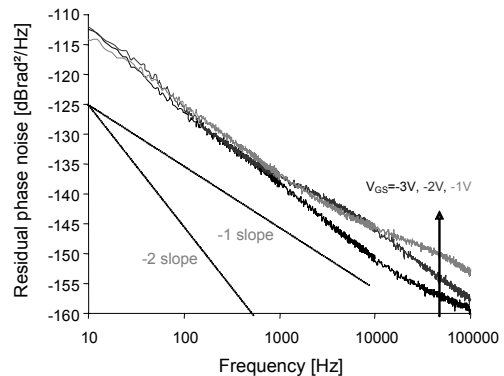


Fig. 3. Residual phase noise of a  $0.25 \times 2 \times 75 \mu\text{m}^2$  gate width transistor @ 10 GHz ( $V_{DS}=10$  V,  $V_{GS}$  varies from -3V to -1V).

The residual phase noise frequency dependence is not monotonous. The G-R magnitude and frequency are once again found to depend strongly with the bias conditions and temperature as for LFN spectra. The residual phase noise is found to improve under increase input power (i.e. transistor's compression) due to the non-linearity conversion into the device. This measurement gives pertinent indications for the bias of the transistor for an optimized oscillator phase noise.

### III. LARGE SIGNAL MODEL

The transistor large signal model is usually based on the knowledge of a large set of parameters [5]. From the numerous large signal models available in CAD simulators no model fits for our GaN HEMT devices (due to the difficulty to get together a good behavior on the transconductance shape, the ohmic resistance, etc). Thus our own non-linear model is developed. It is based on an intuitive technique making use of a reduced set of parameters, without any need about technological parameter knowledge.

The next paragraphs present the main steps leading to the set up of the model used for the oscillator design.

#### A. Voltage controlled Current source model setup

The LFN and the dynamic S-parameters measurements are used to get the better compromise for the oscillator quiescent point, that is found at  $V_{GS} = -3$  V and  $V_{DS} = 10$  V. Pulsed measurement is performed under these 'hot' bias conditions to get the right output characteristics using a pulse length  $\delta t = 0.1$   $\mu$ s and a pulse separation  $T = 0.5$  ms. Then the current source model is achieved using mathematical expressions based on Fager model [6] that is suited for the ohmic regime description of the device. Important care is brought to these analytical expressions being derivable up to three times at least to ensure the exactness of the controlled source model when used in harmonic balance simulation. The figure 4 illustrates the whole model.

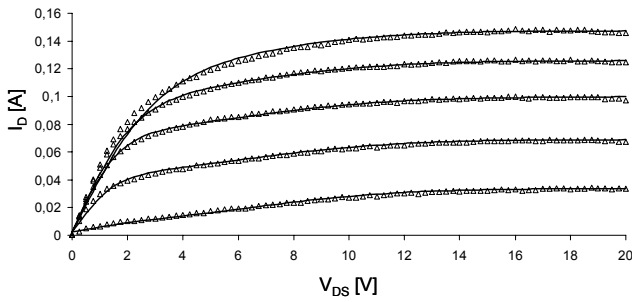


Fig 4 0.25x2x75  $\mu$ m<sup>2</sup> HEMT output pulsed characteristics ( $\delta t = 0.1$   $\mu$ s,  $T = 0.5$ ms) for gate-source voltage varying from  $V_{GS} = 0$  V to  $V_{GS} = -4$  V (Bias condition:  $V_{GS} = -3$  V,  $V_{DS} = 10$  V, Measurement :  $\Delta$  and Simulation: —)

$$I_D = (I_{Fager} + I_{correction}) * K_{correction} \quad (1)$$

$I_{Fager} = I_S(V_{GS}) * \tanh(P_S(V_{GS}) * V_{DS})$  allows to fit the ohmic region from figure 4, with  $I_S(V_{GS})$  and  $P_S(V_{GS})$  polynomial expressions.

$I_{correction} = A_P * \tanh(P_P * (V_{DS} - V_{TP}) + A_P)$  is a correction term to get the good saturated current level, where  $A_P$ ,  $P_P$ ,  $V_{TP}$  are fitting parameters.

$K_{correction} = A_C * \tanh(P_C * (V_{GS} - V_{TC}) + P_C)$  permits to have at least seven times derivable  $I_D$  expression to make the model suitable for the oscillator simulation with harmonic balance simulation.

Excellent agreement is found between the simulation and the measurement both on the output characteristics (figure 4) and  $I_D(V_{GS})$  curves.

#### B. Small signal model

The extrinsic parasitic elements (pad capacitances, series resistances and inductances) are evaluated using the method developed by Dambrine [7]. The drain and gate pad capacitances can be extracted from Y-parameters at a gate voltage below the pinch-off. Next, the parasitic resistances and inductances are extracted under positive  $V_{GS}$  bias conditions ( $V_{GS} = +3$  V) where the capacitances do not influence on the extraction. The small-signal model gives accurate results for  $I_D$  ranging from 20 mA (@  $V_{GS} = -4$  V) to 100 mA (@  $V_{GS} = 0$  V). An illustration is given on figure 5.

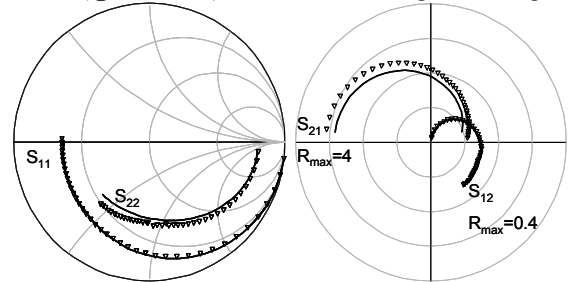


Fig 5. 0.25x2x75  $\mu$ m<sup>2</sup> HEMT S-parameters from 40 MHz to 40 GHz ( $V_{GS} = -3$  V  $V_{DS} = 10$  V, Measurements:  $\Delta$ ; Simulation: —)

#### C. Large signal model – compression point $P_{1dB}$

The figure 6 shows the large signal device excursion behavior from the 'hot' quiescent point. The 1 tone compression of the transistor is in good agreement with experience. The output power  $P_{OUT}$  is plotted versus the input power  $P_{IN}$  for a HEMT featuring 0.25\*2\*75  $\mu$ m<sup>2</sup> HEMT.  $P_{OUT}$  discrepancy is due to the technological dispersion of the transimpedance. This measurement was performed on an older device, for which  $g_m$  was 4% below. However a good agreement is still found. The compression occurs for an output power  $P_{1dB} = 19$  dBm.

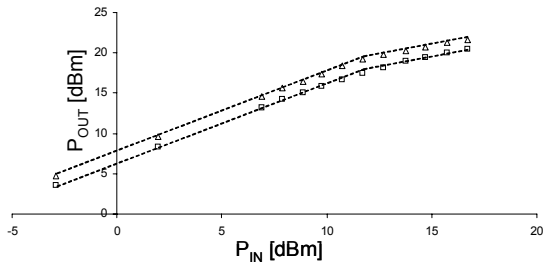


Fig. 6.  $P_{OUT}$  vs  $P_{IN}$  (@10 GHz); Measurement:  $\square$ ; Simulation:  $\Delta$ .

#### IV. X-BAND OSCILLATOR

This section is focused to the design of a X-Band oscillator using microwave integrated circuit (MIC) technology.

##### A. MIC Circuit Design

The MIC circuit makes use of microstrip lines on cuflon substrate ( $\epsilon_R=2.1$ ,  $\tan(\delta)=4.5 \cdot 10^{-3}$ ). A common-source oscillator structure is designed with an open microstrip line for the resonator on the gate. Bonding wires are used to connect the transistor accesses to the microstrip lines. The starting oscillation conditions in this common-source configuration are obtained thanks to the negative resistance on the gate ( $S_{11}$ ). However when the  $S_{11}$  gain is maximal an undesirable negative resistance also appears due to the bonding wire inductances. By shifting the oscillation conditions towards a lower  $S_{11}$  gain zone (figure 7),  $S_{22}$  can be adjusted to a value below one. Therefore a classical output matching network can be used.

The figure 6 shows a moderate power saturation beyond the compression leading to high voltage gate control value out of the model validity (more than 10 V peak-to-peak swing on the gate). For these reasons, the limitation of the negative resistance on  $S_{11}$  is a key point for such a design.

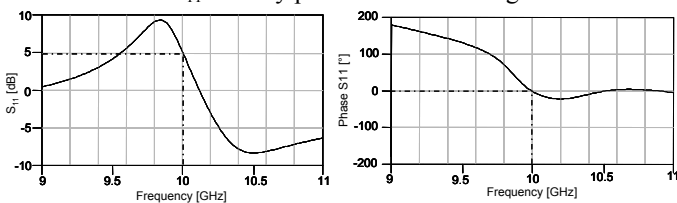


Fig. 7. Gain and phase simulation – The dashed lines present the starting conditions for the oscillator design.

##### B. Oscillator performance

The Figure 8 shows the measurement results of the X-Band oscillator. The inset of figure 8 shows a 20 dBm output power measured close to 9.9 GHz, but a poor 2<sup>nd</sup> harmonic is found at -10 dBc, while the third harmonic is rejected more than -30 dBc from the carrier. The phase noise is measured using a spectrum analyzer around -105 dBc/Hz @ 100 kHz from the carrier. The pushing and pulling factors are simulated

respectively at 600 kHz/V and 370 MHz (open-short termination circuits).

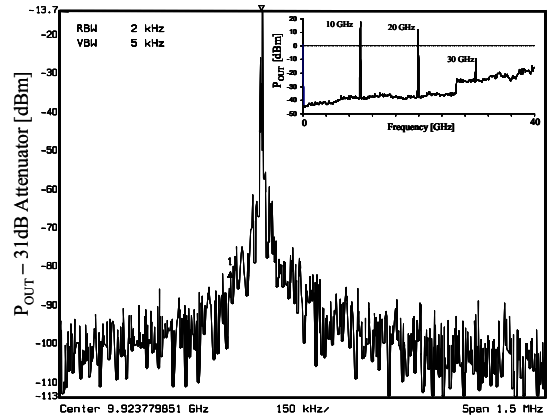


Fig. 8. Oscillator output power versus frequency ( $V_{GS}=-3$  V  $V_{DS}=10$  V), measurement with 31 dB attenuator value. A measurement between 0 and 40 GHz is presented in the inset.

#### V. CONCLUSIONS

A high power X-Band oscillator using AlGaIn/GaN HEMT is proposed. The design starts from the device low frequency noise and residual phase noise characterization to large signal modeling. Then the circuit is designed based on this concept. The original large signal modeling technique used provides to the designers an accurate ‘easy to build’ model, without any knowledge about the technological process. This approach is suitable for many RF design applications when no accurate model is available.

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#### REFERENCES

- [1] J.G.Tartarin et al., “Low frequency and linear high frequency noise performances of AlGaIn/GaN grown on SiC substrate,” *GaAs2005*.
- [2] J.G.Tartarin et al., “Low frequency noise of AlGaIn/GaN HEMT grow on  $Al_2O_3$ , Si and SiC substrates” *18<sup>th</sup> international conf. on noise and fluctuations ICNF 2005 published in American institute of physic*, pp. 399-402
- [3] A. Minko et al., “AlGaIn-GaN HEMTs on Si with power density performance of 1.9W/mm at 10GHz”, *IEEE Trans. Electron Device Lett.*, Vol. 25, N°7, pp.453-455, July 2004.
- [4] J.M. Peransin et al., “1/f noise in MODFET’s at low drain bias” *IEEE Trans. on Electron Devices*, vol. 37, No 10, October 1990, pp. 2250-2253
- [5] I. Angelov et al., “On the Modelling of High Frequency and High Power Limitations of FETs”, *Integrated Non-linear Microwave and Millimetre-wave Circuits (INMMiC) Workshop*, Roma, Italy, 4 p., 15-16 November 2004
- [6] C. Fager et al., “Prediction of IMD in LD MOS Transistor Amplifiers using a new large-signal model” *IEEE Microwave Theory and Technique 2002*, pp. 2834-2842
- [7] G. Dambrine et al., “A new method for determining the fET small-signal equivalent circuit” *IEEE Trans. On Microwave Theory and Technique*, Vol. 36, N°7, pp. 1151-1159, July 1988.