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Trapping Related Degradation Effects in AlGaIn/GaN HEMT.

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Abstract— Reliability in GaN based devices still motivates numerous studies because the involved degradation mechanisms are different from that in III-V narrow bandgap devices. Direct investigations on high electron mobility transistors (HEMT) are performed with low frequency noise (LFN) measurements and pulsed electrical characterization. Undoped AlGaIn/GaN devices grown on silicon substrate are stressed at a junction temperature of 175°C. Gate-lag and drain-lag measurements method have been performed versus different quiescent bias points and under different pulse conditions. This method allows the discrimination of each lag phenomenon as well as the thermal contribution. Thus it is possible to track and model the trapping mechanisms versus bias conditions. This electrical modelling is completed with LFN measurements, which is largely used for reliability investigations.

I. INTRODUCTION

AlGaIn/GaN high electron mobility transistors (HEMT) stand as an interesting solution to substitute GaAs and SiGe technologies for power and high frequency applications. They take advantages from higher breakdown voltage, higher power density, higher thermal conductivity and from very good low noise capabilities [1]. Hence, GaN devices can pretend to be used in integrated transceivers for power amplification, low noise amplification, frequency synthesis and mixers.

From now on, reliability studies are on going to develop behavioural models and to focus on the degradation trends (drift in power, PAE) under RF, DC or temperature stress [2]. Among the available solutions of characterization, we later on present a method making use of I(V) electrical and low frequency noise (LFN) measurements. The crossed interpretations of data issued from these characterizations are suitable to extract and model trapping phenomena related to lag effects. These two different techniques are next used to evaluate traps related degradation on devices which have been stressed under high junction temperature conditions (175°C) during 2000 hours. LFN and I(V) pulsed measurements are applied to stressed devices and test samples. A gate-lag and drain-lag extraction method is developed to evaluate and discriminate the nature of trapping effects as well as their evolution before and after stress. The

structural defects evolution is also investigated under ohmic and saturated biasing conditions.

HEMT devices are grown by MOCVD technique on silicon substrate using the AlGaIn/GaN HEMT UMS usual process. Transistors feature 0.25*8*125 μm^2 gate area, 27% alumina content and non-intentionally doped layers.

II. GATE-LAG AND DRAIN-LAG CHARACTERIZATION

This method is based on I(V) pulsed measurements at specific quiescent bias point to discriminate gate-lag and drain-lag phenomena from self-heating effects. The pulse duration is chosen as short as possible (0,1 μs) in order to limit self-heating, and the period between pulses is set to 50 ms.

Preliminary static measurements are performed, featuring an average degradation of 40% on I_{DSS} before and after the application of the stress.

A. Gate-lag modelling

Pulsed I(V) characterization is realized thanks to DIVA D210 commercial setup (figure 1 a). A current probe has been added to observe the shape of the pulses of drain current in time domain (using an oscilloscope, figure 1 b).

Firstly, in order to remove self heating effects at the quiescent bias point, $V_{\text{GSquiescent}}$ varies from -10 V to $V_{\text{pinch off}}$ (-4 V) while $V_{\text{DSquiescent}}$ remains constant ($P_{\text{DCquiescent}}=0$ W on the given V_{GS} range).

Then, $I_{\text{DS}}(V_{\text{DS}})$ for different V_{GS} are used to extract gate-lag behaviours when drain-lag contribution is neglected: the procedure consists in extracting the data at $V_{\text{DS}}=V_{\text{DSquiescent}}$ (figure 2) which represents the only point where the only lag contribution comes from the gate.

The two methods illustrated on figure 1 lead to identical linear trend of the lag effects on the gate access (figure 2): moreover, time domain study is useful to assess the shape of the pulse response, as lag effect can be attributed to time constant (RC) or to pulse level modification (fixed charges). Thus, these later time graphs indicate that the lag is not attributed to RC time constant but to fixed charges in the structure. As V_{GS} is shifted while V_{DS} remains constant, both V_{DG} and V_{GS} can be

invoked to locate the fixed charges respectively between drain and source or gate and source, and LFN measurements will next be used to locate these traps. Tunnelling related effects will be discussed in the extended version of the paper.

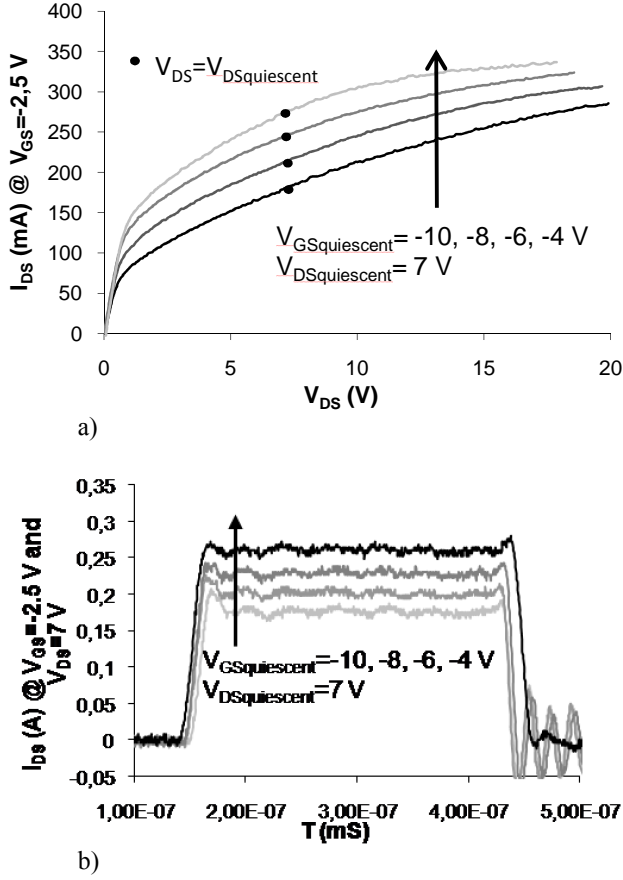


Fig. 1. Pulsed measurements: a) classic I(V) curves for different $V_{GSquiescent}$. b) time domain characterization of I_{DS} pulses at $V_{DS} = V_{DSquiescent}$ for different $V_{GSquiescent}$.

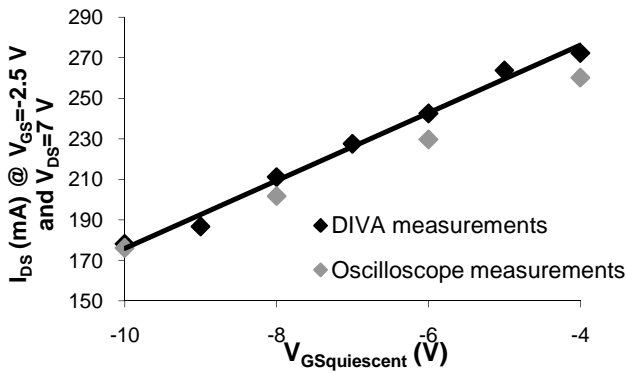


Fig. 2. Gate-lag evolution versus $V_{GSquiescent}$: extracted from pulsed measurements (from classic I(V) and time domain measurements).

On figure 3 are plotted gate-lag curves which are extracted from pulsed I(V) for a test sample and a stressed device. These graphs are normalized versus the I_{DSS} of each device. Gate-lag related traps are more sensitive after the application of the stress, as the slope of the variation increases for these devices.

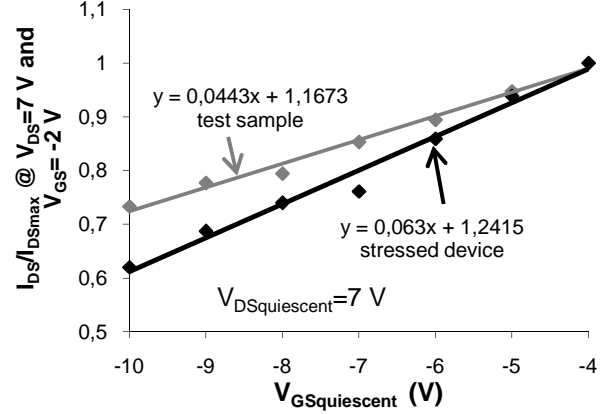


Fig. 3. Normalized gate lag evolutions extracted from pulsed I(V) for a test sample and for a stressed device.

B. Drain-lag

Pulsed I(V) measurements are performed to evaluate drain-lag. For that purpose, $V_{GSquiescent}$ is kept at a constant value while $V_{DSquiescent}$ varies from 0 V to 15 V. Moreover, $V_{GSquiescent}$ is set at $V_{pinch\ off}$, so that $P_{DC} = 0$ W (no thermal effect): however gate-lag effects also contribute to the overall lag signature. This problem can be removed by deembedding the gate lag contribution using the previous gate-lag model (at $V_{DSquiescent} = 7$ V only, for figure 3) for both the test sample and the stressed device.

In a first step, measurements are carried out with a pulse period of 50 ms (as for gate-lag characterization). Normalized I_{DS} currents versus I_{DSS} are presented in figure 4.

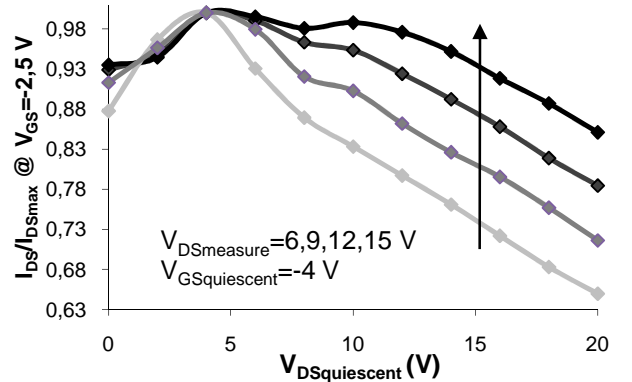


Fig. 4. Drain-lag representation extracted from pulsed I(V) measurements with a pulse period of 50 ms.

As the $V_{DS_{\text{quiescent}}}$ (x-axis) value at the maximum of I_{DS} do not corresponds to the equivalent value of V_{DS} measured, it is assumed that no drain lag effects occur in the devices. Moreover, the monotonous decrease of each plot whatever the V_{DS} quiescent point also eliminates any drain lag origin for the current trends. Some hypothesis about hot electrons effects [3] activated at high V_{DG} (i.e. at high quiescent bias point) can be drawn, which explain the gate dominating effect upon the drain lag contribution.

Other studies at lower T pulse periods are performed to reveal drain-lag phenomenon: reducing T to 1 ms limits the hot electrons related effects, and allows tracking the drain-lag effects (relaxation times in GaN devices are known to cover a large range of time, and thus T reveals different phenomena) (figure 5). In this new case of study a maximum of drain current is observed when $V_{DS}=V_{DS_{\text{quiescent}}}$ for the test sample (figure 5.a). A larger evolution from part to part of the maximum I_{DS} can be noticed for the stressed device in comparison with the test sample, once again revealing the evolution of traps mechanisms during the application of a thermal stress.

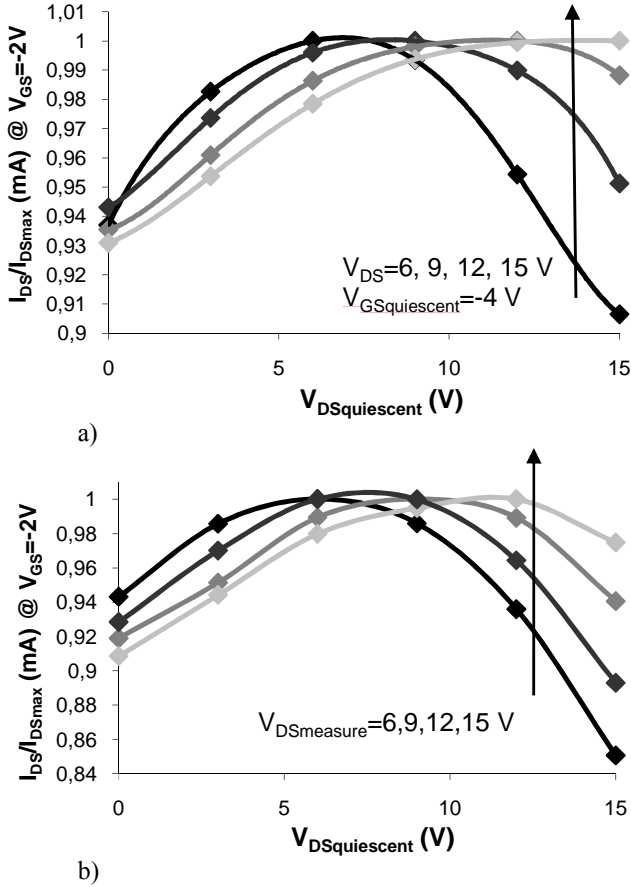


Fig. 5. Drain-lag representation extracted from pulsed $I(V)$ measurements with a pulse period of $T=1$ ms: a) test sample and b) stressed device.

III. LOW FREQUENCY NOISE

Low frequency noise is largely used as a diagnostic tool to evaluate and locate defects in the structure. The evolutions of the LFN signatures are also powerful to track the evolution of the defects at different periods of the stress. In this study we focus on evolution of the noise spectra under ohmic and saturated biasing conditions. Measurements are carried out using a transimpedance amplifier direct measurement technique which allows rapid LFN measurements of S_{ID} , S_{IG} , and the correlation coefficient over a wide frequency range (from 1 Hz to 100 kHz).

A. Ohmic biasing conditions

The low frequency noise spectrum of the test sample exhibits a $1/f$ trend at $V_{GS}=0$ V superimposed with GR centers in the upper frequency band. When V_{GS} decreases down to the pinch-off voltage, a stronger contribution of several GR appears (figure 6).

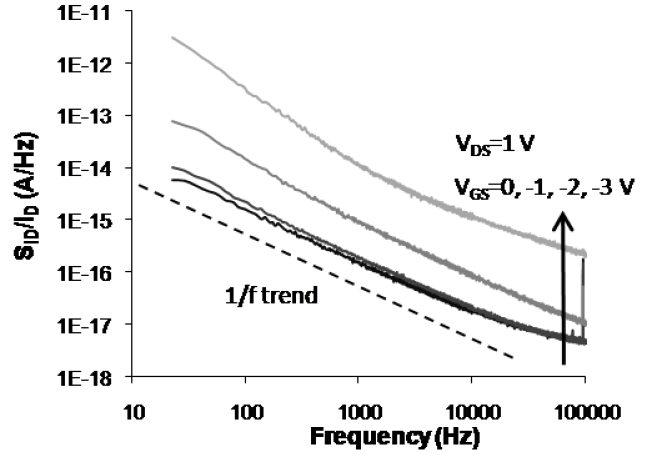


Fig. 6. Low frequency noise spectra of the test sample under ohmic biasing conditions.

At $V_{GS}=0$ V, the stressed devices spectrum features a $1/f^\gamma$ trend ($\gamma=1.11$). Numerous GR centers appear when the device is pinched (figure 7). The discrimination of the noise sources is realized using robust homemade extraction software [4]. Up to 3 GR per frequency decade can be extracted with 5 % accuracy.

Comparing figure 6 and 7, we notice the degradation of $1/f$ noise with an increase of the frequency index γ after the application of stress. The higher level of $1/f$ flicker source for the stressed devices masks the GR centers signatures. As γ is usually related to process maturity ($\gamma \neq 1$ stands for non mature technologies), it can be assumed that the structural integrity of the layers are degraded under the application of the thermal stress.

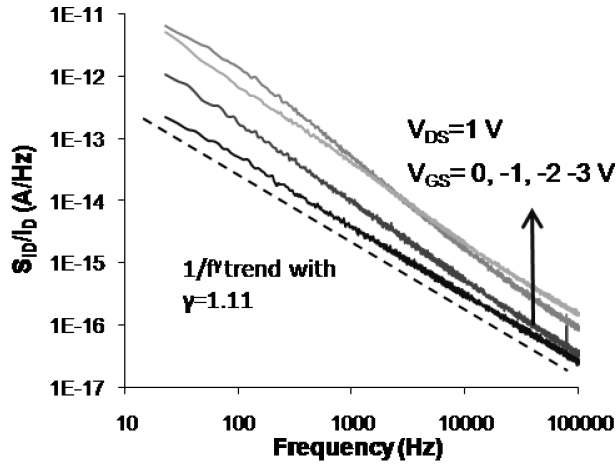


Fig. 7. Low frequency noise spectra of stressed devices under ohmic biasing conditions.

B. Saturated biasing conditions

Under saturated biasing conditions (figures 8 and 9), the observations lead to the same conclusions: we observe a degradation of the $1/f$ noise source, associated with an increase of the frequency index ($\gamma=1.11$). The cut off frequencies of GR centers drift toward high frequencies, attributed to a change of the time constants of the traps previously located in the GaN bulk. The LFN spectra have been measured over a wide range of biasing conditions, and both the $1/f$ and the GR noise sources have been extracted. From this extensive characterization campaign on stressed devices and on sample device, it is thus possible to locate the defect in the drain-gate region, and specially in the 2DEG GaN layer (bulk and AlGaIn/GaN interface).

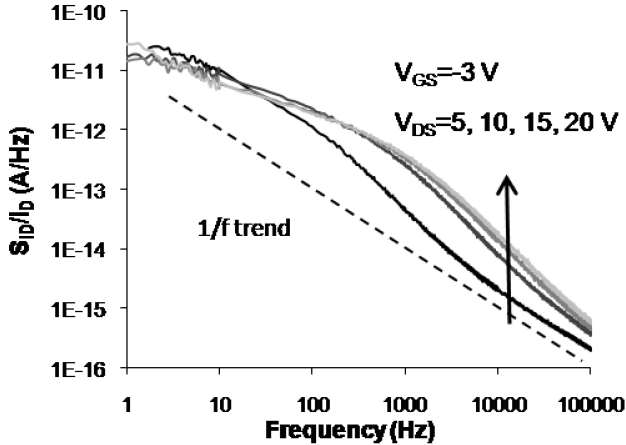


Fig. 8. Low frequency noise spectra of test sample under saturated biasing conditions.

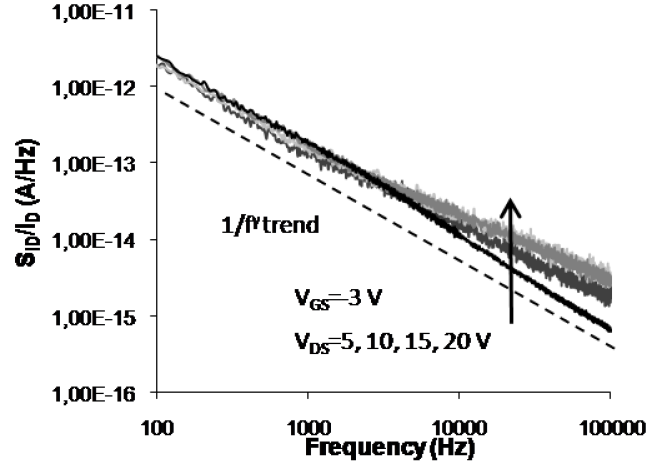


Fig. 9. Low frequency noise spectra of stressed device under saturated biasing conditions

The lower frequency is decreased down to 1 Hz for the test sample to allow the extraction of GR centers sensitive at lower frequencies, while this frequency is set to 100 Hz for stressed devices because of the single $1/f^{\gamma}$ noise source contribution.

IV. CONCLUSION

We have proposed a characterization of AlGaIn/GaN HEMT devices with electrical and low frequency noise measurements setups: from $I(V)$ pulsed measurements, gate-lag and drain-lag behaviours have been extracted under different pulse periods conditions. The stressed devices feature larger lag effects than the sample devices. LFN measurements have revealed numerous GR centers for the test samples, while these GR become less sensitive on stressed devices because of the large increase of the $1/f^{\gamma}$ noise source: moreover a change on the frequency index $\gamma=1.11$ reveals a degradation of the GaN material between gate and drain accesses.

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