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An athermal measurement technique for long traps characterization in GaN HEMT transistors.

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Abstract

GaN High Electron Mobility Transistors (HEMTs) is very promising for high power switching and radiofrequency operation. However, the lack of reliability feedback is one of its major drawbacks. Trapping effect especially is one of the main performance limitations of such components. Many measurement techniques exist for trapping effects characterization, especially for short traps (μs to several ms). However for longer time constants, self-heating may distort the measurements. This paper presents an electrical and athermal transient measurement method which has been developed to study the trapping and detrapping time constants of such components. It allows the extraction of long transients without self-heating problems and is usable in long term electrical stress experiments. A simulation of this method with a simplified component's model and the measurements results are presented. With this technique, we investigated especially the long time constants ($\tau > 20$ ms) over a range of temperature from 10°C to 90°C . We observed three thermally activated trap signatures on GaN devices with our method.

Keywords- slow transients, traps, GaN, High Electron Mobility Transistors (HEMTs).

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1. Introduction

High band gap semiconductor devices such as AlGaN/GaN High Electron Mobility Transistors (HEMT) are promising for RF power and high-voltage switching applications [1]. However, the main limitation of its performance is the trapping effect, appearing before and during its operating lifetime [2, 3, 4]. One of its principal consequences is the current collapse: a recoverable reduction in drain current after the application of a high voltage. These trapping effects in GaN HEMTs have a slow nature. The recovery time from current collapse can be long for these devices (>100s to several days) [3, 5, 6]. This phenomenon is thus critical in the component's applications i.e RF systems or power electronics.

A variety of techniques already exist in order to measure this phenomenon like C-DLTS [7] but this technique is not always suitable for studying this kind of semiconductor devices [8, 9], the capacities to measure being very small and to measure in a short time. The other existing techniques like I-DLTS, DLOS or low frequency noise measurements [10, 11, 12, 13] give a lot of information but (as DLTS) are not easily incorporated in long-term electrical stress experiments. Some methods such as transient measurement are promising for their use in long-term electrical stress [8, 14] but self-heating effects may distort the signal, even for relatively low currents. A correction of this effect is possible using the thermal resistance [15].

In this paper, we present an alternate way of characterizing the trapping time constants without thermal effects. This athermal transient measurement technique is used to analyze the slow detrapping ($\tau > 20\text{ms}$) behavior of GaN HEMTs. It is also usable with in-situ setup in long-term stress experiments. This method allows a measurement in the saturation or ohmic region without self-heating problems.

2. Methodology

Our method consists in a transient measurement in pulsed mode between two equilibrium states (figure 1) in order to study slow transients in the saturation or ohmic region without the occurrence of self-heating: The thermal time constant being around $150\ \mu\text{s}$. The signals on the drain and the gate are generated via an IV measurement bench from AMCAD Engineering. The image of the drain current is then retrieved using the voltage drop of a shunt resistance of low value ($0.5\ \Omega$). In order to only extract the current in the pulses, we developed an electronic card with instrumentation amplifiers and a sample and hold circuit.

Regarding the span of the transient (from several microseconds to 1000s), the use of the sample and hold device doesn't visibly distort the signal.

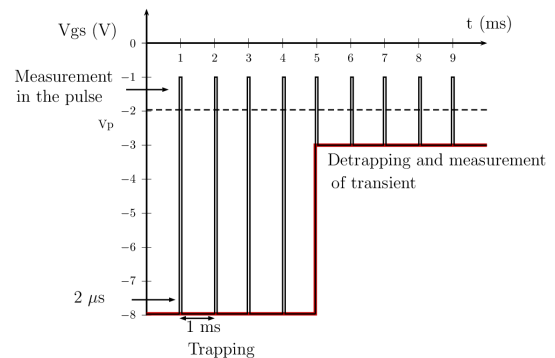


Fig. 1. Methodology of measurement: Signal applied on the gate of the transistor. The drain bias is fixed at 10 V or 0.5V, depending on the location of traps to measure.

Regarding the measurement in itself, the transistor is first pulsed from an OFF-state at $V_{gs} = -8\text{V}$. The pulsed measurement is at $V_{gs} = -1\text{V}$, -1.9V (close to the pinch-off) or 0V and the drain bias is

fixed at $V_d = 10V$ or $0.5 V$ depending on the location of traps to measure: in the saturation region for buffer traps or in the ohmic region for surface traps. The trapping state is held for a relatively long period of time, ensuring the same initial state for all measurements. Then, the device is pulsed from a less negative state, also below the pinch-off voltage at $V_{gs} = -3V$ with the same high voltage, ensuring the emission of traps. The measured detrapping time constants are then between several ms to 1000s.

The measurements are done in a range of temperature from 283K to 363K and the time constants are then extracted using a multiexponential model. For each temperature, we extract the number of defects to add in the model using the Prony algorithm, giving one exponential and starting coefficient for each defect. We then use a Levenberg-Marquardt algorithm in order to extract the corresponding time constants [17].

The devices on which this study is conducted are AlGaIn/GaN HEMTs powerbars with a $0.5\mu m$ gate length and 25W output power.

3. Simulation of the measurement method

In order to be sure that the pulsed measurement doesn't interfere with the course of trapping and detrapping of the defects, we developed a simulation of the component with ADS. The intrinsic current source is modelled through a hyperbolic tangent equation and adjusted in order to correspond with pulsed IV measurements on the transistor. The thermal behavior is simulated via a thermal Ohm equation (Eq. 1):

$$T_j = R_{TH} * P_{diss} + T_c \quad (1)$$

T_j is the junction temperature, T_c the case temperature, P_{diss} the dissipated power and R_{TH} the thermal resistance. The R_{TH} and C_{TH} parameters are extracted using measurements of $I_{d_{ss}}=f(T_j)$ and $I_{d_{ss}}=f(t, P_{diss})$. Two thermal junctions were necessary in order to reproduce the thermal behavior given by the self-heating measurements. The variation of $gm=f(T_j)$ was also extracted in order to complete the electro thermal model.

The trapping and detrapping phenomena are included using a model given by Jardel et al [16]. A little modification is done in order to include a feedback of the case temperature and self-heating effects on the time constants values. This

temperature dependence in Arrhenius is set to values close to reality (between several ms and 100s, $E_a=0.58 eV$).

The pulsed gate signal is then integrated at the entry of the circuit. The method was simulated from 10 to 90 °C and the trapping and detrapping time constants were retrieved with the signal envelope and found in agreement with simulated values (figure 2) until $\tau < 20ms$. Below this value, the length of the pulses distorts the output visible time constant. This result confirms the absence of interference of the pulses on the measured time constants for $\tau > 20ms$.

Furthermore, the simulated channel temperature was extracted. The maximum temperature elevation

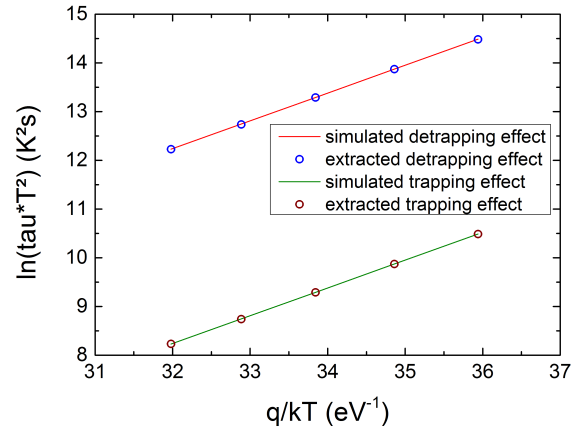


Fig. 2. Comparison between simulated and extracted values for trapping and detrapping phenomena.

was found to be of $0.3^\circ C$, the transistor being really in a stable thermal state due to the pulsed signal on the gate (with a 0.2 % duty cycle). We are then able to measure long trapping and detrapping effects at any polarization, i.e closer to standard current levels in the application, without thermal effects.

We also simulated the self-heating of the component for some of the polarization protocols used in the literature [2] for ON-state measurements. The high current levels induce critical self-heating ranging from $\Delta T=27 K$ for $V_{ds}=10V$, $V_{gs}=0V$ and 1s-pulse to $\Delta T=15.6 K$ for $V_{ds}=6V$, $V_{gs}=1V$ and 1s-pulse (fig 3). The resulting thermal effect is then very important and will deform the activation energies extracted, confirming the need for an athermal measurement technique or a correction of its effects [15].

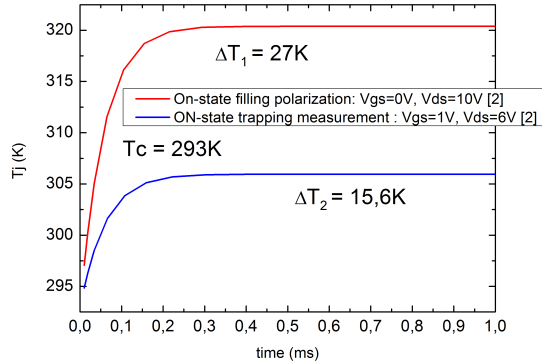


Fig. 3. Simulated self-heating effect of the component during ON-state filling pulse and ON-state trapping measurement.

The originality of this work is then to allow a trapping or detrapping measurement without self-heating effects, without restriction on power density.

4. Measurement results

The concept being validated with the simulation, we measured the detrapping time constants of several GaN HEMTs with $V_{ds}=0.5V$ and $V_{ds}=10V$ with our method. An example of drain current transient is presented on figure 4.

The measurements at $V_{ds}=10V$ presented three trapping characteristics activated at different

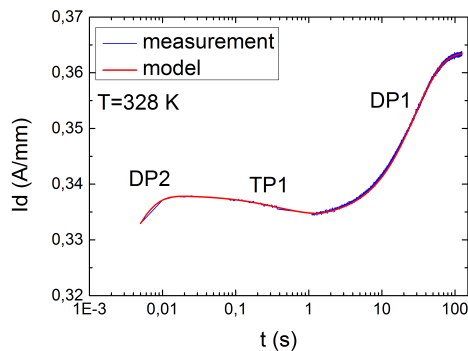


Fig. 4. Example of a measured transient envelope using the athermal technique. Two detrapping phenomena (DP1 and DP2) and a trapping phenomenon (TP1) are found.

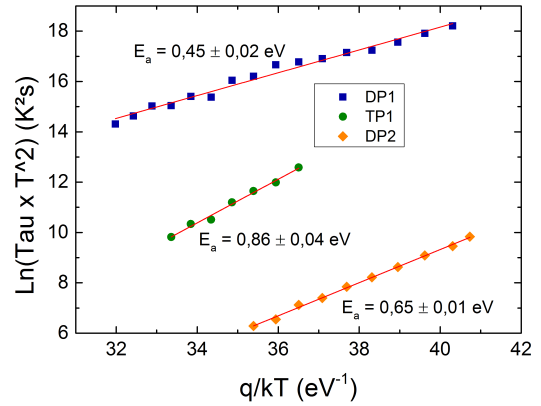


Fig. 5. Arrhenius plots of the measurement at $V_{ds}=10V$. Three defects are present.

temperatures. Two detrapping time constants (DP1 and DP2) at 0.45 eV and 0.65 eV and a trapping effect (TP1) at 0.86 eV were measured (fig 5). These activation energies are associated to C/O/H impurities for DP1 [18], VGa Oxygen complex for DP2 [19] and gallium vacancies for TP1 [20]. The full paper will present and discuss the results of these long trapping effects extraction in details. It will also present the extracted defects located closer to the surface ($V_{ds}=0.5V$), at different gate levels (different power densities).

Acknowledgements

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