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Enhancement of VCSEL performances with a new bonding process

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Motivations

Development of a new VCSEL technological process (called Through Silicon Holes Electroplated Copper process)

Main advantages:

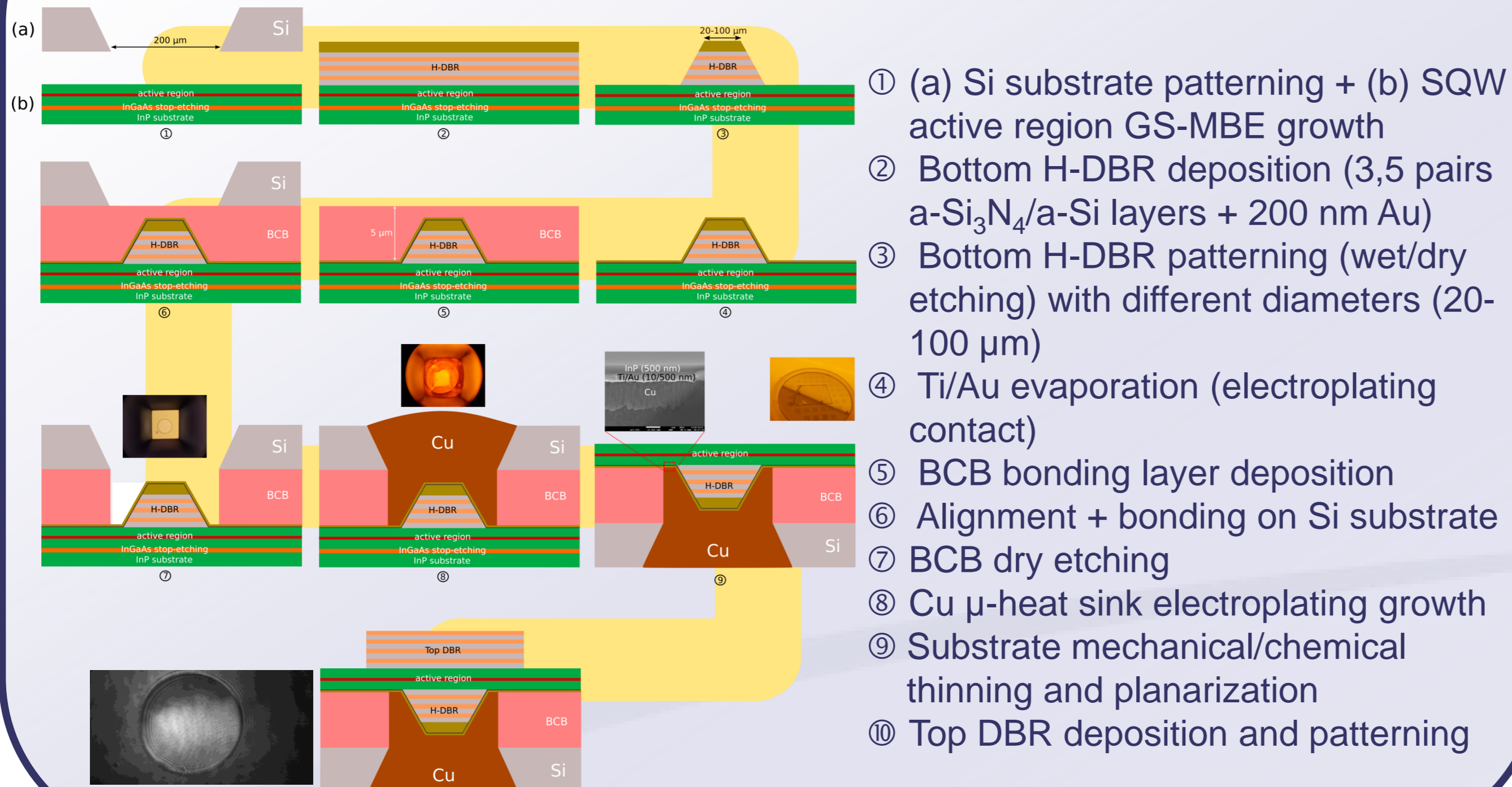
- hybrid integration of (virtually any) III-V active region on Si host substrate
- mechanical stress-induced-free approach with respect to standard large area dissipative Cu surfaces solutions
- possibility of microelectronics, photonics and microfluidics on-chip integration
- fully compatibility with optical pumping and electrical injection schemes
- cost-effectiveness and potential industrial scalability

Demonstration of:

- 1.55 μm emitting InP-based SQW-OP-VCSELs
- Improved optical and thermal laser performances

QW-OP-VCSEL fabrication

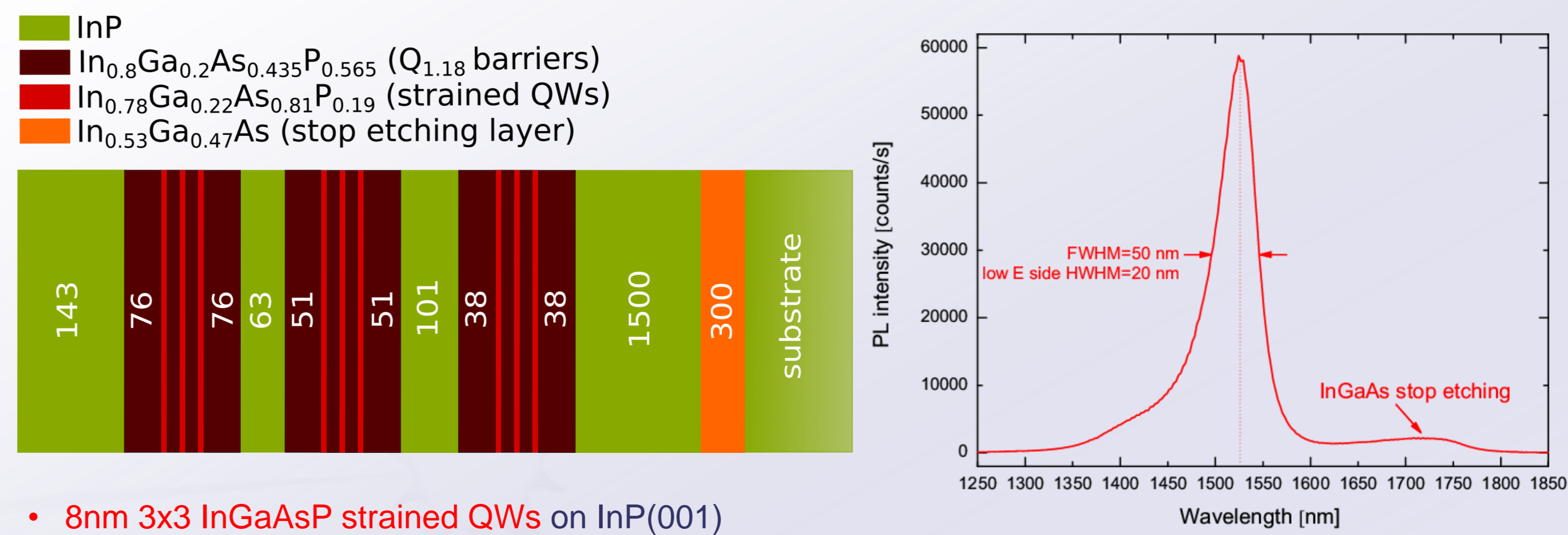
Trough Silicon Holes Electroplated Copper (TSHEC) process [1]



[1] F. Taleb et al., 26th IPRM International Conference, 2014

Active region structure

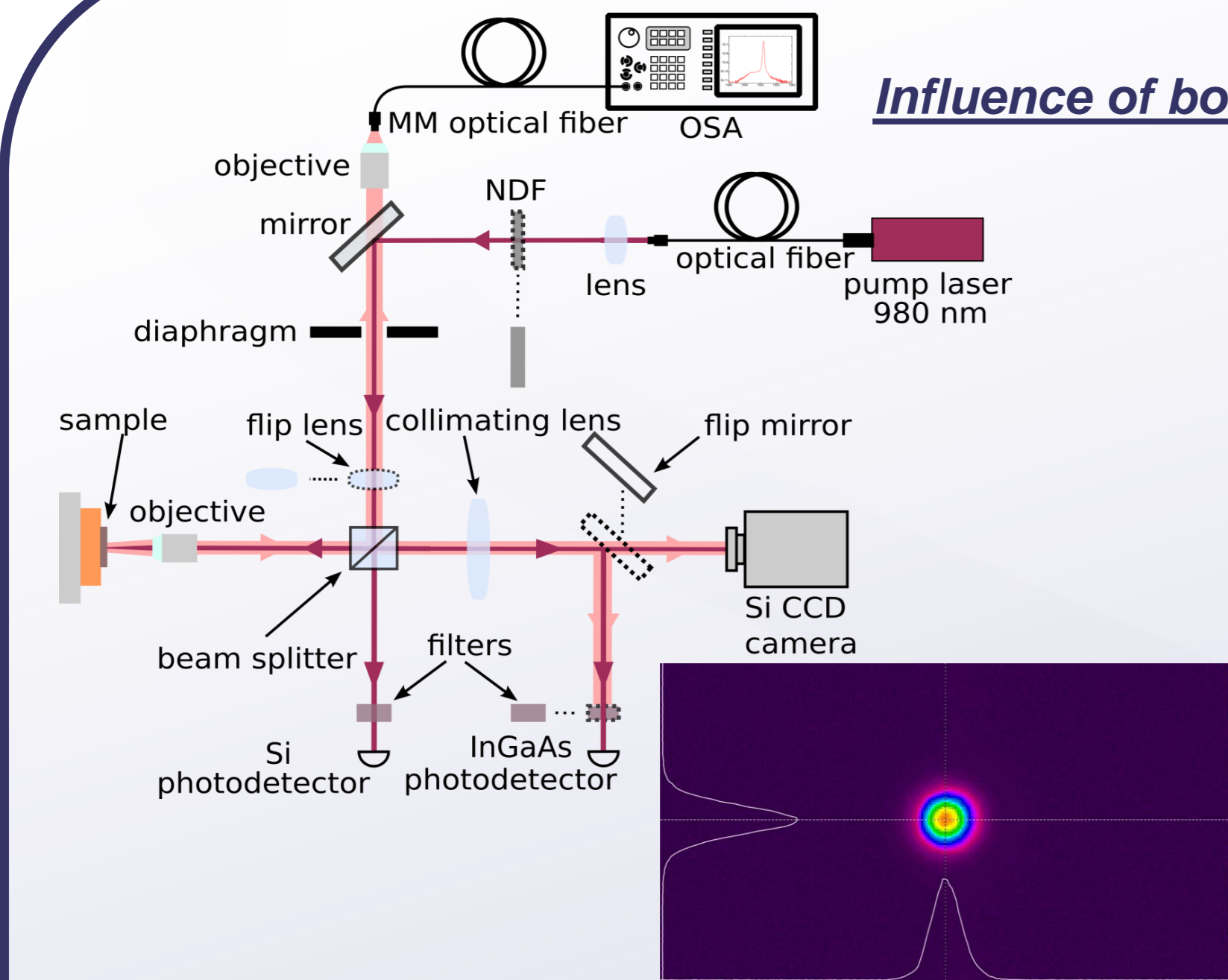
SQW-based active region structure and PL characterization



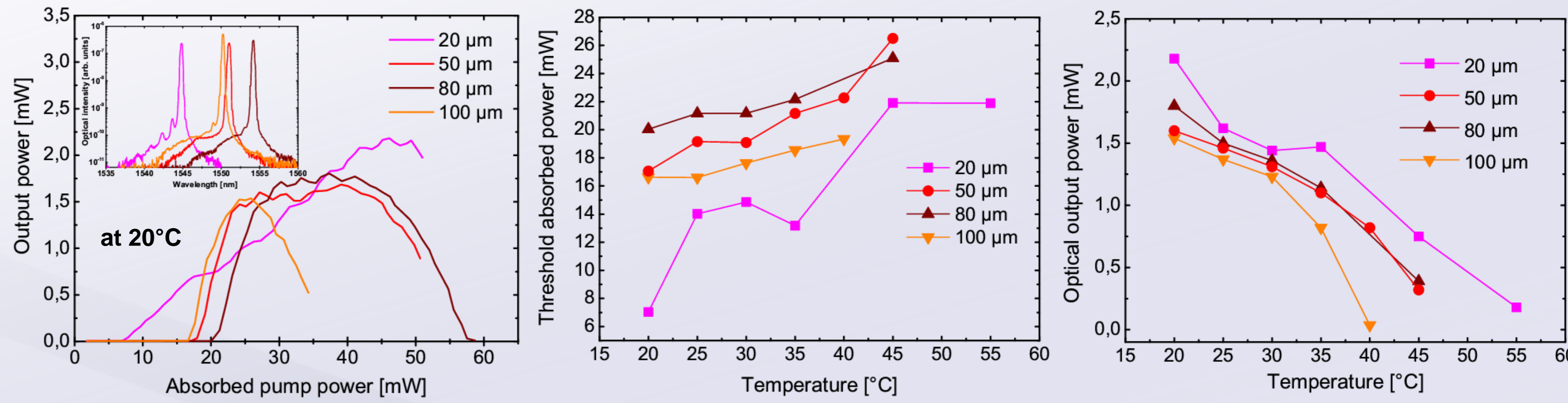
- 8nm 3x3 InGaAsP strained QWs on InP(001)
- Optimized Q_{1.18} barriers thickness \rightarrow uniform pumping of the active region
- Micro-cavity length optimization to match maximum SQWs gain emission (CAD design + post-process InP phase layer thickness wet etching fine adjustments)
- SQWs emission at 1.52 μm to compensate red thermal shift under operation
- FWHM = 50nm; low energy side HWHM = 20nm \rightarrow smooth interfaces

Optical characterization

Influence of bottom H-DBR sizes on CW single mode VCSEL emission wavelength, output power and threshold



- Experimental setup used for VCSEL characterization:
- Sample surface and mode profile imaging
 - Real-time P_{inc}, P_{refl}, P_{abs}, P_{out} measurements
 - Spectrum & temperature dependence analysis



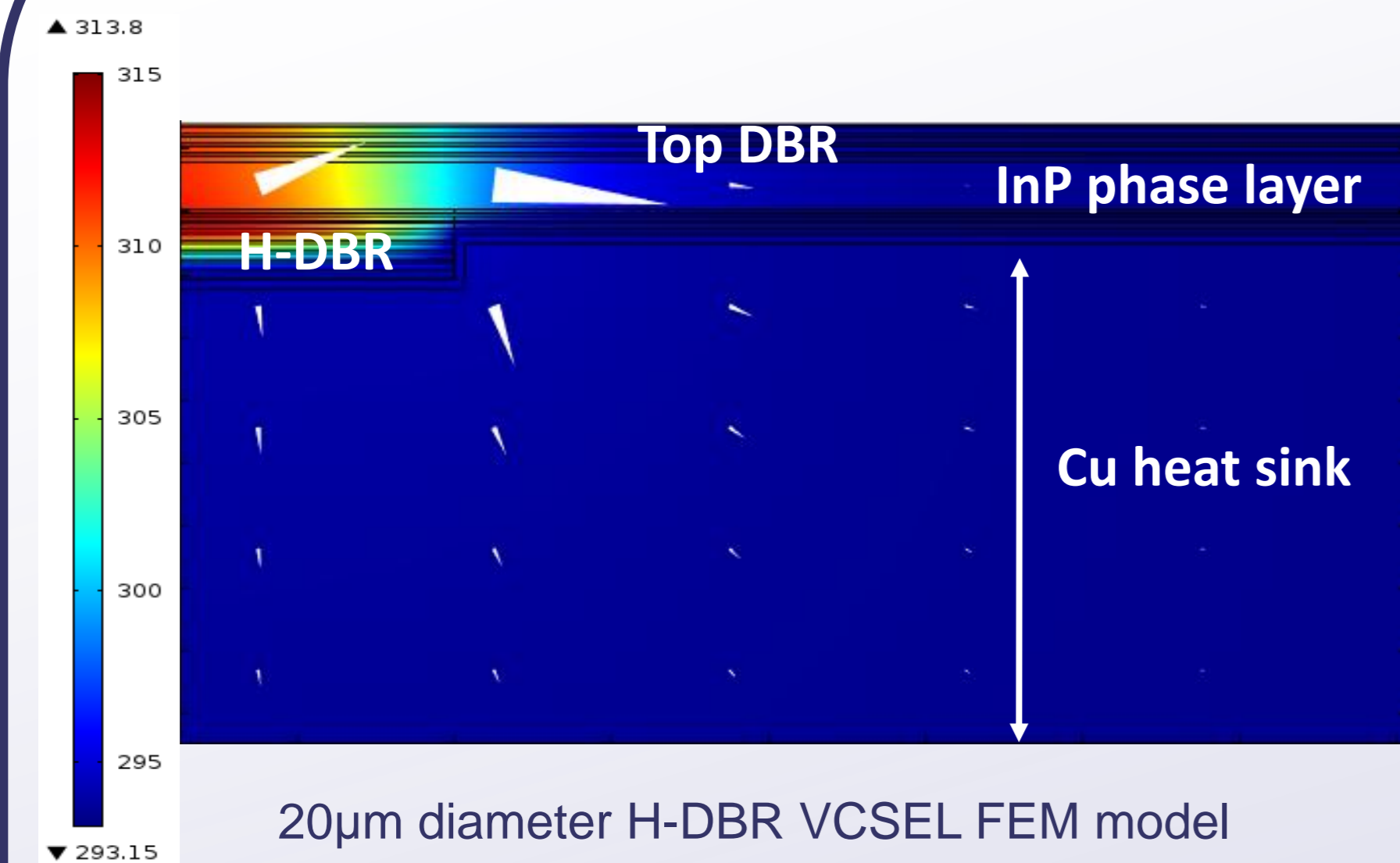
For 20 μm diameter H-DBR at 20°C:

- Emission at 1.544 nm
- P_{out} max > 2 mW in CW SM emission
- P_{th} = 7 mW
- Lasing up to 55°C

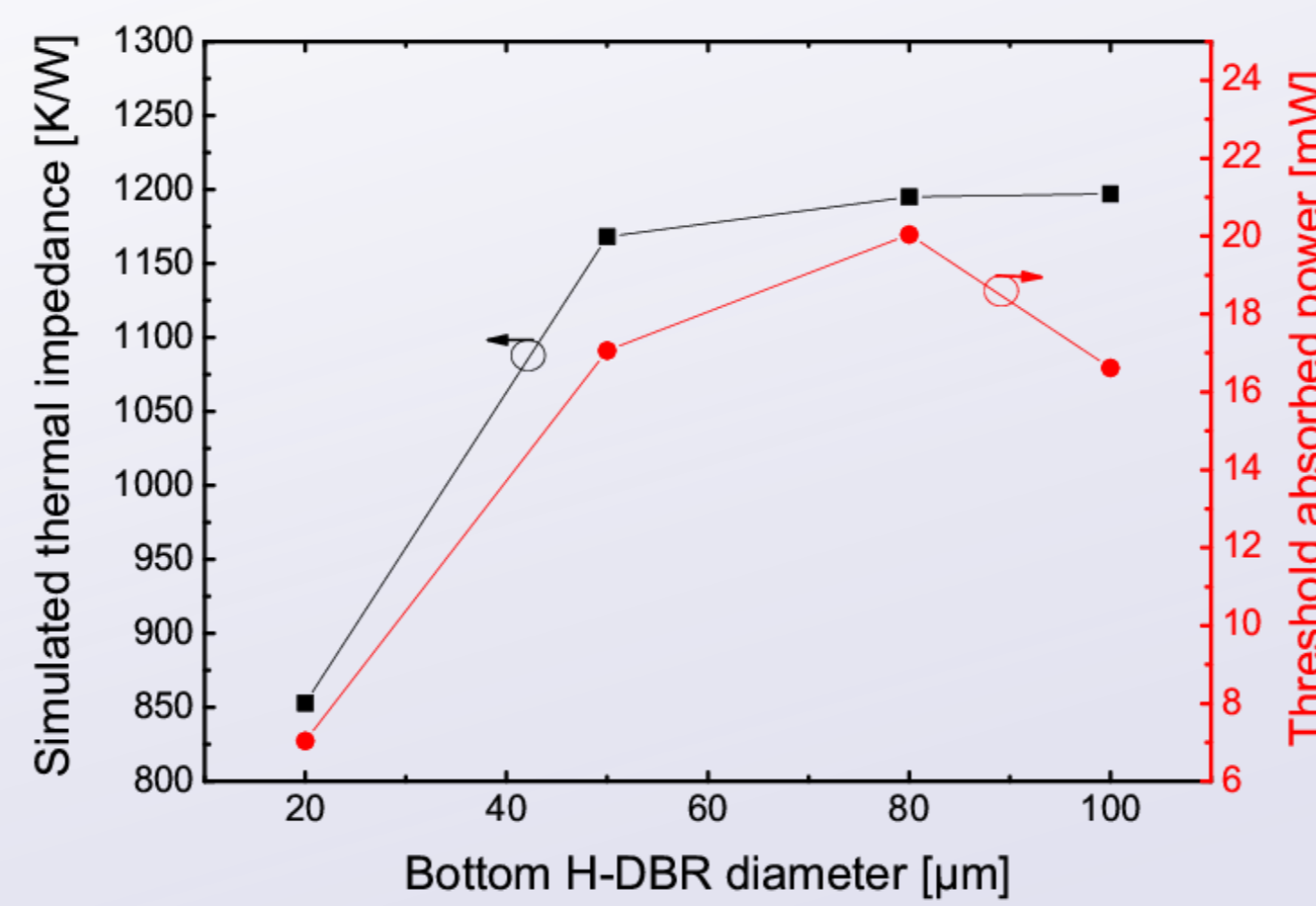
Red shift, higher threshold and lower P_{out} max for higher H-DBR diameter

Thermal characterization

FEM thermal modelling

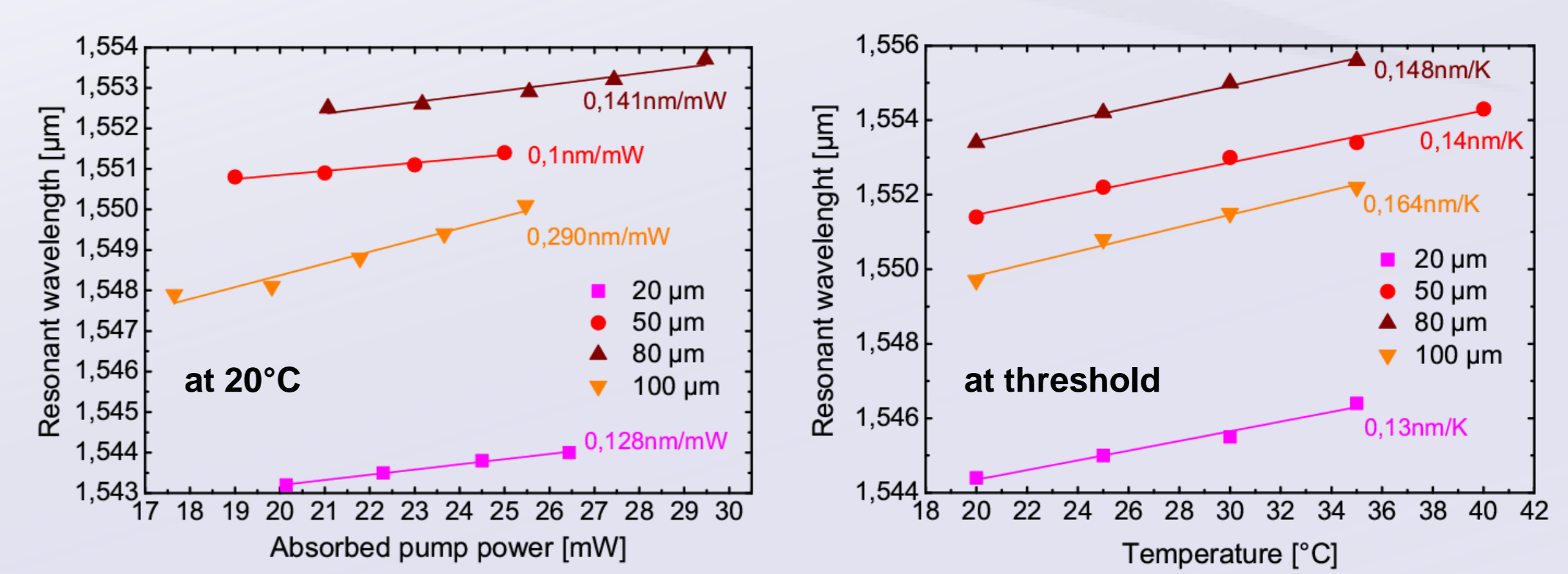


$$R_{th} = \frac{\Delta T}{P_{diss}}$$



Correlation between simulated thermal impedance and threshold absorbed power for different H-DBR diameters sizes

Preliminary thermal impedance measurements



$$R_{th} = \frac{\Delta \lambda}{\Delta P_{abs}} \left(\frac{\Delta \lambda}{\Delta T} \right)^{-1}$$

Experimental measurements of the thermal impedance in agreement with FEM simulations

Conclusions

- Development of TSHEC technology for active region and Si substrate integration
- Enhancement of optical and thermal performances with respect to previous VCSEL technology
- Study on bottom H-DBR size influence on VCSEL emission and thermal properties

Perspectives

- Further improvements of TSHEC technology \rightarrow towards higher P_{out}, lower threshold, lower R_{th}, more reliable process
- Development of TSHEC technology for EP-VCSELs
- On chip microelectronics (temperature sensors, VCSEL driver, etc.)?

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