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High performance, low cost, and double node upset tolerant latch design

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Abstract—In this paper, a high performance, low cost, and double-node-upset (DNU) tolerant latch design (referred to as HLDUT) is proposed in 22nm CMOS technology. The latch mainly consists of a single-node-upset (SNU) resilient cell and a 3-input C-element, and the SNU resilient cell mainly constructs from triple mutual feedback 2-input C-elements, thus the latch is DNU (let alone SNU) tolerant. Using clock gating methodology, high speed transmission path, and fewer transistors, the latch also performs with lower overheads regarding power dissipation, transmission delay, and silicon area. Simulation results have demonstrated the SNU/DNU tolerability, and a ~97.44% area-power-delay product saving for the latch design on average compared with the previous radiation hardened latch designs.

Keywords—single node upset; double node upset; soft error; radiation hardening; circuit reliability

I. INTRODUCTION

In nanoscale CMOS technology, by further shrinking transistor feature size, integrated circuit performance is significantly improved. However, the critical charge of circuit nodes is subsequently decreased, and as a result, in radiation environments, particle striking induced soft errors such as single-node-upset (SNU) and double-node-upset (DNU) occurring in memory elements are becoming a prominent concern with technology evolution [1].

In order to effectively tolerate SNU, researchers have proposed a number of radiation hardened schemes like FERST [2] and LCHR [3]. By means of techniques like dual modular redundancy, these schemes can robustly retain data for latch designs. However, technology scaling results in that, charge sharing induced DNU is becoming more prominent especially in harsh radioactive environments [4]. As a result, existing SNU tolerant latch designs are no longer robust facing to DNU, and cannot be applied to systems requiring higher reliability.

Using techniques like increasing transistor feature size for weak nodes, multiple modular redundancy, and layout solutions such as node spacing increase, well isolation, and guard rings makes a latch design DNU tolerant. For instance, the DNCS-SEUT latch design in [5] and NTHLTCH latch design in [6] are DNU tolerant by means of multiple redundant feeding back C-elements, but these latch designs perform with too large cost penalties regarding silicon area, power dissipation, and transmission delay.

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In this paper, a high performance, cost effective, and robust latch named HLDUT latch is proposed. The latch mainly consists of a 3-input C-element and an SNU resilient cell constructing from triple mutual feedback C-elements to retain data. The latch is not only SNU tolerant, but also DNU tolerant, and simulation results have demonstrated the robustness and considerable area-power-delay product (APDP) saving on average compared with the previous hardened latch designs.

II. PROPOSED HARDENED LATCH DESIGN

A. Circuit Structure and Behavior

Fig. 1 presents the circuit structure of the proposed latch. The SNU resilient cell (referred to as SRC) consists of two transmission gates (to avoid positive feedback loops to save power), two inverters (to ensure correct feedback logics), and three 2-input C-elements to retain data. As we can see, the latch constructs from the cell, a 3-input C-element, two clock gating (CG) based inverters, and other three transmission gates.

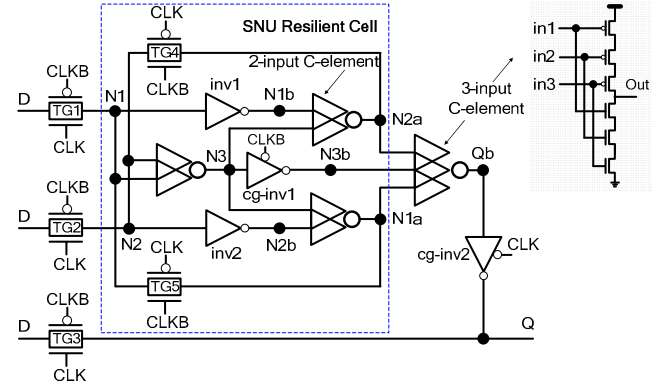


Fig. 1. Proposed HLDUT latch.

When CLK = 1, the latch works in transparent mode. D propagates to N1, N2, and Q, through TG1, TG2, and TG3, respectively, and then all the inverters and C-elements are biased correctly. Note that, TG4, TG5, and cg-inv2 are OFF, and hence positive feedback loops and current competition are avoided to save power dissipation. Using CG technology, Q is prevented from being driven through cg-inv2 and instead Q is directly driven through TG3 to improve performance.

When $CLK = 0$, the latch works in latching mode. SRC keeps correct data, and Q is only driven by SRC through cg_inv2 . As for an SNU, in the case that a single node inside SRC is affected, SRC restores back the correct data from the SNU like RFC latch [7], and in the case that N2a, N3b or N1a is affected, the 3-input C-element holds correct data on Qb. Specially, when N2a, N1a, Qb or Q is affected, the latch restores back from the SNU. Hence, the latch tolerates SNU. Next, when a pair of nodes is affected by a DNU, since N1 equals to N1a and N1b regarding soft error sensitivity (so does that for N2-N2a-N2b), we only need to consider N1 and N2. Thus only N1, N2, N3, N3b, Qb, and Q are the key nodes. As for any key node accompanies with Q, these paired nodes can restore back since SRC is SNU resilient. As for any other key node accompanies with Qb, these paired nodes can also restore back except $\langle N3b, Qb \rangle$. As for any other key node accompanies with N3b, and other pairs, the 3-input C-element blocks the glitches. In sum, the latch tolerates DNU.

B. Simulation Results

The HLDUT latch was designed using the 22 nm CMOS technology of PTM [8] (Supply voltage is 0.8V). The layout was drawn by Cadence platform (Virtuoso), and pertinent simulations using HSPICE were performed. According to simulations, the operation of the latch in the normal mode of operation is exactly the same as that of a conventional latch.

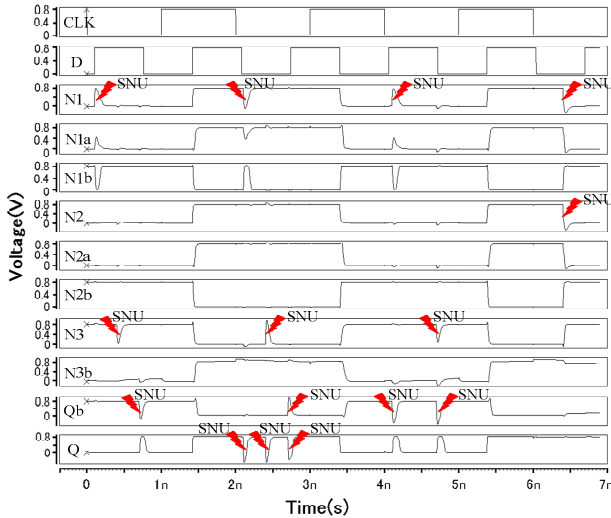


Fig.2. Simulation waveforms for HLDUT latch.

Fig. 2 shows the indicative SNU/DNU injection simulation results for the latch. As for soft error sensitivity, $N1 = N1a = N1b$, $N2 = N2a = N2b$, thus the simulations for N1a, N1b, N2a, and N2b are omitted. As shown in Fig. 2, at 0.1, 0.4 and 0.7 ns, an SNU is simulated on N1, N3 and Qb, respectively, but the nodes restore back the correct data. At 2.1, 2.4, 2.7, 4.1 and 4.7 ns, a DNU is injected on node pairs $\langle N1, Q \rangle$, $\langle N3, Q \rangle$, $\langle Qb, Q \rangle$, $\langle N1, Qb \rangle$ and $\langle N3, Qb \rangle$, the nodes also restore back the correct data (let alone SNU). At 6.4 ns, a DNU is simulated on $\langle N1, N2 \rangle$, the nodes cannot restore back. However, the 3-input C-element blocks the glitches, resulting in no effect on Q. As we can see, the simulation results validate the SNU/DNU tolerance.

III. LATCH COMPARISON AND EVALUATION

To make fair comparison, the FERST, LCHR, DNCS-SEUT and NTHLTCH latch designs were designed in the same technology. Comparison results are presented in Table I, with respect to whether SNU/DNU is tolerant, silicon area, the average of dynamic plus static power, transmission delay and APDP product, respectively. Similarly, the area of these latch designs was also measured in equivalent unit size transistors (USTs) as in [9], and the APDP was calculated by multiplying area, power, and delay. Obviously, among the same type latches (e.g. DNU tolerant ones), a smaller APDP is better.

From Table 1 we can see that, as for the proposed latch design, DNU hardening brings about little more area penalty than the only SNU tolerant latches, but the power, delay, and APDP is the smallest. Compared with the other DNU tolerant latch designs, the proposed is DNU tolerant (let alone SNU) as well, but saves a $\sim 97.44\%$ APDP on average. In sum, the proposed latch is not only robust, but also cost effective.

TABLE I. COMPARISON AMONG RADIATION HARDENED LATCH DESIGNS

Latch Name	SNU Tolerant	DNU Tolerant	Area (UST)	Power (μW)	Delay (ps)	$10^{-3} \times$ APDP
FERST	Yes	No	104	1.17	52.06	6.33
LCHR	Yes	No	93	1.06	70.38	6.94
DNCS-SEUT	Yes	Yes	162	2.35	65.41	24.90
NTHLTCH	Yes	Yes	178	2.20	13.01	5.09
Proposed	Yes	Yes	156	0.83	1.46	0.19

IV. CONCLUSIONS

In this paper, a novel robust, and cost effective latch design is proposed to effectively tolerate SNU/DNU. Simulation results have demonstrated the robustness and a $\sim 97.44\%$ APDP saving on average compared with the previous radiation hardened latch designs.

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