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Electrical and Physical Analysis of Thermal Degradations of AlGaIn/GaN HEMT under Radar-type Operating Life

Farid TEMCAMANI, *member IEEE*, Jean-Baptiste FONDER, Olivier LATRY, Cédric DUPERRIER

Abstract— Failure mechanisms in AlGaIn/GaN HEMT RF power amplifiers implemented on silicon substrate and envisaging radar operating conditions are investigated in this paper. Several power amplifier prototypes have been designed, fabricated, characterized, and tested. Ageing tests were performed in conditions as close as possible to real applications. Ageing under increased drain voltage allowed studying both thermal and electrical aspects. Characterization performed before and after ageing tests proved that ageing process is mainly due to thermal stress for the irreversible part and to trapping effects for the reversible one, respectively. This was confirmed by additional physical analysis, the results revealing strong changes of the Schottky contact. Photons emission microscopy associated with X radiography gives spatial correlation between gate degradation and evolution of the brazing interface between the transistor chip and its packaging. It also illustrates the appearance of overheating points and acceleration of the Schottky contact degradation.

Index Terms—GaN, HEMT, Radar, reliability, failure, power amplifier, ageing bench, channel temperature, physical analysis, electrical analysis

I. INTRODUCTION

AlGaIn/GaN HEMT technology presents a high mobility thanks to the heterostructure and wide bandgap material. It proves good performances, making it suitable for power applications, higher frequencies and temperature operation [1][2]. Many studies have been published since the early '90s [3]-[9] while commercial power transistors were issued on the market more than ten years ago. In spite of their impressive performances, their reliability still remains unknown.

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The AlGaIn/GaN heterostructure has to deal with defects coming from the material properties and fabrication process. As a result, many researches have been conducted to evaluate and enhance the device reliability in working conditions as close as possible to the final application [10]-[16].

This paper identifies the main parameters affecting the reliability and irreversible degradations (reversible effects are investigated in [10]) of a radiofrequency power amplifier implemented in this technology. According to our experiments, the critical parameters affecting device reliability are the electrical constraints related to high voltage and current operation and thermal constraints related to transistor self-heating effects. Ageing tests, electrical characterization, and failure physical analysis were performed to rank these parameters. In this regard, the global study methodology is described in the second section while ageing tests results are detailed in the third one. Electrical characterization is reviewed in section IV while the physical origin of degradations is studied and discussed in section V. Our study is completed by physical and structural analyses, as described in section VI. Finally, conclusions are drawn in the last section.

II. METHODOLOGY AND MEASUREMENTS

A. Device under test

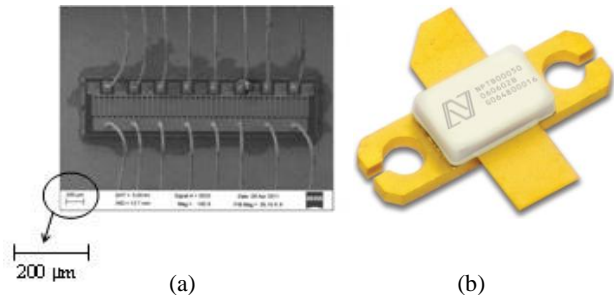


Figure 1 – Transistor under test: (a) chip and (b) packaging

For designing amplifiers, we choose commercial 50 W GaN HEMTs (reference NPTB00050 from Nitronex) with the

following characteristics:

- 80 gate fingers
- 0.5 μm gate length
- 16.8 mm total gate width
- V_{DS} breakdown voltage higher than 110 V for gate voltage between -2 V and 0 V.

The die's package is AC360B type ceramic frame. Connection to leads is performed with eight gold bond wires for both gate and drain. Source terminal is via-grounded to the frame. The chip thickness is 150 μm .

The HEMTs have been used for designing 50 W class-B amplifiers, operating at 3 GHz frequency and 28 V drain bias voltage. Load-pull impedances were simulated with a "blackbox" manufacturer model and ADS Agilent software. The objective was to obtain the maximum output power with the highest reachable power added efficiency. Microstrip matching circuits were then designed on Rogers Duroid RT6010.2 Cu-Clad Substrate ($\epsilon_r=10.2$, $h=0.63$ mm). Classical techniques as microstrip impedance transformers and low frequency stabilization (by a 100 Ω resistor in series with gate) were used. Under pulsed-RF measurements, we reached 50 W of saturated output power in class-B, which corresponds to 3 W/mm of power density. PAE reaches a maximum of 53%.

B. Methodology

Our methodology is based on several steps, from amplifier design to micro-structural analysis of the transistor's possible failure zones, including ageing tests and electrical characterization.

The first step is device characterization to understand with maximum accuracy its structural, thermal, and electrical properties. This step should offer sufficient information for designing, fabrication and measurement of prototype amplifiers.

In the second phase, the amplifiers are built and measured. Furthermore, the prototypes are tested on the ageing bench.

Finally, to explain the ageing evolution, and possibly the device failure, physical analyses are performed. Analysis tools go from simple visual inspection to transmission electronic microscopy (MET), including radiography and photon Emission Microscopy (EMMI). They should allow confirmation or invalidation of assumptions formulated after electrical characterization and ageing tests.

C. Stress test bench and electrical characterization

The test bench [16], shown in Fig. 2, is based on a central unit that can test several devices simultaneously. It consists of a computer driven control and data-recording peripherals (power supplies, triggers, memories). Power modules, made up of thermally regulated Cu base plates on which test

amplifiers are fixed and thermally coupled, are driven by this central unit. The RF part consists of a signal source, providing RF pulses triggered by the central unit, a power amplifier delivering sufficient input power level to each tested device, a power divider, couplers and circulators to measure input power and return loss.

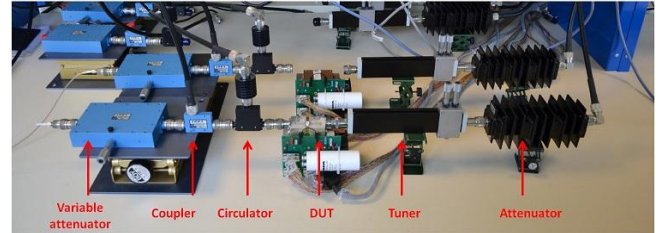


Figure 2- The ageing bench

The output of each DUT (device under test) is connected to a 40 dB attenuator, connected further to a power sensor. During measurements, the RF power, current, voltage and temperature are monitored and stored. Ageing can be performed both in L-band (1-2 GHz), as in [17], and S-Band (2 – 4 GHz).

Electrical characterization consists of conducting several electrical measurements before and after ageing tests, such as:

- Transistor DC output characteristics: $I_{\text{D}}(V_{\text{GS}}, V_{\text{DS}})$.

In this regard, two particular parameters give information on physical degradation: the pinch-off voltage V_{p} and the on-state drain to source resistance R_{DSon} .

- DC characteristic of the gate contact $I_{\text{G}}(V_{\text{GS}})$, which allows barrier height and ideality factor extraction.
- $P_{\text{OUT}}(P_{\text{IN}})$ RF characteristic, to estimate the maximum output power, power gain, and power added efficiency (PAE).

D. Physical analysis

The physical analysis includes analyses from macroscopic to nanoscopic scale. Analysis tools could be summarised as follows:

- Visual inspection simply consists of opening the device packaging. In this case, a first inspection is performed with an optical microscope while a second one is with a scanning electron microscope (SEM).

- Photon Emission Microscopy is a non destructive method commonly used to reveal structural surface defects in semiconductors [18][19]. The photon intensity is proportional to current density. Typical application of such a technique is to compare the current distribution across the gate fingers in a transistor. The system consists in a Phemos (Hamamatsu) microscope equipped with a Si-CCD ultrasensitive camera cooled down to very low temperature (-70°C). Wavelengths detected are between 400 nm to 1100 nm. Images are acquired with the same exposition time and colour scale under DC bias conditions. Optical signature of emitted photons is compared

between stressed and unstressed devices. Spatial resolution of the EMMI pictures is approximately 2 $\mu\text{m}/\text{pixel}$ (2600 μm x 2600 μm per image).

- X radiography: this technique, based on X and Gamma rays, is used to estimate the quality of the brazing between the transistor and its package, mainly after ageing tests. As in previous case, the results are compared between stressed and unstressed devices.

- Micro-structural analysis of failures with Transmission Electron Microscopy (TEM) and Focused Ion Beam (FIB). TEM is commonly used to investigate the inner structure of very small samples such as gate contacts, transition between two layers, etc. Structural contrast and/or chemical contrast are observable revealing details at nanometre scale. In our case, it is used to evaluate the sharpness of the Schottky gate contact, the most thermal sensitive area in a GaN HEMT, on a fresh and on an aged device.

This technique requires some sample preparation in FIB and SEM. The sample is extracted from the whole transistor structure and is thinned into a 40 nm thick lamella to become electron-transparent and thus allowing TEM study. These milling/cutting operations are performed with a pico to nano amp gallium focused ion beam depending on the preparation step (milling, cleaning...).

Equipment we used for TEM is a JEOL JEM-ARM200F HR-TEM. The contrast of the Scanning Transmission Electron Microscopy - High Angle Annular Dark Field (STEM-HAADF) images dependent of the atomic number (Z) of elements. The acquisition is done with a camera length of 8 cm and 0.1 nm probe.

- Energy Dispersive X-ray Spectroscopy (EDS): JEOL JEM-ARM200F is equipped with optional EDS. EDS is based on the characterization of X photons emitted by the sample during the electron beam crossing. This technique applied to FIB samples allows analyzing of chemical compositions with 0.2 nm probe.

III. AGEING TESTS

A. Test protocol

Five power amplifiers (prototypes) were aged on the test bench shown in Fig. 2 which can supports up to eight devices, the technical risks limiting the number of tested devices. It should be recalled here that the test must be preceded by a long characterization of transistors and amplifiers, in our case the cumulated duration of the five components ageing being about 3600 hours. Furthermore, as shown later, only small result dispersion was noticed between different transistors and amplifiers.

As already mentioned, the objective of this research is to highlight the dominating phenomenon that influences the

amplifiers' performances evolution and degradation. In this regard, identical amplifiers with similar matching circuits have been tested and only biasing conditions (V_{DS0} and I_{D0}) were modified.

TABLE I
DURATION OF EACH AGEING TEST

Bias	Test duration (hours)
40 V 0 mA	837
40 V 600 mA	752
43 V 0 mA	819
45 V 0 mA	791
45 V 200 mA	432

Indeed, the amplifiers' power efficiency has little dependence versus drain-to-source bias voltage V_{DS0} . Proceeding this way allows the simultaneous increase of the drain voltage excursion and dissipated power in the transistor (i.e., channel temperature). Pulsed RF and CW excitations induce different stresses in the device. While the thermal state of the transistor is steady in the CW case, the channel temperature swings at the pulses' rate. It is especially true if pulse length is larger than several thermal time constants τ_{TH} and period T is much higher than pulse length, as in our case. We can easily conclude that these thermal cycled working conditions will induce a different wear out than CW one.

Sometimes, the channel temperatures induced by these tests could exceed 350°C, therefore lower values are set for the base plate temperature. The main effects are the small variations of load and source impedances. The load curve is only translated horizontally compared to its nominal position with $V_{DS0}=28$ V. As a consequence, the gate to source transistor junction will become open before starting to work within ohmic zone (i.e., time-varying V_{GS} becomes larger than threshold value before the load curve reaches the knee zone of the I-V network). This was evidenced during our measurements. Therefore, input power is fixed according to the average gate current.

The protocol of these tests is inspired from the one related to the nominal operation as follows:

- Frequency: 3 GHz;
- Base plate temperature: 20° C;
- Pulsed RF signal: duty cycle 15%, pulses width of 450 μs ;
- Input power $P_{IN}=39.5$ dBm, fixed, so that average gate current I_G is larger than 300 μA . It corresponds to soft gain compression of about 1 dB. Tests biasing conditions are as follows:
 - $V_{DS0}=40$ V and $I_{D0}\approx 0$ mA (class-B);
 - $V_{DS0}=40$ V and $I_{D0}=600$ mA (deep class-AB, $I_{D0}\approx I_{DSS}/10$);
 - $V_{DS0}=43$ V and $I_{D0}\approx 0$ mA (class-B);

- $V_{DS0}=45$ V and $I_{D0} \approx 0$ mA (class-B);
- $V_{DS0}=45$ V and $I_{D0}=200$ mA (deep class-AB).

Operation in class-AB is tested to evaluate the quiescent current effect on amplifier performance degradation. It should be recalled here that a strong dependence between the quiescent drain current and the RF output power can be noticed in pulsed mode [10]: as the output power rises (i.e., gate and drain swing), the quiescent bias current tends to lower. For instance, for "45 V 200 mA" stressed device, the drain bias current between RF pulses is almost null at maximum output power. It was proved that this phenomenon is related to trapping effects. Hence, it can be considered that at the specified stress conditions, "45 V 200 mA" and "45 V 0 mA" devices run both in class-B.

Simulations show that the breakdown voltage is not reached in all these tests, the maximum reached voltage being about 90 V in the worst case ($V_{DS0}=45$ V), therefore leaving sufficient margin (the measured breakdown voltage is about 110 V). Power characteristics of each amplifier, e.g., $P_{OUT}=f(P_{IN})$, is measured before and after each test and pulsed I-V and CW S-parameters measurements are performed as well. Finally, we point out that tests are performed without interruption, each amplifier being tested during hundreds of hours, as resumed in Table 1.

B. Performance monitoring

Contrary to base plate temperature, the injected power in the amplifier is not regulated, therefore affecting negatively the tests which require constant power levels. Measurements show small changes of $\pm 5\%$ in the worst case and $\pm 2\%$, on average. These small variations are due to ambient temperature between day and night. They are reversible and did not affect our conclusions. We take into account on long term average variations.

Measured changes of the amplifier characteristics (output power P_{OUT} , average drain current I_D and average gate current I_G) which affect each tested device are summarized in Table 2. For example, $\Delta I_d/I_d$ stands for average drain current in large signal condition during the stress test.

The following conclusions could be drawn:

- Degradations of P_{out} , I_d and I_g variations are globally correlated.
- A stronger decrease of the output power affects the amplifiers operating with higher dissipated power (45 V-200 mA, 45 V-0 mA and 43 V-0 mA). In both first cases, the output power decrease has a lower value than in the case of 43 V and 0 mA. These cases have also the same dissipated power. Cases with (40 V, 0 mA) and (40 V, 600 mA), present a similar power degradation. It means that quiescent current has a small influence on the performance degradation.
- The drain current strongly decreases in (40 V, 600 mA)

case, having no evident correlation with the output power decrease. The latest is even similar to the case with 40 V and 0 mA for which the drain current is almost constant. It means that the strong decrease of drain current is due to quiescent current I_{D0} decrease during the test.

- There is a strong increase of the average gate current. The variation is close to 300 μ A when starting the test and increases up to two or three times during the ageing test. It should be noticed that this gate current is not a leakage one and is essentially related to a light gate saturation (the gate-to-source junction becomes lightly passing). According to our experiments, the input power remains constant during the test. Hence, the gate current increase is related to drift of the junction threshold voltage.

IV. ELECTRICAL CHARACTERIZATION

A. RF power characterization

$P_{OUT}=f(P_{IN})$ and $I_D=f(P_{IN})$ characteristics of the amplifiers are measured before and after each ageing test. Furthermore, power gain and efficiency are calculated with these measured results. Table 3 presents the variations measured during the tests for power gain with low (30 dBm) and high (39 dBm) input power levels (respectively named $\Delta G_{P_{OUT}}$ and ΔG_C). The compression gain decreases for all tested amplifiers, a result that is in good agreement with the power decrease noticed in the previous paragraph.

Otherwise, for some amplifiers low power gain has increased. It means that the device performance degradation occurs especially for large V_{DS} and I_D swings. Therefore, it would be interesting to examine the transconductance g_m and R_{DSon} , both transistor parameters being decisive for high power gain. Table 4 resumes the variation of high power efficiency ($P_{IN}=39$ dBm), low power drain current (ΔI_{DPOUT}) and high power drain current (ΔI_{Dcomp}). All tested amplifiers showed drain current decrease at high output power level. It is also in good agreement with the assumption that g_m and R_{DSon} degrade in the ohmic zone. Otherwise, it is clear that in all other cases, the drain current increases at low input power levels. It is also in correlation with low level power gain for 40 V-0 mA and 43 V-0 mA cases. In both cases, the amplifiers operate in class-B and in consequence the pinch-off transconductance changes strongly with I_{D0} . The latest parameter depends itself of pinch-off voltage V_p . This parameter seems to be essential. Nevertheless, the low level gain decreases for 45 V-0 mA and 45 V-200 mA (Table 3) have probably another reason. Both transistors tested under 45 V come from a different production batch than the other three. In addition, we noticed that the (40 V, 600 mA) test only showed a small increase in power efficiency.

It confirms our previous assumption of correlation between I_D decrease during the test and I_{D0} decrease. It is also confirmed by the simultaneous I_{DPOUT} and I_{Dcomp} decrease. Moreover, the contribution of I_{D0} to the efficiency is weak so the latter is enhanced.

B. DC measurements

Measurements of the output characteristics $I_D(V_{DS}, V_{GS})$, input characteristic $I_G(V_{GS})$ and leakage characteristic $I_G(V_{DG})$, are performed. The objective is to find correlations between the variations of the transistor performances and its intrinsic behaviour. For the sake of simplicity, only pertinent parameters will be presented and discussed.

Figure 3 illustrates the DC output characteristics of the transistor tested in case (45 V, 200 mA), before and after ageing. The observed degradations are typical and measured for all components. As expected, and under low V_{DS} , the output transistor characteristics show a transconductance g_m decrease and an R_{DSon} increase. Output power degradations observed previously are due to these variations.

The conjunction of both elements (g_m and R_{DSon}) induces a shift towards the right of the knee of V_{DS} - I_D DC characteristics. The V_{DS} and I_D swings have then smaller amplitudes and the output power is lowered. However, under high V_{DS} (greater than 15 V), the shift of pinch-off voltage V_P to more negative values becomes a more important parameter than the g_m decrease.

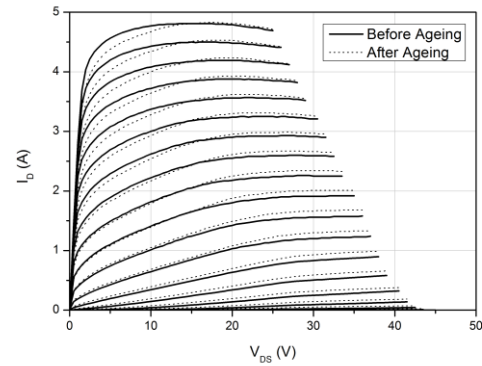


Figure 3- $I(V)$ output characteristics for the test 45 V-200 mA: before ageing and after ageing. $-1.8 \text{ V} < V_{GS} < 0 \text{ V}$ with a 0.1 V step.

In Table 5, we present an inventory of R_{DSon} and g_m variations for $V_{DS}=3.5 \text{ V}$ and V_P variations for $V_{DS}=30 \text{ V}$.

Results show clearly that for almost all transistors pinch-off voltage V_P and transconductance g_m decrease. R_{DSon} increases in all cases. Previous assumptions deduced from RF power measurement are confirmed.

Another interesting measurement concerns the Schottky gate-to-source contact. It consists in measuring before and after ageing the DC $I_G(V_{GS})$ characteristic for the direct part and the DC $I_G(V_{DG})$ for the reverse part and the leakage current.

TABLE 2
EVOLUTION OF AMPLIFIERS' ELECTRICAL PERFORMANCES DURING THE TEST. DEGRADATIONS OF P_{OUT} , I_D AND I_G ARE CORRELATED.

Bias conditions	ΔP_{OUT} (%)	$\Delta I_D / I_D$ (%)	$\Delta I_G / I_G$ (%)
40 V 0 mA	-3.0	-2.4	$\approx +90$
40 V 600 mA	-3.9	-16	$\approx +100$
43 V 0 mA	-13	-7.8	$\approx +220$
45 V 0 mA	-10	-5.5	$\approx +150$
45 V 200 mA	-12	-5.2	$\approx +200$

TABLE 3
VARIATION OF AMPLIFIERS' POWER GAINS. G_{POUT} IS THE LOW POWER GAIN AND G_C IS THE POWER GAIN IN THE COMPRESSION ZONE.

Bias	ΔG_{POUT} (dB)	ΔG_C (dB)
40 V 0 mA	+0.4	-0.1
40 V 600 mA	0	-0.2
43 V 0 mA	+0.4	-0.2
45 V 0 mA	-0.2	-0.4
45 V 200 mA	-0.4	-0.4

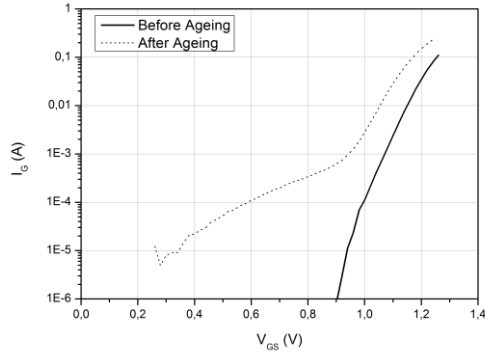


Figure 4- Phenomenon of a double barrier height after the transistor ageing test under 43 V-0 mA.

For the direct measurement, the increase of the threshold voltage V_{TH} is clearly correlated to the gate current increase during the ageing. So, the origin of the latter is established.

TABLE 4
VARIATIONS OF MAXIMAL ADDED POWER EFFICIENCY, AND DRAIN CURRENT AT LOW AND HIGH POWER LEVELS.

Bias	ΔPAE (points)	ΔI_{DPOUT} (%)	ΔI_{Dcomp} (%)
40 V 0 mA	-2.4	+5.2	-1.3
40 V 600 mA	+1.8	-6.3	-9.4
43 V 0 mA	-4.2	+7.9	-1.9
45 V 0 mA	-3.3	+14.8	-4.4
45 V 200 mA	-0.6	-2.3	-1.9

TABLE 5
VARIATION OF R_{DSon} , AND g_m FOR $V_{DS}=3.5$ V AND OF V_P FOR $V_{DS}=30$ V.

Bias	ΔR_{DSon} (%)	Δg_m (%)	ΔV_P (%)
40 V 0 mA	+9.4	+0.5	-1.8
40 V 600 mA	+5.1	-0.5	-1.8
43 V 0 mA	+12.4	-4.3	-2.9
45 V 0 mA	+9.2	-5.5	-2.1
45 V 200 mA	+12.6	-4.2	-1.6

TABLE 6
EXTRACTION OF THE BARRIER HEIGHT Φ , THE IDEALITY FACTOR η , AND THE INTRINSIC RESISTANCE R OF THE GATE TO SOURCE JUNCTION, BEFORE AND AFTER THE AGEING TEST UNDER 43 V-0 mA

	Before ageing	After ageing
Φ_1 (eV)	1.76	0.81
η_1	1.31	1.54
R_1 (Ω)	0.29	0.28
Φ_2 (eV)	-	0.54
η_2	-	4.39
R_2 (Ω)	-	-0.3

For the reverse part, the conclusion for the leakage current is less obvious. Transistors with higher channel temperature (43 V-0 mA, 45 V-0 mA and 45 V-200 mA, see Table 7) do not have the same behavior. Special interest is given to the 43 V-0 mA case. The transistor shows a strong increase of leakage current and a threshold voltage decrease. Furthermore, the direct characteristic (figure 4) changed after the ageing test and presents now two barrier heights. The effect was observed but less clearly for the 45 V-0 mA case. The second Schottky barrier appeared during the ageing test has a worse ideality factor η_2 (Table 6). This double barrier effect has been already mentioned in literature [21] for Ti/4H-SiC Schottky diodes. It is due to interface states caused by the ageing test.

V. DISCUSSION ON THE ORIGIN OF DEGRADATIONS: TEMPERATURE ROLE

In HEMT GaN, with other kinds of stress, the Schottky contact is not the only degraded structure during stress. Pits and trenches could have formed under the gate edge at the device's drain side, for under high-power DC conditions [24][25]. These off-state stress conditions produce electroluminescent signature [26] unlike on large area as in our observations. The electroluminescent signature is typically relevant here for a large phenomenon like diffusion of Au for several gates in a part of the transistor. It is not a much localised region like pit evolution after DC stress already observed in previous work [27].

Previous summarized conclusions are:

- The transconductance decrease at low V_{DS} and the simultaneous R_{DSon} increase seem to be the origin of the higher gain compression and the output power decrease.
- All measured pinch-off voltages were shifted to more negative values, for high V_{DS} . The quiescent currents have then increased; the small signal transconductance has increased in the same way as the small signal gain has increased for some devices.
- A decrease of gate-to-source junction voltages of all tested devices has been noticed. It is the origin of the strong increase of direct gate current during the ageing tests.

In conclusion, all electrical degradations affect the control mechanism of the transistor. The gate is the more impacted zone. Confirmation is given by the Schottky barrier evolution for the tests imposing the most severe thermal constraints. So, the channel temperature seems to be an important parameter for the transistor ageing analysis.

In the following paragraphs we will establish the correlation between the channel temperature and the observed degradations. The channel temperature is generally not well estimated in life-test benches [15]. On the other hand, the estimation of the temperature in the pulsed mode imposes not only the knowledge of the device's thermal resistance R_{TH} , but

also the thermal time constant τ_{TH} . Two techniques are generally used: infrared thermography and electrical measurements [28]. In the present paper, we apply these techniques to physical analyses of degradations.

A. Principle of the channel temperature measurement

Infrared thermography is a well known technique for temperature measurement which was particularly applied to RF power transistors [22]. It is very efficient to establish temperature cartography but this spatial advantage is just the opposite of its too large integration time, which is not compatible with the instantaneous temperature measurement, which is necessary in pulsed mode.

For temporal requirements, Joh *et al.* [23] proposed an electrical-based method for small transistors (4x100 μm). It consists in varying the temperature and measuring the corresponding drain saturation current I_{DSS} . To each temperature corresponds a unique current value. A preliminary calibration phase must be performed. It consists in imposing different uniform temperatures to the transistor and measuring I_{DSS} values.

B. Application of the Infrared technique

We measure the surface temperature after the gate edge at the drain side using the infrared thermography microscope QFI InfraScopeTM. The resolution is 1024x1024 pixels. The base plate temperature is regulated. At the point of measurement, there is only a 500 nm thick SiN passivation layer. So we are close to the "real" channel, under the gate. Moreover there is no low R_{TH} metal at this point to conduct and lower the temperature.

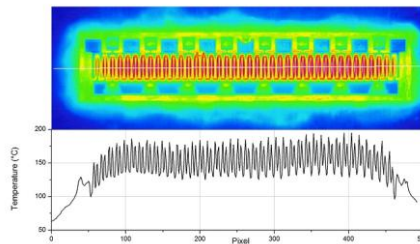


Figure 5- Evolution of the temperature cartography along the transistor (white line).

Figure 5 shows an example of the temperature's evolution along the transistor when it dissipates 45 W DC power and the base plate temperature is maintained at 45°C.

The channel temperature is globally uniform. Except for the ten extreme fingers (at the right or at the left) for which the temperature is about 30° lower. Figure 6 confirms the different thermal behaviour between central and peripheral fingers. It shows also the non linearity of the device's global thermal resistance.

From these measurements, we deduced a thermal resistance of $3.0^{\circ}\text{C}/\text{W}$. The corresponding DC dissipated power is 45 W and the base plate temperature is 45°C . For comparison, the manufacturer's datasheet gives a value of $3.2^{\circ}\text{C}/\text{W}$, in similar conditions.

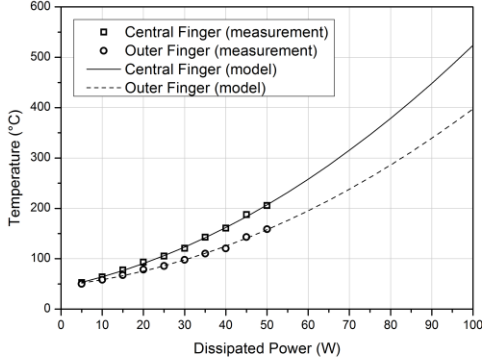


Figure 6. Non linearity of the transistor's thermal behaviour (points: measurements, line: model).

C. Application of the electrical technique

We adapt here the Joh et al. [23] technique to our transistors which have large gate widths ($80 \times 200 \mu\text{m}$). During the calibration phase, V_{DS} is maintained constant and V_{GS} is pulsed. Low value is pinch-off voltage V_{P} and high value is 0 V. The objective is to minimise the transistor self-heating. Due to the large gate periphery of our devices and thus the weak contribution of these edge effects, we assume that the channel temperature is quasi uniform.

As explained above, the calibration phase is obtained by imposing variable temperature T to the transistor and measuring the I_{DSS} current. We measured short drain pulses when the base plate temperatures is varied in the 30°C to 140°C range with a 10°C step. The pulses' width was chosen sufficiently small to avoid the transistor's self-heating and not alter the measurement. The pulses' width was $2 \mu\text{s}$ and the repetition rate was 1 ms.

Figure 7 shows the calibration characteristic with a constant negative slope ($-8.4 \text{ mA}/^{\circ}\text{C}$) on the whole calibration range.

After the calibration phase, the transistor was measured in the operational conditions (with the self-heating). Pulses with $200 \mu\text{s}$ width were applied to the gate. In figure 8, we present the transient response to a pulse of 25 W of dissipated power.

The response is exponential with a saturation value of 84.8°C (reached after $450 \mu\text{s}$) and a time constant of $100 \mu\text{s}$.

In the same conditions with the infrared technique, we obtained 85.9°C . Both techniques lead to the same value.

In conclusion, infrared technique has an advantage for spatial analyze, while the electrical technique have an advantage for transient analyze of temperature. So, we have

coupled both techniques for our physical analyses.

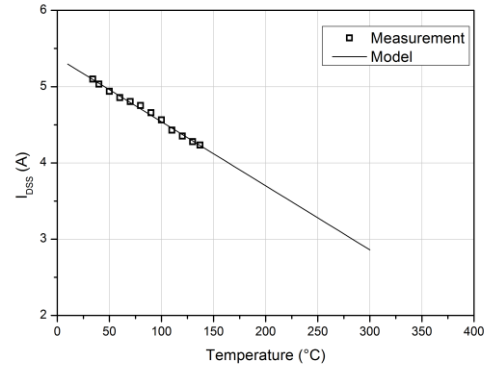


Figure 7- Temperature calibration characteristic.

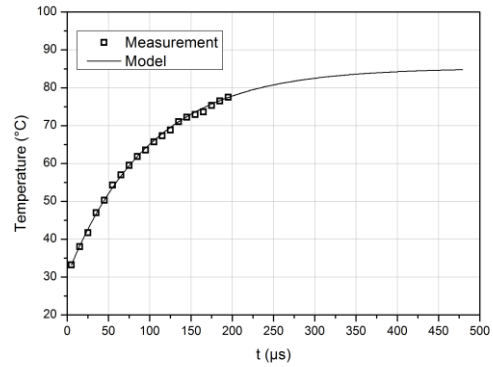


Figure 8. Transient temperature response to a pulse of 25 W dissipated power.

D. Application to degradation analysis

To compare the effect of temperature and electrical constraints, we estimate the channel temperature (during the RF pulse, figure 9) and the maximum drain voltage reached during the ageing tests, for different bias conditions (table 7). The maximum drain voltage is theoretically (and confirmed by simulations) equal to $2V_{\text{DS0}}$. Table 7 shows clearly that the tests with the highest temperature, are $43 \text{ V}-0 \text{ mA}$ and $45 \text{ V}-200 \text{ mA}$. These tests are also the ones with higher variations of P_{OUT} , I_{D} and I_{G} , and the most important evolution of the gate characteristics (figure 8). The correlation between these evolutions and the channel temperature appears clearly. On the other hand, no clear correlation could be established with the maximum electrical constraint (Table 7).

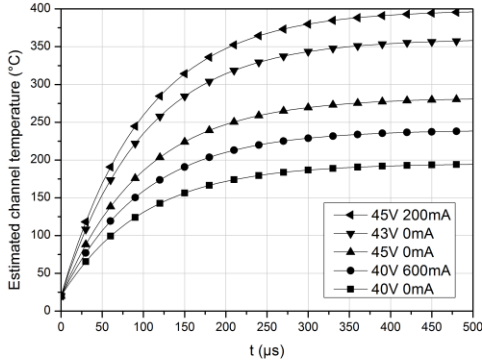


Figure 9. Estimation of channel temperature ($t=0$ corresponds to the pulse start, pulse width= $450 \mu\text{s}$) for $P_{IN}=39.5 \text{ dBm}$ input power and different bias conditions.

For example, comparison shows that the test with 43 V-0 mA has a higher maximum temperature than in 45 V-0 mA test. It is related to lower power efficiency for 45 V. Degradation of electrical performances (Table 2) is also higher for 43 V in spite of lower voltage swing.

TABLE 7: CHANNEL TEMPERATURE AND MAXIMUM DRAIN VOLTAGE DURING THE AGEING TEST.

Bias	Maximum channel temperature (°C)	Maximum drain voltage (V)
40 V-0 mA	194	80
40 V-600 mA	237	80
45 V-0 mA	280	90
43 V-0 mA	356	86
45 V-200 mA	394	90

E. Additional thermal study

To complete this study, two transistors were tested in a thermally regulated oven. The objective was to have more conclusive elements on the thermal degradation assumption.

Two new transistors which had been submitted to no ageing test were stored at 250°C during 200 hours, and then at 300°C , during 200 hours again. DC I-V characteristics were measured and compared to the reference device to detect any evolution.

Globally, the sign of variation of studied parameters confirms the thermal impact observed with RF ageing tests. Quantitatively, the pinch-off voltage V_p variations go over the RF ageing tests ones. Many reasons could explain this observation:

- Even for high reached temperature during ageing test (over 300°C), this temperature is not in a steady state as in thermal storage.

- During RF tests, another phenomenon is possibly added to thermal effects which induce a V_p shift towards positive values. Globally we possibly observe both effects. Here conditions are in real mission profile like in radar applications.

We remind that the originality of this work is not to compare or decorrelate the consequence of one parameter like temperature, off-state, or DC stress, but it is in real life with radiofrequency in pulse mode where the high power amplifier is stressed both by electrical and thermal conditions in operating conditions.

- Thermal degradations during RF ageing tests are possibly not uniform. In thermal storage, temperature distribution is however uniform.

Finally, we observed that the degradations are irreversible.

To detect a possible contribution of trapping effects in transistor's ageing, some devices were tested on the ageing bench and relaxed, and were again characterized in DC. Their package was opened and the die was illuminated with sunlight. Finally their I-V characteristics were measured.

We observed that pinch-off voltage V_p grew continuously during relaxation, while the transconductance remained unchanged. This behavior, in the absence of electrical or thermal constraints, means the presence of electrical charges trapped in the substrate.

The shift of V_p to negative values is compatible with posterior liberation of trapped charges accumulated during the RF ageing tests in the substrate and/or in surface layers.

VI. PHYSICAL ANALYSIS

We present here a synthesis of results partially published elsewhere [10, 11, 13]. Physical analysis results complete our previous conclusions and show how the thermal constraint deteriorates aged devices.

A. Visual inspection

The visual inspection with optical microscope shows, for aged devices, a granular appearance and cracks in metallic zones. This observation is confirmed by the Scanning Electron Microscope (SEM). Surface of metallic zones appeared strongly and densely crackled (figure 10). Thermal cartography (figure 11) put in evidence that the localization of the most crackled zones (figure 11a) corresponds to the zones with the highest self-heating (figure 11b). It proves that the texture changing is related to source and drain finger's temperature. It is also related to the difference between gold and semiconductor thermal expansion coefficients. Thermal expansion coefficients of GaN and Si are respectively $3.4 \cdot 10^{-6} \text{ K}^{-1}$ [29] and $2.5 \cdot 10^{-6} \text{ K}^{-1}$ at 300 K [30]. The Au one is $14.2 \cdot 10^{-6} \text{ K}^{-1}$. For example for a channel temperature of 350°C (compatible with estimated values, table 7), the dilatation difference between Au and GaN, for a $200 \mu\text{m}$ finger, is around $0.77 \mu\text{m}$.

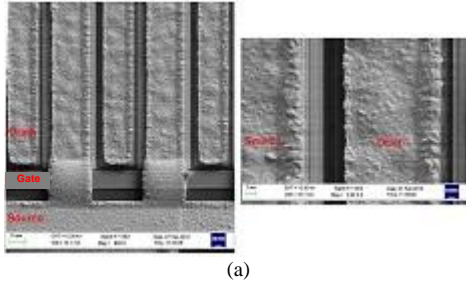


Figure 10- SEM picture of source and drain metallic zones in (a) fresh and in aged and (b) degraded transistor.

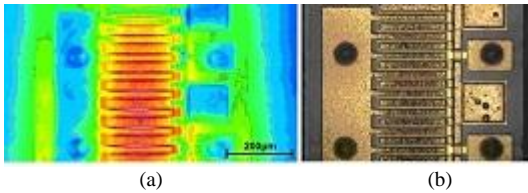


Figure 11 - Comparison between the (a) distribution of temperature and (b) granularity of source and drain metallic zones

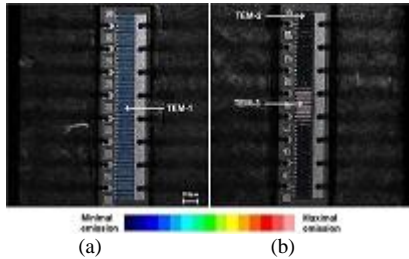


Figure 12- EMMI picture of (a) a fresh and (b) an aged transistor: 3 TEM lamellas are sampled. Picture example of EMMI concerns $V_{DS}=20$ V and $I_D=100$ mA. (a): drain current (and pinch-off voltage) is uniform on all gate fingers, (b): drain current is higher at center fingers and lower at the edge. TEM-1, TEM-2 and TEM-3 are the samples extracted for micro-structural analyses.

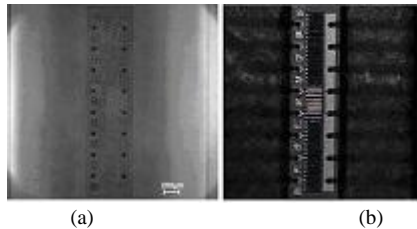


Figure 13- Pictures of (a) RX and (b) EMMI of the degraded transistor after pulsed RF ageing at $V_{DS}=45$ V and $I_D=200$ mA. Picture example of EMMI concerns $V_{DS}=20$ V and $I_D=100$ mA.

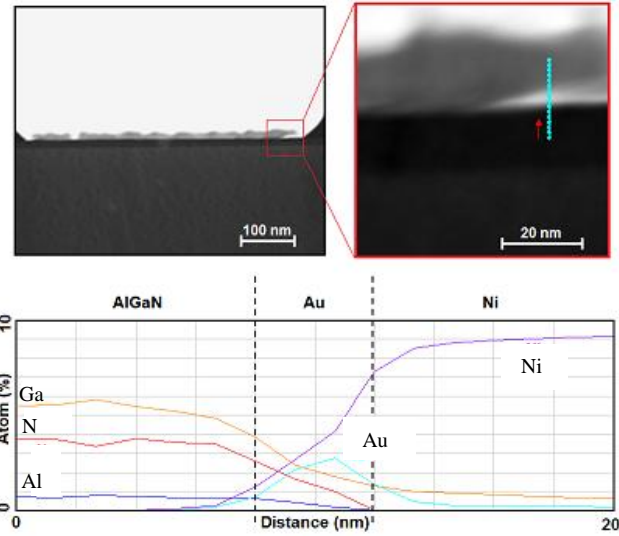


Figure 14- EDS measurement (across the blue line) of the degraded Schottky contact of an aged component, (at TEM-3). It shows a migration and inclusion of gold (Au) in the Ni-semiconductor Schottky contact

B. Localization of defects by non destructive techniques

The most interesting observation concerns devices observed with Photon EMISSION Microscopy (EMMI) with a bias close to pinch-off voltage ($V_p=-1.8$ V). Only the results relative to the 45 V-200 mA biased stressed device are presented here even if great similarities have been noticed on other aged devices. For this aged device and at $V_{DS0}=20$ V and $I_{D0}=100$ mA ($V_{GS0}=-1.35$ V) bias point, EMMI pattern showed that the more intense emission is focused in the central zone for aged devices (figure 12b). For fresh devices and at the same bias point, it is spread uniformly (figure 12a). It means that central fingers have a pinch-off voltage which has decreased. The correlation with the temperature concentration and increase on these fingers is obvious. Moreover, X radiography showed a degradation of the brazing on the aged components bottom. Voids are larger and bountiful in the zones detected by EMMI (figure 13). The phenomenon worsens the temperature effect because of more difficult heat flow at the points where the brazing is degraded.

C. Micro-structural analysis of degradations: TEM and FIB

This part concerns the transistor aged under 45V-200mA (in sections III and IV). Three thin lamellas were extracted: respectively TEM-2 and TEM-3 on an external finger (low thermal strain) and on a central finger (high thermal strain) of an aged transistor, and TEM-1 is a reference sample on a fresh device. Figure 11 depicts these three areas with the related Photo EMISSION Microscopy (EMMI) in DC bias conditions. The micro-structural analysis revealed an important

degradation of the Schottky contact (inter-metallic diffusion Au/Ni) [11]. The degradation is coherent with temperature (uniform degradations along the gate, more intense in the hot zones). This structural modification is also coherent with the electrical evolution of the contact (see paragraph IV-B).

No noteworthy degradation was observed on the source and drain ohmic contacts or on the interface between passivation and semiconductor layers. No degradation as "channel diffusion" or "delimitation" which could cause surface trapping was either observed. It is in agreement with electrical measurements.

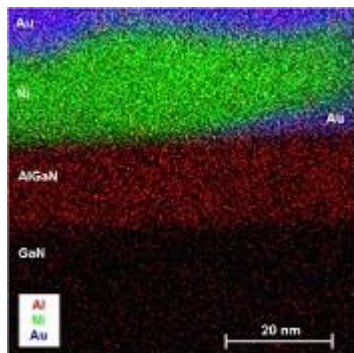


Figure 15- EDS cartography of the degraded Schottky contact of an aged component, (at the gate edge and on the drain side). It confirms the gold (Au) migration in the Ni contact.

It is confirmed by chemical cartography (figure 15). An EDS analysis was performed on the TEM-3 sample. Results are shown in figure 14. They highlight a migration and inclusion of gold (Au) in the Ni-semiconductor Schottky contact. That explains the barrier height decrease compared to a homogeneous Ni-semiconductor contact. It is also in good agreement with electrical characterization. These degradations are irreversible.

VII. CONCLUSION

Failures mechanisms in AlGaIn/GaN HEMT RF power amplifiers based on silicon substrate have been analysed in radar operating conditions. Several prototypes have been designed, fabricated, characterized and tested by means of ageing tests performed in conditions as close as possible to the real application.

Moreover, we observed that the transistor hold out to high temperature is not related only to good physical properties of GaN, but also to the quality of interfaces in the component. It proves that the gate contact is the most sensitive region to temperature in the transistor. Thermal properties of substrate are therefore critical. The studied transistor was based on silicon substrate. We remind that silicon has a low thermal conductivity. This fact was considered with particular

attention. Another element specific to GaN is the existence of trapping effect, which was also evaluated.

Ageing under increased drain voltage allows studying both aspects simultaneously. Different characterizations performed after ageing tests led us to some assumptions on the degradations (partially irreversible) nature. It was proved that they are due to thermal stress for the irreversible part and to trapping effects for the reversible one. These assumptions were confirmed by additional physical analysis. Results revealed strong modifications of the Schottky contact, which explains the evolution of electrical parameters too.

Photons Emission Microscopy associated to X radiography gives spatial correlation between degradations of the gate and the evolution of the interface braze between the transistor chip and its packaging. The more numerous braze vacuums cause locally a thermal resistance increase, appearance of overheating points and acceleration of Schottky contact degradation.

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