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Abstract -- This paper deals with reconfigurable back-to-back converter topology and control orders in Wind Energy Conversion Systems (WECS). A typical WECS with Doubly Fed Induction Generator (DFIG) in balanced conditions is concerned. Based on the classical topology, a fault tolerant converter without any redundancy has been studied. The presented fault tolerant topology allows a "five-leg" structure with converters reconfiguration after switch failure detection. Furthermore, the control strategy for classical topology can no longer be applied after fault occurrence. Thus, a "five-leg" control strategy has also been proposed. The validation of the reconfigurable digital controller for the studied WECS with DFIG topology has been performed using a Hardware-in-the-Loop (HIL) reconfigurable platform including a Field Programmable Gate Array (FPGA) chip. HIL simulation results in both healthy and fault conditions have been presented to show simultaneously the viability of the studied converters topology and the reconfigurable control.

Index Terms-- Wind energy, DFIG, fault tolerant converters, reconfigurable back-to-back converter, switching of control orders, FPGA, switch failure.

I. INTRODUCTION

At the end of 2011, the installed wind power in Europe was around 97 GW [1]. According to European wind energy association, wind turbines could provide 49% of EU electricity in 2050 [2]. Global market of wind energy is clearly expanding steadily, and consequently the technologic competition in this area has been accelerated. The demand for continuously available power electronics systems is increasing. Most loads that are fed by power systems require non-stop and fault tolerant operation. Wind Energy Conversion Systems (WECS) are typical application cases where the efficient production is directly linked to economic benefits [3], [4]. More particularly, WECS are sensitive to power switch failure. A sudden failure in one of the power switches decreases system performance and can lead to disconnection of the power system. More, if the fault cannot be quickly detected and compensated, it can lead to hardware failure. In [5], a power switch failure detection for three-leg fault tolerant converter topology has been developed. This approach minimizes the time interval between the fault occurrence and its diagnosis. The possibility to detect a faulty switch in less than 10 µs by using a diagnosis simultaneously based on a "time criterion" and a "voltage criterion" has been demonstrated. In order to perform such a short detection time, a Field Programmable Gate Array (FPGA) fully digital implementation has been used. A fault tolerant "six-leg"

converter topology with one redundant leg and a Doubly Fed Induction Generator (DFIG) for WECS has also been studied [5]. The fault detection scheme and the compensation algorithm have also been implemented into a FPGA target. By implementing a redundant leg, the applied control strategy remains the same for both healthy and faulty operation modes, because the converters topology remains a "six-leg" structure after the fault detection and compensation.

Five-leg converter topology has already been proposed for drive applications such as independent control of two three-phase motors [6] or AC/AC supply of a three-phase induction machine [7]. It has been shown that this converter topology could give satisfactory results in such applications. However, in post-fault operation, the DC bus voltage value has been doubled to preserve the maximum power capability of the drive. However, doubling the current and voltage implies that the power switches ratings must be four times greater than those in healthy operation. Such high switch ratings results high additional costs. Accordingly, the authors have proposed to reduce the power level of the post-fault configuration to a suitable value and provide only the balanced operation of the drive. In this case, the power switches ratings could be the same as in normal operation. However in a WECS case, it is not possible to change instantaneously the active power level in post-fault operation by updating the reference rotational speed in controller. Because the electromechanical time constant of the wind turbine is much larger than the electric time constant of the DFIG [8]. In [9], a five-leg converter control has been studied for a WECS in normal operation mode. However, as far as WECS with DFIG is concerned, the applications of such a reconfigured "five-leg" converter in switch fault operation with the associated FPGA-based reconfigurable control have never been reported in the literature. Such a converter topology might be interesting and efficient for this purpose.

This paper proposes a FPGA-based reconfigurable control for "six-leg" fault tolerant converter topology without redundancy, which can be used in WECS with DFIG. The fault tolerant topology and the associated control give the possible switch failure fault tolerance capability. Compare to classical "six-leg" converter used in WECS with DFIG, the proposed fault tolerant converter requires three additional bidirectional devices. After switch fault detection and converter reconfiguration, the converter becomes a "five-leg" topology. Thus, the control strategy for "six-leg" configuration in healthy condition can no longer be applied to this "five-leg" structure and must be reconfigured as quickly as possible. For this purpose, a fast fault detection method developed in [3] has been used. Moreover, in order to perform fast fault detection and control reconfiguration, the entire digital control has been implemented into a single FPGA target [10]. The FPGA implementation offers many advantages: possibility of reducing the sampling period, insensitive to disturbance, the possibility of full integration of control system in a single control board and rapid reprogramming [11].

In the next section, the proposed converter topology has been presented. The proposed method that uses a common leg after the fault detection has been explained. Reconfigurations of converters in the cases of an open-circuit and short-circuit faults have also been discussed. After that, the reconfigurable control to switch from the classical control for a six-leg converter to the new control for the five-leg converter has been detailed. At last, experiments in healthy or faulty conditions using "FPGA in the Loop" hardware implementation have been presented and carefully discussed.

II. FAULT TOLERANT SIX-LEG CONVERTER TOPOLOGY WITHOUT REDUNDANCY

A. Fault Tolerant Converter Topology

The classical WECS, with a horizontal axis wind turbine and an indirect controlled 3MW DFIG with Maximum Power Point Tracking (MPPT) and pitch controls has been used in this

study [12-13]. The proposed fault tolerant WECS with DFIG, without power switch redundancy, is shown in Figure 1. The power converter is based on the classical "six-leg" topology, which is composed by 12 semiconductors (S_i and $S_{i'}$) and 12 anti-parallel diodes (D_i and $D_{i'}$), with i = {1, 2, 3, 4, 5, 6}.

Figure 1. Fault tolerant WECS with DFIG without power switch redundancy.

Compared with the classical one, the proposed fault tolerant converter topology includes also fast active fuses (f_i and $f_{i'}$) and three additional current bidirectional switches T_k (k = {1, 2, 3}). After the fault occurrence and detection of a power switch, the reconfigured converter topology becomes a "five-leg" structure with a common leg shared by the Rotor Side Converter (RSC) and the Grid Side Converter (GSC). It should be noted that fast acting fuses are connected in series with each power switch in the proposed fault tolerant topology (Figure 1). In the case of an open-circuit, the isolation is implemented by removing the gate signal from the switches of the faulty leg. In the case of a short-circuit, the faulty leg is isolated by the very fast acting fuses. The role of fuses and their selection criteria regarding corresponding drivers will be discussed later in this paper. In both cases, the isolation is implemented by removing the gate signals from the switches of the faulty leg. In summary, the fault compensation is achieved by the following steps:

- detection of the faulty leg,
- removing the control orders of the faulty leg,
- triggering the suited bidirectional switch T_k,
- adjust or not the DC bus voltage depending on the DFIG speed,
- changing the PWM control for both RSC and GSC,
- stopping the fault detection scheme.

B. Common leg connection after fault detection

An equivalent circuit per phase for the RSC and the GSC is presented in Figure 2. R_f and L_f are, respectively, the resistance and the inductance of the RL filter and $e_{k'n}$ is the phase grid voltage. R_r and L_r are the resistance and the cyclic inductance, respectively; e_{rkm} is the electromagnetic force depending on the DFIG speed. Points n and m correspond to the neutral connections of the grid and DFIG's rotor, respectively.

Figure 2. Equivalent circuit per phase for the RSC and the GSC.

Depending on the considered switch failure case (open-circuit or short-circuit), the scheme of the reconfigured converter topology is not the same. The both fault cases are discussed for the GSC. A similar analysis could be made for the RSC.

1) Case of an open-circuit fault

In the $S_{k'}$ open-circuit fault case, the switching orders of the faulty leg k' are removed but the leg is not disconnected from the DC bus due to the anti-parallel diodes. The faulty leg is noted by the number k', the common leg is noted by the number k. The other legs i, j and i', j' ($i \neq j \neq k \in \{1, 2, 3\}$) operates normally. The common leg connection after the fault detection in open-circuit fault case is shown in Figure 3.

As shown in this figure, the current i_{cl} in the common leg can be expressed by:

$$i_{cl} = i_{rk} - i_{fk'} + i_D \quad (1)$$

Figure 3. Common leg connection in open-circuit fault case on $S_{k'}$.

2) Case of a short-circuit fault

The equivalent circuit just after the appearance of a short-circuit fault of the switch $S_{k'}$ is shown in Figure 4(a). When the switch $S_{k+3'}$ becomes on-state, capacitors of the DC bus are short-circuited by the faulty leg *k'* (Figure 4(b)). This case is dangerous, thus a reliable protection must be used to isolate the faulty leg. Some possible locations of fuses in voltage source converters have been discussed in [14]. Moreover, several tests with short-circuit of IGBT have been performed to study the rupture phenomena and examine how a fuse protects an IGBT [15]. These papers demonstrated that one fast acting fuse in series with each IGBT can efficiently protect it against overcurrent. Drivers in the GSC have an internal protection against short-circuit for each leg of the converter. The fault inhibition time of the drivers, the order of several microseconds, is often adjustable by external passive components to drivers. This inhibition time must be chosen to be greater than the fuses clearing time during the experimental implementation of the fault tolerant topology without redundant leg.

After the DC bus short-circuit occurrence (Figure 4(a)), different cases could occur depending on the fuses clearing time and the fault detection time. However, if the clearing time of fuses is smaller than the chosen fault detection time, the faulty leg is isolated by its fuses, before fault detection. Thus the faulty leg current and the phase current become zero. By this way, a short-circuit fault case becomes an open-circuit fault case.

Figure 4. (a) Equivalent circuit for the GSC phase *k'* in short-circuit fault of $S_{k'}$ ($k = \{1, 2, 3\}$).
(b) Short-circuit current path just after the fault occurrence.

Thus, for the connection of the common leg in the $S_{k'}$ short-circuit fault case, the faulty leg is firstly disconnected from the DC bus by the fuses and the switching orders of the faulty leg *k'* are then removed after the fault detection. The faulty leg is noted by the number *k'*, the common leg is noted by the number *k*. The other legs *i*, *j* and *i'*, *j'* ($i \neq j \neq k \in \{1, 2, 3\}$) operates normally. The connection of the common leg after the fault detection in a short-circuit fault case is shown in Figure 5.

As shown in this figure, the current in the common leg i_{cl} can be expressed by:

$$i_{cl} = i_{rk} - i_{fk'} \tag{2}$$

Figure 5. Common leg connection in short-circuit fault case on $S_{k'}$.

In short-circuit case, the current i_{cl} only depends on the currents i_{rk} and $i_{fk'}$.

C. Fault detection scheme

The power switch fault detection is based on the comparison between the measured and estimated pole voltages, v_{k0}, respectively noted v_{k0m} and v_{k0es}. With ideal switches considerations, a fault occurrence can be determined by using a comparison between the measured and estimated pole voltages. However, in real case, due to the turn-off and turn-on propagation times, the interlock dead time generated by the switches drivers and the delay time introduced by the Analog-to-Digital converters and the voltage sensors, the voltage error ε_{io} (($i = \{k, k'\}$ avec $k = \{1, 2, 3\}$) is not null: This error is composed of peaks during switching times. To avoid false fault detections due to power semi-conductors switching, a fault detection scheme using simultaneously a “time criterion” and a “voltage criterion” has been used (Figure 6).

Figure 6. Fault detection scheme.

With this fault detection scheme, the fault can be detected in several tenths of microseconds. The resulting signal f_i from the fault-detection scheme is used to remove the switching orders of the faulty leg, connect the faulty leg to the common one by triggering the suited bidirectional switch T_k and stop the fault detection scheme (with $i = \{k, k'\}$ and $k = \{1, 2, 3\}$). This method has been detailed in [5].

III. RECONFIGURABLE FAULT TOLERANT CONTROL

A. Principle

When a power switch fault occurs, the reconfigured converter topology (Figure 1) becomes a "five-leg" structure. Thus, the same control strategy can no longer be applied. A suitable "five-leg" PWM control should be applied depending on the fault location and the chosen common legs k or k' ($k = \{1, 2, 3\}$).

The proposed reconfigurable fault tolerant controller is shown in Figure 7. In healthy conditions, the "fault detection and compensation" block directly applies the switching patterns, determined by the "PWM" blocks of the RSC and GSC controllers, noted by δ_k and $\delta_{k'}$ respectively ($k = \{1, 2, 3\}$). The RSC and GSC controllers are based on a horizontal axis wind turbine model with MPPT and pitch control. For the modeling of the DFIG, the classical model in the Park reference frame has been used [12-13]. The generator used in the studied WECS is controlled to provide active and reactive powers to the grid with a constant frequency and a unity power factor capability. The PWM used in healthy conditions is a classical three phase PWM with a triangular carrier.

Figure 7. Reconfigurable fault tolerant control.

When a faulty switch has been detected, a common leg, noted q, becomes common for both RSC and GSC. The reconfigured converter topology with the faulty leg k or k' is presented in Figure 8.

Figure 8. Reconfigured converter topology when the leg k or k' is faulty.

In this figure, four phase to phase voltages can be used to control four currents: two for currents of the DFIG and two for the currents of the connection of GSC to the grid.

In healthy conditions, the RSC deliver to DFIG's rotor the voltages u_{riq} and u_{rjq} with a pulsation ω_r while the GSC deliver to the grid the voltages $u_{fi'q}$ and $u_{fj'q}$ with a pulsation ω_s. The voltages delivered to the DFIG have variable amplitudes and pulsations because the WECS operates at variable speed. A vector description of these different voltages with a potential related to the common leg q is illustrated in Figure 9. This figure shows that the maximal phase to phase voltages are the sums of the voltages u_{riq} and u_{rjq} with $u_{fi'q}$ and $u_{fj'q}$ respectively. Thus, after compensation of the converters, these voltages must not exceed the DC bus voltage v_{dc}. Therefore, depends on the operating point of the wind turbine (hyper or hypo synchronous mode of the DFIG with a slip between ± 30%), it might be necessary to increase the DC bus voltage in order to guarantee the same performances as before the fault. Increasing the DC bus voltage could be done by modifying the corresponding reference in the GSC control. The DC bus voltage level to be applied to five-leg converter depends on the operating point of the DFIG. The choice of this value will explain in the section IV.B.3.

Figure 9. Vector description of RSC and GSC voltages after the fault compensation.

B. Choice of the common leg

After the connection of the current bidirectional device related to the faulty leg k or k', a common leg q at RSC and GSC must be chosen, depending on the faulty leg (Figure 8). If the faulty leg is the leg k, the common leg q is the leg k'. Inversely, if the faulty leg is the leg k', the common leg q will be the leg k. Moreover, four reference phase to phase voltages u_{riq}^{*}, u_{rjq}^{*}, $u_{fi'q}^{*}$ and $u_{fj'q}^{*}$, relative to the common leg (with $i \neq j \neq k \in \{1, 2, 3\}$ and $q \in \{k, k'\}$) must be generated for the five-leg PWM in order to control the new converters topology. The generation of these different reference phase to phase voltages according the faulty leg k or k' and the common leg q is illustrated in Figure 10.

Figure 10. Reference line to line voltages according the common leg q.

Once the reference voltages v_{rim}^{*}, v_{rjm}^{*}, $v_{fi'n}^{*}$ and $v_{fj'n}^{*}$ are chosen according the faulty leg k or k' ($i \neq j \neq k \in \{1, 2, 3\}$), the reference phase to phase voltages u_{riq}^{*}, u_{rjq}^{*}, $u_{fi'q}^{*}$ and $u_{fj'q}^{*}$, can be generated. Considering that the grid and DFIG phases are balanced with a Y coupling (Figure 8), the phase q can be chosen as reference for the generation of phase to phase voltages. So, from the Figure 8, it can be written:

$$\begin{cases} v_{rim}^{*} + v_{rjm}^{*} + v_{rqm}^{*} = 0 \\ v_{fi'n}^{*} + v_{fj'n}^{*} + v_{fqn}^{*} = 0 \end{cases} \tag{3}$$

As the phase q is chosen as reference, the reference phase to phase voltages u_{riq}^{*}, u_{rjq}^{*}, $u_{fi'q}^{*}$ and $u_{fj'q}^{*}$, for the DFIG and the grid connection respectively, can be expressed by using the last reference voltages:

$$\begin{cases} u_{riq}^{*} = v_{rim}^{*} - v_{rqm}^{*} \\ u_{rjq}^{*} = v_{rjm}^{*} - v_{rqm}^{*} \\ u_{fi'q}^{*} = v_{fi'n}^{*} - v_{fqn}^{*} \\ u_{fj'q}^{*} = v_{fj'n}^{*} - v_{fqn}^{*} \end{cases} \tag{4}$$

From equations (3) and (4), a transform matrix can be defined to express the phase to phase voltages:

$$\begin{bmatrix} u_{riq} \\ u_{rjq} \\ u_{fi'q} \\ u_{fj'q} \end{bmatrix}^{*} = \begin{bmatrix} 2 & 1 & 0 & 0 \\ 1 & 2 & 0 & 0 \\ 0 & 0 & 2 & 1 \\ 0 & 0 & 1 & 2 \end{bmatrix} \begin{bmatrix} v_{rim} \\ v_{rjm} \\ v_{fi'n} \\ v_{fj'n} \end{bmatrix}^{*} \tag{5}$$

C. Five-leg PWM

The generation of the control orders δ_i, δ_j, $\delta_{i'}$, $\delta_{j'}$ and δ_q of top switches of different legs (Figure 8) is mainly based on the method published in [7], [16]. In fact, the switching orders are generated from the reference phase to phase voltages u_{riq}^{*}, u_{rjq}^{*}, $u_{fi'q}^{*}$ and $u_{fj'q}^{*}$ as shown on Figure 11. The first operation consists to divide by the DC bus voltage v_{dc} different reference phase to phase voltages from equation (5) in order to obtain four voltages in per unit, which

are necessary for the comparison with triangular carriers. These voltages in per unit are defined by:

$$\begin{bmatrix} < m_i > \\ < m_j > \\ < m_{i'} > \\ < m_{j'} > \end{bmatrix}^* = \frac{1}{v_{dc}} \begin{bmatrix} u_{riq} \\ u_{rjq} \\ u_{fi'q} \\ u_{fj'q} \end{bmatrix}^* \quad (6)$$

Secondly, a specific PWM with two triangular carriers is used for a comparison with the previous signals in per unit (Figure 11). The obtained signals m_i^*, m_j^*, $m_{i'}^*$ and $m_{j'}^*$ can have three levels (-1: 0: +1) and are used to generate the signal m_{cod}, which is expressed by:

$$m_{cod} = 1 + \left(m_i^* + 1\right) + 3 \cdot \left(m_j^* + 1\right) + 9 \cdot \left(m_{i'}^* + 1\right) + 27 \cdot \left(m_{j'}^* + 1\right) \quad (7)$$

The values of signal m_{cod} vary between 1 and 81 according to the values of signals m_i^*, m_j^*, $m_{i'}^*$ and $m_{j'}^*$. Finally, the different control orders δ_i, δ_j, $\delta_{i'}$, $\delta_{j'}$ and δ_q are established with five Look Up tables (LUT).

Figure 11. Generation of the "five-leg" PWM.

In the following section, the implementation of the fault detection and compensation as well as the different PWM controls in a unique FPGA target is explained. The "FPGA in the loop" prototyping methodology we have used is summarized and the implementation is detailed [10].

IV. FPGA IN THE LOOP EXPERIMENTS

A Field Programmable Gate Array (FPGA) component to detect a faulty switch and reconfigure the converter and the control as quick as possible has been used. By using an FPGA, a faulty switch can be detected and cleared in a few tenths of microseconds with the possibility to modify rapidly the generation of control orders after the fault detection and reconfiguration of converters in "five-leg" topology.

Any errors during the implementation of algorithms on FPGA target may cause serious damage to the controlled system, usually very costly, and delays in the development of the first prototype. That's why a methodology for prototyping and experimental validation of the implementation of algorithms on FPGAs for electrical systems has been developed (for example: for an active power filter or a WECS in faulty conditions with a converters topology including a redundant leg) [3]. This first experimental validation allows to validate algorithms (different PWM controls and fault detection and compensation) implemented on FPGA while having the power part of the system emulated on a computer connected to the FPGA. This method of prototyping is called "FPGA in the loop". It is the same principle of Hardware In the Loop (HIL) simulation.

"FPGA in the loop" prototyping evaluates performances and weaknesses of control algorithms; these can be detected in this virtual environment while eliminating the risk of damage to all or part of the electrical system. The main reasons to use the "FPGA in the loop" prototyping for the study of the continuity of service in a WECS in the case of a faulty switch are:

- the power part of a WECS is not available,
- costs incurred by the construction of the power are very high,

- experimental tests involve significant risks for the overall safety of the operation (risk, large electrical power into play ...).

A. "FPGA in the loop" prototyping

In this section, the Top-Down design flow we have used to implement and validate the fully digital fault detection and the reconfigurable control orders is discussed.

"FPGA in the loop" prototyping methodology consists to validate step by step the modeling in different time modes (continuous and discrete) and the implementation of switching orders algorithms into the FPGA. The methodology is based on three principal stages, which are developed below:

- functional simulation,
- mixed simulation
- "FPGA in the loop" experiment.

1) Functional simulation

At this first stage of the design flow, the power part of WECS (DFIG, infinite electrical grid and fault tolerant converters topology) shown in Figure 1 and the sensors (mechanical and electrical) are modeled using the Matlab/SimPower Systems. The interfaces, RSC and GSC controls, the different PWM controls and the fault detection and compensation scheme, shown in Figure 7 have been modeled using Matlab/Simulink. The studied WECS is first modeled in the continuous-time mode and then in the discrete-time mode. In the functional simulation, the up-counter shown in Figure 6 is modeled by an integrator. The threshold value h in first comparator must be chosen equal to 3 at 5 % of DC bus voltage v_{dc} in order to eliminate offset near zero of voltage sensors.

For experimental tests with a real power part, the threshold value N_t must be chosen regards on:

- the time response of the voltage sensors used for the pole voltages measurements,
- the characteristics and performances of the analog data acquisition, mostly analog to digital converter and interface electronics,
- the dead time of the IGBTs' drivers.

However, in all simulations, sensors and interfaces of the power part are simulated with Matlab/SimPower Systems. Thus, the threshold value N_t will be chosen as the lowest as possible.

Thus, the values of the thresholds N_t and h are chosen, respectively, to be equal to 10 (corresponding to 10 μs) and 50 V.

After the validation of all WECS models by functional simulation in the continuous-time mode, the power part and the sensors of the WECS have been modeled with the Matlab/SimPower Systems in discrete-time mode with a time step equal to 1 μs. The interfaces, RSC and GSC controls and the fault-detection and compensation scheme have been modeled with Matlab/Simulink. The sampling period for RSC and GSC controls has been chosen to be equal to 1 ms. For different PWM controls and the fault-detection scheme, the sampling period is chosen to be equal to 1 μs.

Since the final results obtained for the functional simulation (continuous and discrete time mode), for the mixed simulation, and for the HIL simulation are identical, after having validated the control part in each stage according to the proposed top–down design flow, only HIL simulation results have been presented [5],[10].

2) Mixed simulation

Since only the fault detection and compensation scheme and different PWM controls (choice of common leg, classical and five-leg PWMs) have been implemented into the FPGA target in this paper, only these parts are modeled with the DSP Builder. The GSC and RSC

controls and the WECS power part model remain the same as the ones used in the functional simulation in discrete-time mode. The different input signals of different PWM controls and of fault detection and compensation scheme (Figure 7) are: the reference voltages delivered by RSC and GSC controls, noted v_{rk}^{*} and $v_{fk'}^{*}$, the DC bus voltage v_{dc} and the measured pole voltages v_{k0m} and $v_{k'0m}$., ($k \in \{1, 2, 3\}$) . Considering the A/D converters that we have used with 12-b resolution, the format of input voltages signals are chosen to be equal to [1, 0, 11] (i.e., 1 b for the sign bit and 11 b for the decimal part). It should be noted that in an experimental test bench, the interface modules reduce the value of the analog signals in the range [−1, +1]. The output signals from the fault detection and compensation scheme are the twelve switching patterns C_k, C_{k+3}, $C_{k'}$, $C_{k+3'}$ and the six fault detection signals f_k and $f_{k'}$. These output signals are logic signals, so the logical format is used with only two values, namely, 0 or 1. A single bit is used to encode these signals. The different PWM controls (choice of common leg, classical and five-leg PWMs) have been modeled with logics gates, comparators and Moore finites states machines. These last have been used in order to synchronize all control orders of RSC and GSC in healthy or faulty conditions.

The triangular carriers, necessary to PWM controls, do not exist in the DSP Builder library. Thus, a digital version of those carriers has been made, as shown in Figure 12. The signal is made from an up-counter, which generates a periodic ramp with an amplitude equal to A_{tr} and a period T equal to $(2^n\text{-}1)$ x T_e. n is the number of bits, depending of the desired switching frequency and T_e the sampling period, which is equal to 1 µs.

Figure 12. Digital triangular carrier used for PWM controls.

Moreover, a Moore finite state machine has also been used to model the fault detection scheme. The state diagram and the control unit of this fault detection scheme for RSC and GSC is illustrated in Figure 13. The up-counter is clocked by a clock pulse with a period T_h of 1 μs ($i = \{k, k'\}$ avec $k = \{1, 2, 3\}$). The values of the thresholds N_t and h have been chosen, , to be equal to 10 (corresponding to 10 μs) and 50 V, respectively.

Figure 13. (a) Moore finite state diagram for the fault detection scheme.
(b) Control Unit of the fault detection scheme.

3) HIL simulation

The reconfigurable platform is based on a DSP S80 development board, which includes a Altera Stratix EP1S80B956C6 FPGA chip. This FPGA contains 79 040 programmable logic elements, 679 user I/O pins, 12 reconfigurable fast PLLs, and 7.4-Mb RAM. The development board has also an on-board 80-MHz oscillator. To implement the fault detection and compensation scheme as well as the different PWM controls into the FPGA target, the following steps have been followed with Quartus II software:

- generation of the synthesizable VHDL code,
- logical synthesis,
- fitting.

At this step, all DSP Builder blocks have been replaced in the Matlab/Simulink environment by a single “HIL block” corresponding to the digital fault tolerant reconfigurable control implemented into the FPGA. The connection between the development board and the computer is done by using a ByteBlasterMV cable for FPGA programming. Figure 14 illustrates the last stage of the top-down design flow. In this case, at each sample time step (here equal to 1 µs), the FPGA receive from the PC the following signals: v_{rk}^{*}, $v_{fk'}^{*}$, v_{dc}, v_{k0m} and $v_{k'0m}$ then it executes the implemented algorithms and return to PC the following signals: C_k, C_{k+3}, $C_{k'}$, $C_{k+3'}$, f_k and $f_{k'}$ computed during this “FPGA in the loop” step ($k = \{1, 2, 3\}$).

Figure 14. HIL simulation platform.

B. HIL simulation results

The power specifications of the studied WECS are given in Table I. A wind speed of 13 m/s is applied on the blades of the turbine which corresponds to the nominal operation of the DFIG (P = -3 MW, N = 1950 tr/min and a 30% of slip in hyper synchronous mode). For the fully digital controller experiments with the FPGA (different PWM controls, fault detection and compensation), the up-counter (see Figure 6) has been clocked by a signal with a period of 1 µs, generated from an internal PLL and the threshold value N_t of the second comparator has been chosen to equal to 10 step (corresponding to 10 µs). The power part of the WECS has been emulated in discrete time mode with a sample time T_e equal to 1 µs. The RSC and GSC controls blocks have a sample time T_{ec} equal to 1 ms (see Figure 14). For the switching frequency of the RSC and GSC, number of bits n is fixed to 9 which corresponds to a frequency equal to 1957 Hz.

Table I. Mechanical and electrical parameters of fault tolerant WECS.

1) WECS in healthy conditions

In first step, the performances of the WECS with a fault tolerant converter without redundancy have been validated in healthy operation. For these simulations, the WECS operated in nominal conditions in the MPPT area. The reference voltage of the DC bus, noted v_{dc}^*, has been set to 1200V. The reference reactive power Q_f^* has been set to 0 VAr, to ensure an unity power factor at the connection point of the GSC with the electrical grid. On the other side, the stator reactive power Q_s varies regarding on its reference value in the RSC control.

A wind speed of 13 m/s (corresponding to the nominal conditions of the wind) has been applied on blades of the turbine, which corresponds to a rotational speed of the DFIG equal to 1950 tr/min (slip equal to -30% in hyper synchronous mode), as shown in Figure 15. The temporal evolutions of different electrical powers of the WECS are shown in Figure 16.

Figure 15. Healthy operation of WECS: DFIG rotational speed, DC bus voltage, *dq* rotor currents.

Figure 16. Healthy operation of WECS: different active and reactive powers of the WECS.

Before the time t = 0.6s, the WECS operates at unity power factor because the reference reactive powers Q_s^* and Q_f^* are equal to 0 VAr, which implies a reactive power provided by the WECS equal to 0 VAr. It is noted that, in this time interval, only the rotor reactive power Q_r is not equal to 0 VAr. In fact, the DFIG requires a reactive power necessary to its magnetization and, as the stator reactive power is equal to 0 VAr, the DFIG consumes reactive power from the rotor. In interval time between t = 0.6s and t = 0.8s, reference stator reactive power is set to – 1 MVAr (Figure 16), which corresponds to the references changing in the rotor current i_{rd} (Figure 15) and rotor reactive power Q_r. In the time interval between t = 0.8s and t = 1s, reference stator reactive power is set to 1 MVAr (Figure 16). It can be observed a little variation of DC bus voltage due to the important variation of rotor reactive power. In fact, the rotor powers are not decoupled as the stator powers in the RSC control, a change of rotor reactive power involves a variation on the rotor active power and then on the DC bus voltage, although the power compensation in the GSC control is achieved to attenuate the DC bus voltage variations. It is noted that the active and reactive powers and the DC bus voltages are well regulated near their reference values.

2) Operation of WECS in faulty condition without fault detection

The same wind speed as in the previous case has been applied on the blades of the turbine. The WECS operated in nominal conditions (P = -3 MW with N_m = 1950 tr/min). It is the worst case for the apparition of an open-circuit or a short-circuit fault on one of the power switches. In fact, consequences for the WECs are more important:

- a variation of the provided power to the grid, so a possible change in frequency if the WECS power is not negligible compared with the electrical grid,
- significant current transients can cause the destruction of mechanical and electrical systems,
- an apparition of a reactive power can result in the voltage variation at connection point with the grid.

The obtained results without fault detection and compensation are shown in Figure 17 in the case of an open-circuit fault on switch S_3 of the leg 3 of RSC at the time t = 0.62s.

Figure 17. Effect of an open-circuit fault on switch S_3 of RSC without fault detection and compensation.

3) Operation of WECS in faulty conditions with fault detection and compensation

In order to validate the performances of the fault detection and compensation scheme, the control changing between the both PWM controls in healthy conditions and the "five-leg" PWM control in faulty conditions, two open-circuit faults on the GSC have been studied:

- case *(a)*: $S_{3'}$ is faulty when $i_{f3'} < 0$ at t = 0.6s,
- case *(b)*: $S_{3'}$ is faulty when $i_{f3'} > 0$ at t = 0.61s.

"HIL simulation results" for the case (*a*) are shown in Figure 18. It can be observed that the waveforms are not affected by the presence of this fault, and the WECS can continue to provide electrical power to the grid in nominal conditions. In this case, it is not necessary to increase the DC bus voltage because the rotor voltages v_{rkm}^* are weak as the DFIG operates in hyper synchronous mode with a slip of -20% (about 20% of stator voltages v_{skm} if losses are negligible and with a turn ratio near to one. Thus, maximal values of additions of reference phase to phase voltages (u_{riq}^*, $u_{fi'q}^*$) and (u_{rjq}^*, $u_{fj'q}^*$) necessary for the five-leg PWM are lower than the DC bus voltage (here equal to 1200 V). The zoomed previously results on a duration of 400 µs are presented in Figure 19. In this figure, it is noted that $\delta_{3'}$ is equal to 1 at the time where the fault on $S_{3'}$ appears. The fault is then detected and compensated 10 µs after its apparition [5].

Figure 18. Case *(a)* with fault detection and compensation of an open-circuit fault when $i_{f3'} < 0$: fault on $S_{3'}$ at t = 0.6s.

Figure 19. Case *(a)* with fault detection and compensation of an open-circuit fault when $i_{f3'} < 0$: Zoomed result of Figure 18.

"HIL simulation results" for the case (*b*) are shown in Figure 20. It should be noted again that WECS operates at nominal conditions with the presence of a fault on $S_{3'}$. However, the DFIG operates in hyper synchronous mode with a slip equal to – 30%, it is necessary to increase the DC bus voltage in order to guarantee the same performances after the fault compensation. In fact, for this operating point and before the fault on $S_{3'}$, additions of reference line to line voltages (u_{riq}^*, $u_{fi'q}^*$) and (u_{rjq}^*, $u_{fj'q}^*$) are greater than the DC bus voltage v_{dc}, initially regulated at 1200 V but lower than 1500 V. Thus, once the fault detected and compensated, the reference of the DC bus voltage has been increased of 25% in GSC control.

Figure 20. Case *(b)* with fault detection and compensation of an open-circuit fault when $i_{f3'} > 0$: fault on $S_{3'}$ at t = 0.61s.

The zoomed results of Figure 20 on a duration of 300 µs are presented in Figure 21when the switch $S_{3'}$ fault occurs at t = 0.61s. When the fault appears on $S_{3'}$, the current $i_{f3'}$ is above the zero. Thus the fault cannot be detected because $D_{3'}$ is on-state and the switch $S_{3'}$, in off-state position, not disturb the conduction sequences: the current $i_{f3'}$ crosses $D_{3'}$ and $S_{6'}$. The leg 3' of GSC operates normally.

At t = 613.355 ms (see Figure 21(b)), $i_{f3'}$ crosses zero and $\delta_{2'} = \delta_{3'} = 1$ and $\delta_{1'} = 0$, therefore $D_{3'}$ and $D_{6'}$ become in off-state and $i_{f3'}$ remains zero, the pole voltage $v_{3'0m}$ is equal to $3/2e_{3'n}$ and the voltage error is equal to $(-v_{dc}/2+3/2e_{3'n})$. Thus the fault can be detected [3]. Therefore the fault detection is achieved 10 µs after (detected at t = 613.365 ms). The fault on GSC is detected 3.4 ms after the fault apparition because, before the fault occurrence, the GSC operates normally.

Figure 21. Case *(b)* with fault detection and compensation of an open-circuit fault when $i_{f3'} > 0$:
(a) zoomed results of 300 µs,
(b) zoomed results of 30 µs.

It is noted that with a fault time detection and compensation about few microseconds, fault impact does not appear on waveforms (any transients) because this time is very small compared to the switching period. Moreover, one can see that for the studied WECS with fault tolerant converters topology without redundancy, the system can still operate in nominal conditions under any power switch failure with these operation conditions and with or without increasing the DC bus voltage level.

In both cases *(a)* and *(b)*, after fault detection and compensation of the faulty switch $S_{3'}$ of the third leg of GSC, the converters topology becomes a five-leg structure with the leg 3 of RSC common to GSC. The different currents $i_{f3'}$, i_{r3}, i_D and i_{cl} for the case *(b)* are presented in Figure 22. It is noted that before the fault apparition, the current i_D in the faulty leg is equal to current $i_{f3'}$ and the current i_{cl} is equal to current i_{r3}. After the fault compensation and converters reconfiguration for an open-circuit fault on $S_{3'}$, the current in the common leg (leg 3) depends on the three others currents ($i_{f3'}$, i_{r3}, i_D), as shown in equation (1).

Figure 22. *GSC, DFIG rotor, faulty leg and common leg currents before and after the fault occurence*.

The same analyses can be achieved for an open-circuit fault on other switches of the GSC or RSC. For the short-circuit faults on switches of RSC or GSC, considerations have been made in section II.B.2. Thus, HIL simulation results for short-circuit faults are as the same as that in open-circuit faults.

V. CONCLUSION

This paper has examined a reconfigurable converter topology and control orders for WECS with DFIG, achieving switch failure fault tolerance capability. The fault tolerant topology has been achieved by adding only three bidirectional devices to the classical back-to-back power converter topology. Moreover, we have presented a fault detection and compensation method by eliminating false fault detection due to semiconductors switching. After fault detection, the reconfigured topology becomes a "five-leg" converter with a common leg for both GSC and RSC. Thus, we have also considered a dynamic "five-leg" control after fault detection. To change as quickly as possible the control strategy from normal to faulty conditions, FPGA technology has been used. The validation of the fully digital reconfigurable controller and

fault detection has been performed using a “HIL simulation”, called “FPGA in the loop” reconfigurable platform. A development board which includes a FPGA chip has been used to perform the experimental digital validations. This approach eliminates the risk of damaging the actual high power WECS, which may not be easily available for experimental validation. The fault detection scheme and the reconfigurable control have been validated by experimental results by using the “FPGA in the loop” prototyping. Results have shown the viability of the studied fault tolerant converters topology without redundancy.

This feature is particularly attractive for wind energy systems in which continuity of the power generation is mandatory.

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