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# ProDEVS : an Event-Driven Modeling and Simulation Tool for Hybrid Systems using State Machines

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## ABSTRACT

This paper introduces a new event-driven modeling and simulation tool for the simulation of hybrid systems. The particularity of this software called ProDEVS lies in its graphical language to define model components behaviour. This graphical language customizes state machines for DEVS and quantized based numerical methods. In this paper, syntax and operational semantic of the language are explained, and a mapping from DEVS to this language is illustrated across two simple examples in discrete-event and continuous domain. Finally a complete hybrid system is modeled and simulated to show the usability and the efficiency of this model.

## General Terms

Languages

## Keywords

State machines, DEVS, Hybrid systems, Event-driven simulation

## 1. INTRODUCTION

DEVS (Discrete Event System Specification) [14] is a general formalism for specifying modular and hierarchical model of dynamic systems. A DEVS specification is executed by an event-driven simulator which ensures the scheduling of timed events and increases the simulation clock to the time of next event. Algorithms and methods to implement an event-driven simulator for DEVS models are also given in [14].

There are numerical methods like the Quantized State System (QSS) family [3] that have shown to efficiently approximate ordinary differential equations. QSS is based on state space discretization, also called quantization, rather than time discretization given by conventional numerical integration methods. Within QSS, a quantization function

maps real-valued numbers onto a discrete set of real values also called quantization levels [3]. A continuous-time system is then approximated by computing the required time for a state variable to reach the next level. This technique has a straightforward representation in DEVS.

DEVS is even considered [1] as the most general formalism since other discrete event languages such as Petri Nets and State Charts but also discrete time systems can be seen as particular cases of DEVS. Moreover DEVS provides a unified framework for representing hybrid systems which combines discrete and continuous dynamics and the usage of QSS based integration methods are noticeably efficient to simulate hybrid systems due to their ability to handle discontinuities [1]. Taking into account these remarks, DEVS is a good candidate for modern modeling and simulation environment.

There is a huge variety of tools which support DEVS: DEVJSJAVA [13], aDEVJS [7], CD++ [12], PowerDEVJS [1], JAMESII [15], VLE [10], PyPDEVJS [11], DEVJS-Ruby [4]. A comparison of this software list is proposed in [5]. If most of them have a Graphical User Interface, none of these tools are able to support at the same time a graphical syntax for atomic component description and the mentioned numerical integration of ordinary differential equations. PowerDEVJS is hybrid system oriented but atomic components are defined in C code.

In this context, we design and implement ProDEVS, an integrated modeling and simulation environment oriented to hybrid systems based on discrete-event simulation theory and DEVS. We define a language which specializes State Machine for building, animating and simulating graphical DEVS specification. We implement an event-driven simulation engine according to the algorithms and the methods previously mentioned. This idea is motivated by the trend for using high-level specification language rather than code for dynamic system design.

The next section gives an overview of the tool and its features. Section 3 introduces the syntax and the semantic of a ProDEVS model. Section 4 shows the mapping between a DEVS atomic component and a ProDEVS State Machine for discrete-event system and continuous system. Section 5 describes an example to illustrate the use of this model in hybrid simulation. Section 6 gives conclusions and perspectives.

## 2. TOOL FEATURES

Our software is implemented in Java and it is based on

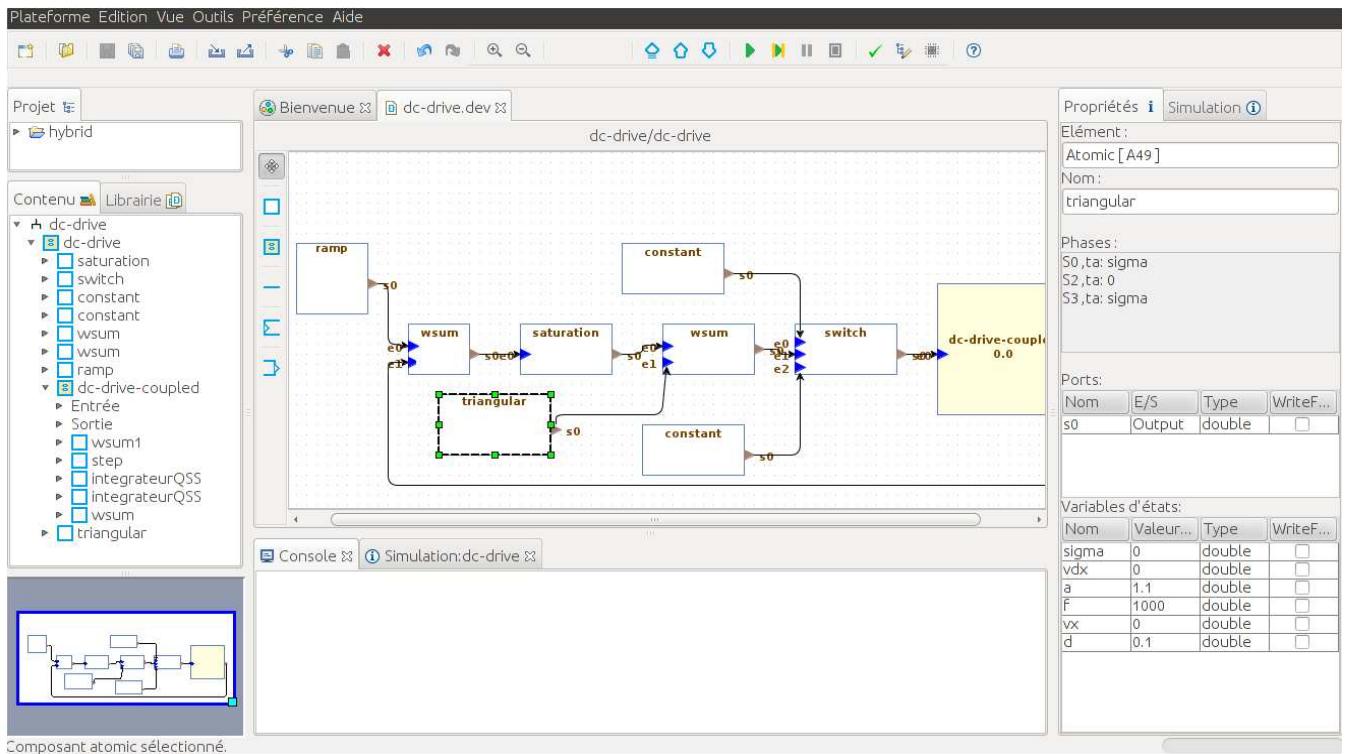


Figure 1: ProDEVS editor

the platform of services OSGI (Open Service Gateway initiative). Thus, each component of the application (editor, model, simulation engine, plot, code generator) is in the form of bundle that can be started or stopped dynamically. OSGI framework also facilitates the addition of new features.

Figure 1 shows a screenshot of the editor. It gives users an easy navigation within the hierarchical levels of the model and allows simulating the model at different level of the hierarchy. The diagram panel in the center allows editing models. There are two type of pallets if it is coupled component or atomic component. A pallet for the description of a block diagram with port and connector is given for the definition of a coupled component and a pallet for ProDEVS State Machine description is proposed when editing an atomic component. We use the JGraphX library for graphical design of the model.

The WEST region contains a project explorer, a model explorer and a library of components. Components can be drag and drop directly from the library to the diagram (import) or from the diagram panel to the library (export). The components of the library are stored in XML files.

The EAST region contains a properties tab for specifying information of models such as initial values of its variables and its parameters. The simulation tab is used to specify the simulation time and the execution algorithm. Two simulation algorithms are available: classic or parallel [14]. In classic simulation only one event at a time can occur. In parallel simulation, more than one event can be received by a component at the same time. In case of non-determinism, the receiver component randomly chooses an event to execute. A complete set of mechanisms (priorities, guards) allows to resolve conflicts in the execution and improves the

semantic of our language.

The simulation can be performed in step-by-step mode, where each variable value can be observed. At the end of the simulation, a new frame gives the plots for selected ports or variables. The bundle for the visualization of trajectories is based on the JFreeChart library.

For a sake of performance, the simulation engine executes compiled code. A specific bundle for loading the model is called when a new simulation is started. For each atomic component, this bundle generates a .java file that is compiled and executed. Compiled code improve significantly the performances compared to interpreted code that needs parsing boolean and arithmetic expressions. However, the user can access the source file to introduce more complex treatments like loops that can not be expressed graphically until now.

A model verifier is used to check static properties on the model. This properties are about the correct construction of the model (typing, valid expression, non-initialised variable,...). Verification result is given as warning and error in the console tab.

We finally design a ProDEVS model transformation to extended TPN (Timed Petri Nets) with data handling called (TTS) Time Transition Systems [2] to generate a finite representation for the accessible states of a ProDEVS model. We consider the Finite and Deterministic subset of DEVS [6], classic DEVS and parallel DEVS. This feature is no further explain here and will appear in another paper.

### 3. PRODEVMS MODEL

We create a customized component-based StateMachine

model that supports DEVS syntax and semantic. In substance, we reuse and specialize many concepts of UML 2.4 (Unified Modeling Language), including packages *BehaviorStateMachines*, *Communications* and *Kernel*. This section gives a description of this model.

### 3.1 Model structure

The abstract syntax for the structure of a ProDEVS model is given by the UML class diagram figure 2. A ProDEVS model compound (composition link) of exactly one component which is either atomic or coupled (inheritance links). A component that is coupled or atomic consists of input or output ports (portDirectionKind attribute). An atomic component is associated with a *DEVSStateMachine* describing its behavior. Coupled component is composed of one to several atomic or coupled components and zero to several connectors. A port must be typed (the class *Port* inherits from the class *TypedElement*). A port acting as a source is connected to zero or more ports acting as a target via connectors. A port that serves as a target is the destination of zero or more ports acting as source via connectors (associations between classes *Port* and *Connector*). A connector can only be associated with two and only two ports at a time. A connector either coupling an output port of a component to an input port of another component (IC) or coupling an output port of a component with an external output (EOC) or coupling an external input to an input port of a component (EIC).

*TypedElement* defines the type of value *DataType* that is a comprehensive list of literal values: boolean, double, integer and float. *PortDirectionKind* is a comprehensive list of literal values: in, out. *ConnectorKind* is a comprehensive list of literal values: IC, EOC, EIC.

We define constraints to check the correctness of the model. Examples of constraint are given through this section in natural language and in Object Constraint Language (OCL):

*If the connector is of type IC, source port must be of type out and the target port must be of type in. In addition, source port and target port must belong to different sub-components of the same current coupled component.*

```
Coupled.AllInstances -> forAll(connector.connectionKind
<> IC) implies (source.portDirectionKind <> out) and
(destination.portDirectionKind <> in) and
(self.includes(source.component) and
(self.includes(destination.component) and
(source.component != destination.component)
```

### 3.2 ProDEVS StateMachine

#### Syntax.

The abstract syntax for a ProDEVS StateMachine is given by the UML class diagram figure 3.

A *ProDEVSStateMachine* is a set of states-transitions that defines the behavior of an atomic component. A phase is a specific parameter that represents a period in the life of the atomic component where it is expected some events to occur (input event or time event). It has a set *outgoing* of transitions departing from this phase, a set *incoming* of transitions entering this phase and a *timeAdvance* attribute to specify the time in which the system as to stay before triggering the output and the internal transition function (a time advance value can also be given by a variable of the component).

*A phase with a time advance equal to infinity must not*

*have an outgoing transition of kind internal and must have at least one outgoing transition of kind external.*

```
self.timeAdvance.val <> infinity implies
forAll(t | self.outgoing->not(t.kind <> internal)) and
exists(t | self.outgoing->t.kind <> external)
```

*A phase with a time advance not equal to infinity must have at least one outgoing transition of kind internal*

```
not(self.timeAdvance.val <> infinity) implies
exists(t | self.outgoing->t.kind <> internal)
```

A transition is an oriented relationship between a source phase and a target phase. It is associated to :

- a trigger which specifies an input that may fire an external transition in case of external event or an output in case of time event (time elapsed in a phase is reached).
- a guard which provides a fine-grained control over the firing of the transition using boolean expression. The guard is evaluated when an event occurrence, external event or time event, is dispatched by the state machine. If the guard is true at that time, the transition may be enabled, otherwise, it is disabled. A guard constrains a set of properties<sup>1</sup> of the component.
- an action which specifies an optional assignment to be performed onto property when the transition fires.
- a source which designates the originating phase of the transition.
- a target which designates the target phase that is reached when the transition is taken.

#### Operational semantic.

The system is in phase  $\varphi$  at a given time and must be in that phase for a period  $e = \varphi.timeAdvance$ , if no external event occurs. When the time  $e$  has elapsed without any external event has occurred, the system triggers a time event and calculates and propagates the output. Then, for each outgoing internal transitions the guards are assessed. The system triggers one of those transitions which are enabled. If instead, an external event occurs on the input before the expiration of  $e$ , the system triggers the corresponding external transition, if it is enabled. In any case, the system reaches a new phase  $\varphi' = \varphi.outgoing.target$  for a period defined by  $\varphi'.timeAdvance$ , the actions associated to the triggered transition are computed and the same algorithm is applied.

When  $\varphi.timeAdvance = \infty$ , it means that it is a passive phase and only an external event will leave the phase. When  $\varphi.timeAdvance = 0$ , it means that this is a transient phase so the output computation and the internal transition triggering are immediately performed.

In ProDEVS, like in DEVS, communications are weak synchronous, i.e., non blocking with (possible) message loss. If both sender and receiver are ready to communicate, the

<sup>1</sup>The term *property* or *structural feature* is used in UML. In this model the class *Property* simply represents a variable of the component.

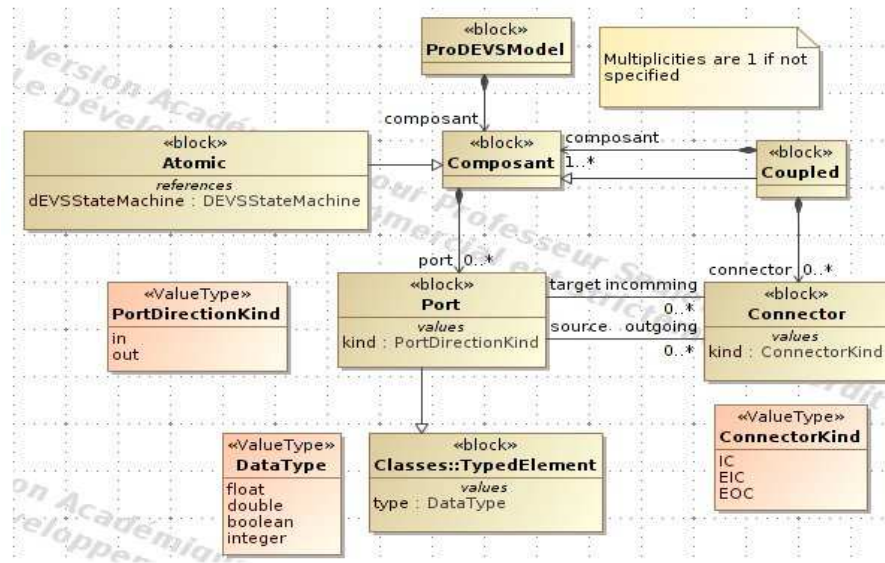


Figure 2: ProDEVS model structure

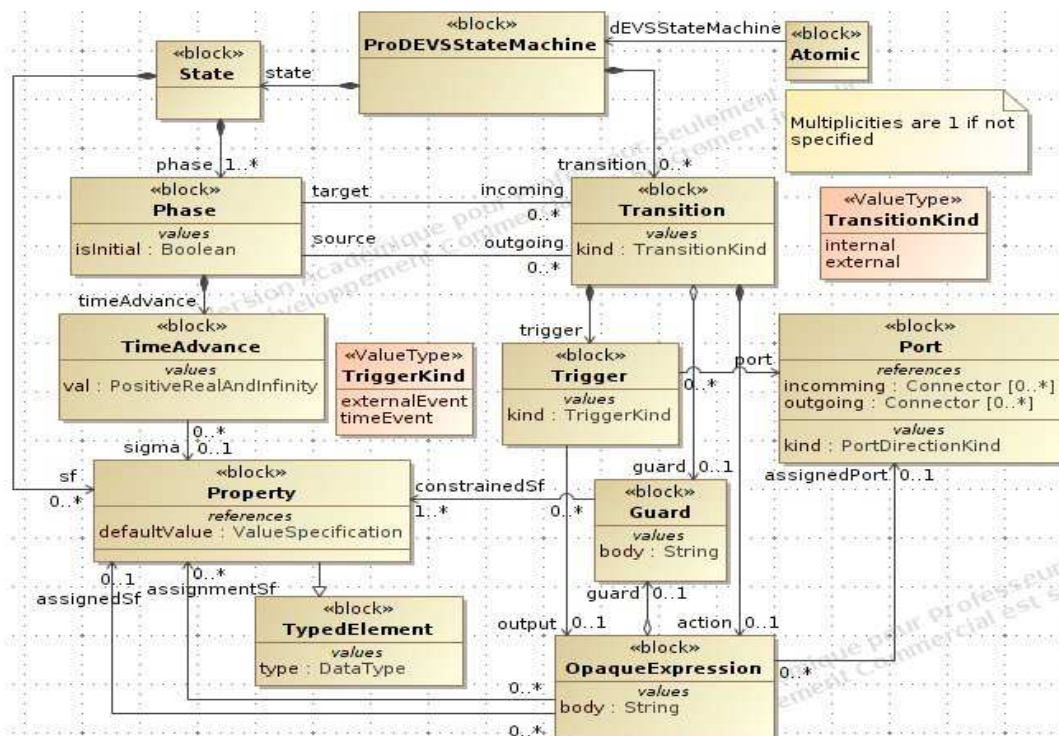


Figure 3: ProDEVS StateMachine

output event is converted into an input event which is instantly received. If the receiver is not ready, the message is lost.

As a result of coupling of concurrent components, there may be multiple components with simultaneous events. Thus, there may be multiple components which are candidates for the next internal state transition. Such components are called *imminents* in the DEVS terminology. In classic DEVS, a *Select* function is added at the coupled component that allows to select the component to execute among a set of imminent components. In parallel DEVS, every imminent components are executed. A component may receive a bag of inputs. A confluent transition function is added to refine a transition in case of simultaneous time event and external event.

A DEVS system is deterministic [9] as the current state of the system is completely determined by its previous state, the input (if any) and the time elapsed since the last transition or the time advance. In other words the output is completely determined by the timing of the input events [9]. A ProDEVS system is indeterministic if more than one transition is enabled at the same time. The user can resolve indeterministic behaviour by use of priorities among a set of transitions. If two enabled transitions have the same priority, the transition to trigger is selected randomly.

The label for internal/output function and external transition function are defined by the following BNF expression:

```
<transition> ::= [<guard>] <trigger> '/' [<action>]
```

The details of the syntax for the trigger event are defined by different kind of events:

```
<trigger> ::= <time-event> | <external-event>
```

- output events (at time event) are denoted by ! followed by the name of the triggered output port, followed by an assignment specification:

```
<time-event> ::= [<!<name> = <output-assignment>]
```

- external events are denoted by ? followed by the name of the triggering input port:

```
<external-event> ::= ?<name>
```

*There are no assignment on port when the trigger is of kind externalEvent.*

```
self.kind <> externalEvent implies self.output->isEmpty()
```

*There is an assignment on output port when the trigger is of kind timeEvent.*

```
self.kind <> timeEvent implies self.output->notEmpty() and
self.port = self.output.assignedPort
```

## 4. PRODEVS IN PRACTICE

This section describes how a ProDEVS State Machine can describe a DEVS atomic component for discrete-event system and continuous system.

### Discrete-event system.

In DEVS, external transition function, internal transition function, output function and time advance function are defined on  $S$  [14]:

- $\delta_{ext} : Q \times X \rightarrow S$  with  $Q = \{(s, e) | s \in S, 0 \leq e \leq ta(s)\}$
- $\delta_{int} : S \rightarrow S$
- $\lambda : S \rightarrow Y$
- $ta : S \rightarrow \mathbb{R}_{0, \infty}^+$

with  $S$  characterized by a set of state variables and their values, i.e.  $S = (sv, v) | sv \in SV, v \in D_{sv}$  such that  $SV$  is the set of state variables and  $D_{sv}$  is the domain of value for state variable  $sv$ .

For example, the state space  $S$  for a buffer BUF is defined by:

$$S_{BUF} = \{(proc\_status, \{free, busy\}), (queue, \{0; n\} | n \in \mathbb{N})\}$$

Or the state space  $S$  of a quantized integrator  $I$  is defined by:

$$S_I = \{ql \in \mathbb{R}, q \in \mathbb{R}, \dot{q} \in \mathbb{R}, \sigma \in \mathbb{R}\}$$

Often, but this is not mandatory, a DEVS atomic component has a special state variable called *phase* that can take a value from a set list of literal values.

An initial state is given as a list of assignment. For example, if the state variables *queue* and *proc\_status* have the initial values empty and free, then the initial state is given as *queue := 0, status := free*. The general form of the internal state transition function is given as *current\_state*  $\Rightarrow$  *next\_state* where *current\_state* is expressed as a boolean expression and *next\_state* as a list of assignment. For example an internal transition buffer BUF could be:

$$(queue > 0 \ \&\& \ proc\_status == free) \Rightarrow \\ (queue := queue - -, \ proc\_status := busy) \quad (1)$$

The general form of a time advance function is given as *current\_state*  $\Rightarrow \mathbb{R}_{0, \infty}^+$  where *current\_state* is expressed as a boolean expression. For example a time advance function for the buffer BUF could be:

$$(queue > 0 \ \&\& \ proc\_status == free) \Rightarrow 0 \quad (2)$$

In ProDEVS we assume that an atomic component always hold exactly one state variable called *phase* that can take many values as necessary from a comprehensive list of literal values. A value for this variable will be represented by a UML state. In the remainder of this paper, for simplicity, we will call a phase one value of state variable *phase*. Thus, in ProDEVS, time advance function and transition functions are associated to each value of phase, or simpler, to each phase, all which is actually restrictive according to DEVS specification.

However, within ProDEVS, the assignments are actions associated with the transitions and the boolean expressions are guards also associated with transitions. For example, a buffer that would be modeled without phase in DEVS will



be modeled in ProDEVS by the state machine in Figure 4<sup>2</sup>.

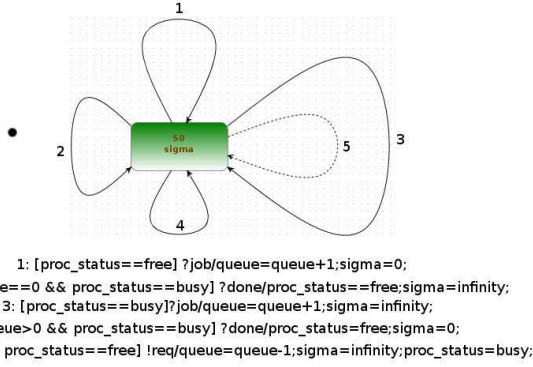


Figure 4: Atomic component BUF with one phase

This mechanism of actions and guards associated with transitions which are themselves a directed relationship between the phases can represent exactly a DEVS model. Indeed, the internal transition function given by equation (1) is encoded by the transition 5 Figure 4. Furthermore the time advance function given by equation (2) is encoded by the transition 4. The guard expresses the *current\_state*, here, ( $queue > 0 \ \&\& \ proc\_status == busy$ ). The action contains the assignments on the state variables from the *current\_state*, here, queue is unchanged and  $proc\_status := free$ . The assignment of the state variable  $sigma$  allows setting the time advance function for *next\_state*.

In fact there are a multitude of ways to model a buffer always with the same behavior. For example it is possible to allocate the state variable  $proc\_status$  in phases. Thus, BUF becomes as shown Figure 5:

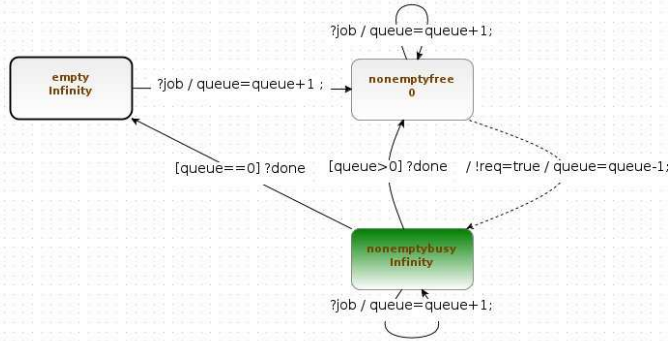


Figure 5: Atomic component BUF with three phases

The *finer grain* BUF model would allocate  $queue$  and  $proc\_status$  into phases. This gives a model without guards and assignments as shown Figure 6.

### Continuous system.

Basically, the QSS method consists in discretizing the space of state variables using a fixed value called the *quantum* size

<sup>2</sup>A dotted arrow represents an internal transition and a full arrow represents an external transition.

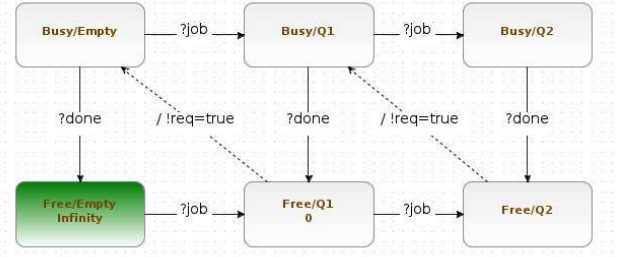


Figure 6: Atomic component BUF with six phases for a buffer with capacity of 2 (taken from [14] page 465).

$D$ . According to this quantum, a variable  $q$  can only take values among  $q \pm kD$  where  $k$  is an integer. The solution  $q(t)$  of a system described by a differential equation is approximated on a grid in the phase space of the system. The resolution of the phase space grid is  $D$ . The time  $h$  required to move from one phase space grid point to another on  $q(t)$  is approximated and a state change will be informed only at this time.

As shown in [8],  $h$  may be computed from classical ODE solvers, e.g. for Euler or Runge-Kutta. Consider an ordinary differential equation in the form of

$$\dot{q} = f(q(t)) \quad (3)$$

We consider the simple Euler integration method

$$q(t+h) = q(t) + h\dot{q}(t) \quad (4)$$

Let the quantum  $D$  be defined by

$$D = |q(t+h) - q(t)| \quad (5)$$

Then the time required for a change of size  $D$  to occur on  $q(t)$  is approximatively

$$h = \begin{cases} \frac{D}{|\dot{q}(t)|} & \text{if } \dot{q}(t) \neq 0 \\ \infty & \text{otherwise} \end{cases}$$

This approach can easily be extended to a set of coupled ordinary differential equations in the form of  $\dot{q} = f(q(t))$ , where  $q$  is a vector of differential variables. For each ordinary differential equation  $i$  of such a system, two variables are necessary. A variable  $q_i$  which is the position of state variable  $i$  on its phase space axis and a variable  $ql_i$  which contains the last grid point occupied by the variable  $q_i$ . These two variables are necessary because the function  $f_i$  is now computed at grid points in the discrete phase space of each element of the vector  $q$ . A variable  $q_j$  may have reached a grid point in its discrete phase space while the variable  $q_i$  has not reached its next grid point yet. Then the time required for the variable  $ql_i$  to be updated becomes

$$h = \begin{cases} \frac{D - |q_i - ql_i|}{|\dot{q}_i(t)|} & \text{if } \dot{q}(t) \neq 0 \\ \infty & \text{otherwise} \end{cases}$$

where  $|q_i - ql_i|$  is the distance already traveled along the phase space axis of state variable  $i$ .

A DEVS description of the quantized integrator is:





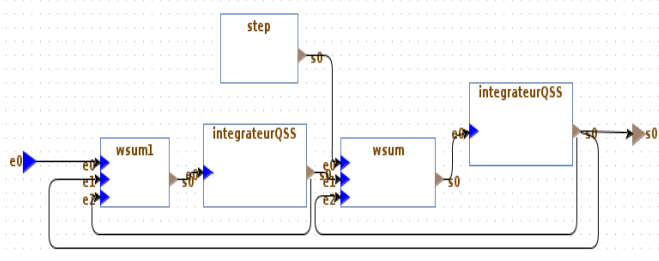


Figure 10: dc-drive model level 1 (dc-drive-coupled)

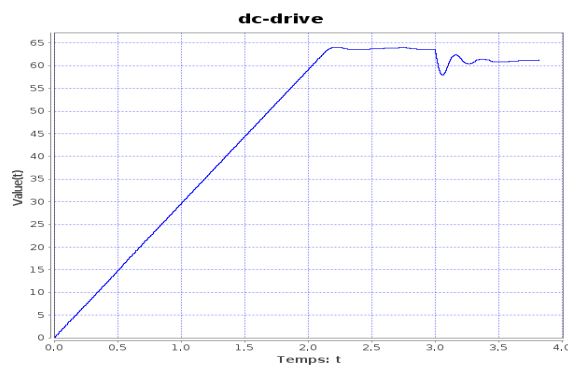


Figure 11: Output of the DC motor

values of each port and variable is stored as type String. The tool performs a type conversion in each step to make the calculations. This cast is expensive. Furthermore we believe we can optimize simulation engine processing such as searching ports connection through the hierarchy.

## 6. CONCLUSIONS

This paper has introduced a new event-driven modeling and simulation tool for the simulation of hybrid systems. The particularity of this software lies in its graphical language to define the behavior of the atomic components. This graphical language customizes state machines for DEVS and quantized based numerical methods. ProDEVS proposes an intuitive and user-friendly interface for designing DEVS model without experience in programming. It provides a block diagram interface for coupled components where users can go up and down the hierarchy with a just a double-click. A library promotes the reuse of models where parameters can be tuned without entering the atomic component. This library can be extended by users thanks to the export feature by a simple drag and drop from the diagram panel to the library panel. ProDEVS provides a model verifier to quickly detect inconsistencies and incompleteness.

We are now developing a formal verification feature of a ProDEVS model. Our approach is based on a transformation to extended TPN (Timed Petri Nets) with data handling called (TTS) Time Transition Systems to generate a finite representation for the accessible states of a ProDEVS model.

Finally we are considering a VHDL coder for hardware implementation of parallel architectures on FPGA to boost the performance and provide rapid prototyping features.

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