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
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Electrical control of interfacial trapping for magnetic tunnel transistor on silicon

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We demonstrate an electrical control of an interfacial trapping effect for hot electrons injected in silicon by studying a magnetic tunnel transistor on wafer bonded Si substrate. Below 25 K, hot electrons are trapped at the Cu/Si interface, resulting in collector current suppression through scattering in both parallel and antiparallel magnetic configurations. Consequently, the magneto-current ratio strongly decreases from 300% at 27 K to 30% at 22 K. The application of a relatively small electric field (~ 333 V/cm) across the Cu/Si interface is enough to strip the trapped electrons and restore the magneto-current ratio at low temperature. We also present a model taking into account the effects of both electric field and temperature that closely reproduces the experimental results and allows extraction of the trapping binding energy (~ 1.6 meV). © 2014 AIP Publishing LLC. [<http://dx.doi.org/10.1063/1.4863689>]

The trapping and detrapping of charges in oxides has been studied in the framework of the insulated gate field effect transistors (IGFETs) several decades ago;^{1–3} however, the trapping effects for hot electrons have been just recently evidenced in magnetic tunnel transistors (MTTs) on Si.⁴ The MTT devices which combine giant magnetoresistance (GMR) and magnetic tunnel junction (MTJ) elements with semiconductor materials have gained intensive interest.^{5–10} These devices can achieve a much higher magneto-current (MC) ratio than conventional GMR or MTJ devices due to the energy filtering effect of the metal/semiconductor Schottky contact in the MTT device. In addition, hot electron injection is a good way to overcome the impedance mismatch between the metal and semiconductor for the electron-injection into the semiconductor.^{11–15} MTT can also provide a highly spin-polarized electron current source for spin-injection into the semiconductor. Our previous work has evidenced a hot electron trapping phenomenon at Cu/Si interface by operating MTT device at temperatures lower than 25 K.⁴ It was found in previous work that as soon as the trapping of hot electrons occurs, the collected hot electron current in Si is dramatically reduced by a factor of between ten and twenty, and the MC ratio is decreased by half. Those effects have been shown to be linked to trapped electrons at Cu/Si interface that enhance an interfacial scattering of the new injected electrons and results in the reduction of the hot electron current that can overcome the Schottky barrier. In this paper, we demonstrate that we can control this interfacial trapping by applying an electrical field across the Cu/Si interface. With a small external electrical field, the trapped electrons can be stripped into Si conduction band and the MC ratio can be restored at low temperature. This work deepens our understanding of the hot electron interfacial

trapping mechanism, and could even lead to a future device design to trap spin-polarized electrons for quantum information application.¹⁶

To be able to apply an electric field across the interface, we first fabricated a wafer-bonded (WB) Si substrate consisting of the following structure: n-Si substrate//4 nm NiFe/4 nm Cu/3 μ m n-Si. This substrate was fabricated by performing an ultra-high vacuum (UHV) wafer bonding from an SOI wafer (with 3 μ m n-Si device layer) to an n-Si substrate by using the Cu/NiFe metal adhesion layer.¹⁵ The handle and insulator layers of the SOI wafer were then chemically removed by tetramethylammonium hydroxide (TMAH) and hydrofluoric acid (HF) solutions, respectively. The doping concentration (N_D) in 3 μ m n-Si and n-Si substrate is about 3×10^{14} cm⁻³ and the resistivity (ρ) is about 1–10 $\Omega \cdot$ cm. Then the WB substrate was introduced in a magnetron sputtering system to deposit a MTT structure containing a spin-valve (SV) structure for the base and an MgO tunneling junction as the emitter. The detailed structure is: WB-Si//Cu(10 nm)/NiFe(4 nm)/Cu(3.5 nm)/Co(4 nm)/MgO(2.7 nm)/Cu(20 nm). The sample was then processed with UV lithography procedure to define the junction and fabricate the electrode contacts on the top Cu (emitter), the SV metals (base), and Cu/NiFe (collector). Fig. 1(a) shows the top view of the WB MTT after lithography and Fig. 1(b) displays the schematic cross-section structure of the device. The Schottky properties of base (SV metal layers) and collector (Cu/NiFe layers) contacts with Si allow us to apply an electric field (accelerating voltage V_e) across the 3 μ m n-Si layer while the collection current I_c is almost kept unchanged. As shown in Fig. 1(c) for the band profile of the device, we apply an emitter bias (V_e) across the MgO barrier. When V_e is larger than the Schottky barrier height (SBH) of Cu/Si, the hot electrons can be injected into Si and most of them are collected at the bottom Cu/NiFe contact. It is worth mentioning that the device

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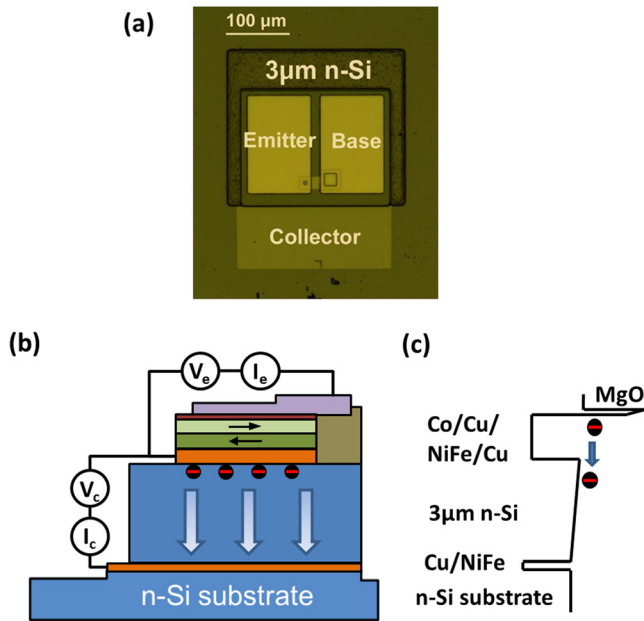


FIG. 1. (a) Top view of MTT device on WB Si substrate after lithography. (b) Schematic view of device cross-section structure during operation. (c) Profile of band structure of device during operation.

was made as a double transistor structure; however, the lower n-Si substrate is not electrically contributing, and the presence of the ferromagnetic NiFe layer in collector does not influence our spin transport results. The electric field generated from the accelerating voltage V_c is used to adjust the interface trapping, while we measure the collector current (I_c) with different magnetization configuration of the SV base. We have performed two types of experiments on this sample: measuring of I_c while varying temperature T or varying accelerating voltage V_c . In both cases, the negative bias for both V_e across the MgO barrier and V_c across the $3\ \mu\text{m}$ n-Si layer corresponds to a higher

Fermi level (E_F) of emitter compared to base, and a higher E_F of base to collector, respectively.

First, to demonstrate the capability of the electrical control of the interfacing trapping, we show in Fig. 2 the magneto-current measurement for the MTT with different V_c and T . The MC is defined as $\text{MC} = (I_{c,P} - I_{c,AP})/I_{c,AP}$, where $I_{c,P}$ and $I_{c,AP}$ are the collector currents for P and AP alignments, respectively. At 26.8 K without V_c [Fig. 2(b)], the MC ratio is obtained at 300%, showing the normal feature of MTT. However, as soon as the temperature is lowered to 22.5 K [Fig. 2(a)], the MC ratio drops rapidly to only 39%, and an evident curvature feature appears for the collection current in the parallel state. All of these behaviors signify the presence of interfacial trapping of hot electrons occurring at low temperature.⁴ If a small accelerating voltage of $-0.2\ \text{V}$ is applied across the $3\ \mu\text{m}$ -Si layer at 22.5 K [Fig. 2(c)], the curvature feature in P state disappears and we obtain again the MC ratio about 280%.

A more precise description of this phenomenon is provided by the detailed measurements in Fig. 3. Figs. 3(a) and 3(c) show the collector current vs. magnetic field curves at $V_c = 0\ \text{V}$ with different temperatures and at $T = 22.5\ \text{K}$ with different V_c , respectively. Figs. 3(b) and 3(d) illustrate the variation of MC ratio and collector current in P and AP states with different T and V_c , respectively. As we can see in Figs. 3(a) and 3(b), as temperature decreases from 45 K to 21 K, a dramatic decrease of collector current occurs in a narrow transition temperature window (T_{tran}) between 21 K and 25 K. At $V_e = -800\ \text{mV}$, the collector current decreases by a factor of 9 for the P state and 3 for the AP state. As a consequence, the MC ratio drops from 300% at 27 K to 30% at 22 K. The reduction of I_c is of the same order as what we have observed from MTT on n-type or undoped Si substrates at the same V_e .⁴ Then we varied V_c at 22.5 K below T_{tran} . As shown in Figs. 3(c) and 3(d), it is interesting to notice that both $I_{c,P}$ and $I_{c,AP}$ increase with the increase of V_c before

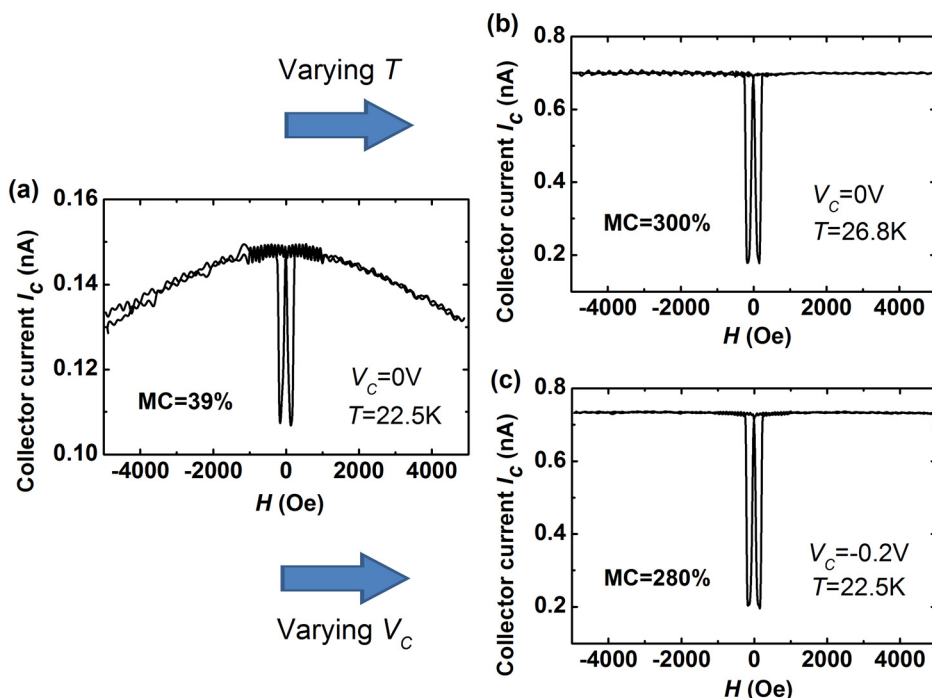


FIG. 2. I_c vs. H curves (a) at 22.5 K with $V_c = 0\ \text{V}$, (b) at 26.8 K with $V_c = 0\ \text{V}$ and (c) at 22.5 K with $V_c = -0.2\ \text{V}$. In all measurements, $V_e = -800\ \text{mV}$.

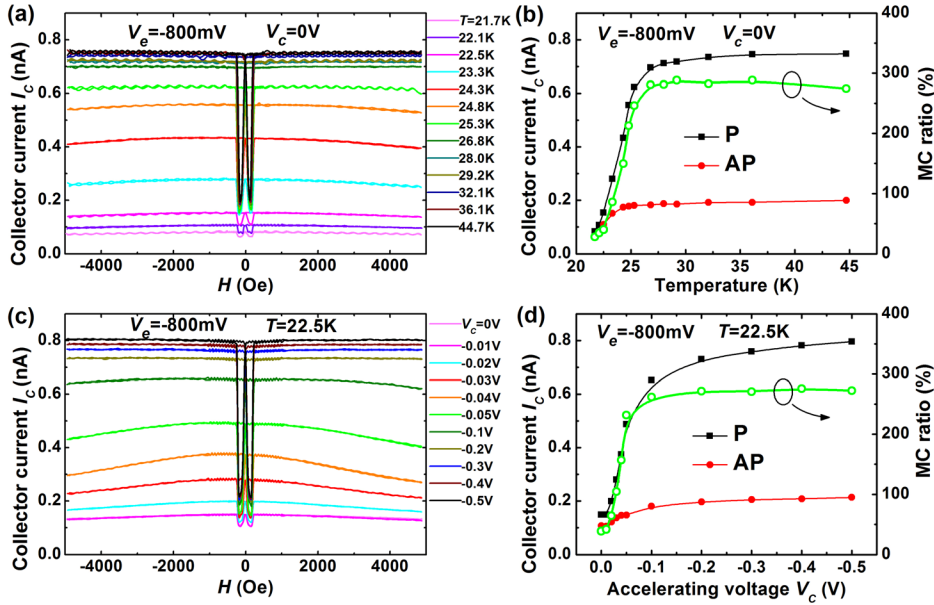


FIG. 3. I_C vs. H curves (a) at $V_c = 0$ V with different temperatures and (c) at 22.5 K with different V_c . Variation of $I_{C,P}$, $I_{C,AP}$, and MC ratio (b) with temperature at $V_c = 0$ V and (d) with V_c at 22.5 K. In all measurements, $V_e = -800$ mV. The P state is taken at $H = -190$ Oe, and AP state is taken at $H = 80$ Oe.

reaching the saturation after -0.1 V. Consequently, the MC ratio increases rapidly from 39% at $V_c = 0$ V to 275% at $V_c = -0.1$ V. The slightly lower MC than 300% is due to a minor increase of the leakage current with V_c in the AP state. It is evident that the small applied accelerating voltage restores the reduced I_C and re-establishes the MC ratio at low temperature. Another interesting feature is the disappearance of the curvature in I_C vs. H curves as soon as I_C returns to the normal value when a V_c is applied. This result is the same as if the temperature were increased. This also further proves that the curvature behavior is related to the interface trapping, which is attributed to the increase of the binding energy of electrons on the trapping centers.⁴

To confirm that the influence of V_c on I_C only takes place at low temperature, we have plotted in Fig. 4 the variation of $I_{C,P}$ with accelerating voltage at different temperatures. The evolution of I_C with V_c strongly depends on the range of voltage. When V_c is lower than a defined critical voltage V_{CR} , I_C increases quickly with the increase of V_c due to the detrapping of electrons. When V_c is higher than V_{CR} , I_C increases slowly because of the small leakage current of Schottky barrier. The critical voltage V_{CR} which characterizes the

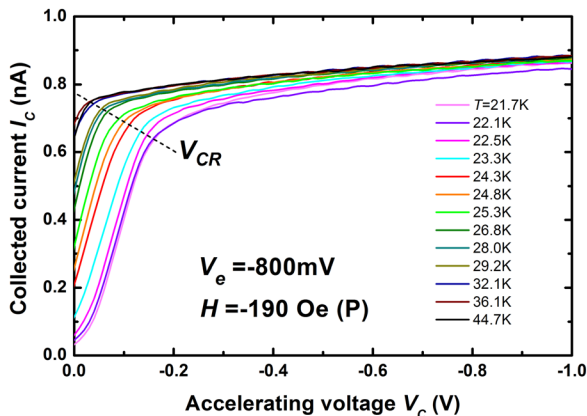


FIG. 4. Variation of $I_{C,P}$ as a function of accelerating voltage V_c at different temperatures. In all measurements, $V_e = -800$ mV. The P state is taken at $H = -190$ Oe.

ionizing field necessary to remove most of the trapped electrons decreases with the increase of T as indicated with the dashed line in Fig. 4. At high temperature, as the traps are no longer active, the rapid increase of I_C is almost suppressed.

The emitter bias (V_e) dependence of $I_{C,P}$ with different V_c is plotted in Fig. 5(a) for $T = 22.5$ K. When $|V_e|$ is larger than 0.64 V, the collector current increases rapidly. This threshold bias corresponds to the Schottky barrier height of Cu on Si (about 0.6 eV).^{17,18} The reduction of $I_{C,P}$ appears in all bias regions above this threshold. With the increase of V_c , I_C recovers the values measured at high temperature without trapping. The emitter bias dependence of the MC ratio with different V_c is shown in Fig. 5(b). Normally, the MC ratio reaches a maximum at the onset of hot electron collection and decreases gradually with the increase of emitter bias due to the insufficient reflection of the hot electrons at the Schottky barrier after inelastic scattering in AP state.⁹ Due to the interfacial trapping, the maximum of the MC ratio becomes narrow with $V_c = 0$ V. When increasing V_c , the MC ratio returns to the normal bias dependent behaviors. Here, we can also observe an increase of the MC ratio at high bias with the intermediate V_c about -0.02 to -0.03 V, which is attributed to the different amplitude of reduction of collector current for P and AP states with different V_c .

Based on our previously proposed model considering the interface electron trapping and releasing,^{4,19} we have extended in this work a model including the electric field to fit the experimental I_C vs. V_e curves with different V_c . The effect of electric field can be considered as a field-assisted tunneling process as schematically shown in the inset of Fig. 5(c). The tunneling barrier width of a trapped electron into Si conduction band can be expressed as $\frac{E_b}{qe}$, where E_b is the binding energy of the trapped electron and e is the electric field. At low temperature less than 25 K, due to the completely frozen out of carriers, the depletion zone in n-Si ceases to exist. The linear band profile makes the electric field directly proportional to the applied accelerating voltage [Fig. 1(c)]. The whole detrapping process including temperature and electric field can be written as

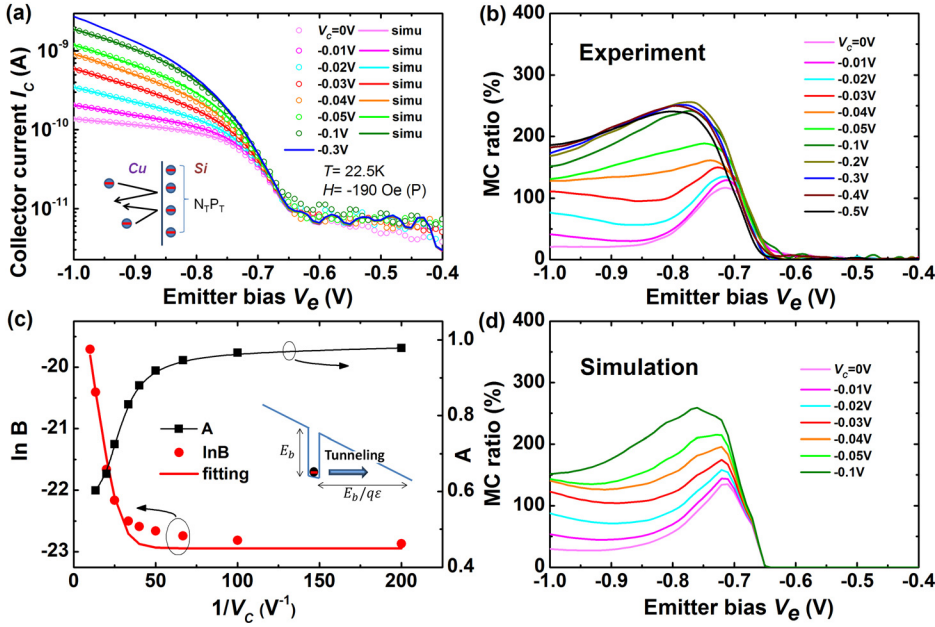


FIG. 5. (a) Emitter bias (V_c) dependent collector current in P state at different V_c for $T = 22.5$ K. Experimental results are shown in open circles and the simulation results are shown in solid lines. All simulations take I_0 from the data at $V_c = -0.3$ V (solid line). Inset: Schematic illustration of the backscattering of injected hot electrons by the trapped electrons at Cu/Si interface. (c) The extracted fitting parameters A and B for bias dependent $I_{c,P}$ as a function of $1/V_c$. The variation of $\ln B$ is fitted to extract the trapping binding energy. Inset: Schematic illustration of field-assistant tunnelling for the trapped hot electron. (b) Experimental and (d) simulation results for the emitter bias dependent MC ratio with different V_c .

$$\frac{dn}{dt} = k_c(N_T - n) - k_{th}n - k_Vn, \quad (1)$$

where N_T is the density of interface traps and n is the density of trapped electrons. The capture rate constant k_c can be expressed by $k_c = \alpha n_e$, where α is electron capture probability and n_e is the density of injected electrons. The thermal depopulation rate constant k_{th} can be written as $k_{th} = \frac{1}{\tau} e^{-\frac{E_b}{k_B T}}$. The electric field depopulation rate constant k_V can be written as $k_V = \frac{1}{D} e^{-\frac{\kappa E_b}{q\phi}}$, where κ^{-1} is the characteristic localization length for trapped electron tunneling into the Si conduction band. When $t \rightarrow \infty$, the trapping occupation probability P_T can be obtained as

$$P_T = \frac{n}{N_T} = \frac{k_c}{k_c + k_{th} + k_V}. \quad (2)$$

Due to the occupation of traps, the trapped electrons will exert an electronic repulsive force on the injected hot electrons and enhance the interfacial scattering effect, as schematically shown in the inset of Fig. 5(a). Therefore the collector current suppression can be expressed by the equation as below

$$I_C = I_0(1 - \eta N_T P_T), \quad (3)$$

where the injected current I_0 is suppressed proportionally to the density of occupied traps $N_T P_T$ with a coefficient η . Now let us insert Eq. (2) into Eq. (3) and then we can get as below

$$\begin{aligned} I_C &= I_0 \left(1 - \eta N_T \frac{k_c}{k_c + k_{th} + k_V} \right) \\ &= I_0 \left(1 - \eta N_T \frac{\alpha \cdot 1e^{10} \cdot I_0}{\alpha \cdot 1e^{10} \cdot I_0 + \frac{1}{\tau} e^{-\frac{E_b}{k_B T}} + \frac{1}{D} e^{-\frac{\kappa E_b}{q\phi}}} \right) \\ &= I_0 \left(1 - \frac{A I_0}{I_0 + B} \right), \end{aligned} \quad (4)$$

where $A = \eta N_T$ and $B = \frac{1e^{-10}}{C\alpha} e^{-\frac{E_b}{k_B T}} + \frac{1e^{-10}}{D\alpha} e^{-\frac{\kappa E_b}{q\phi}}$. We can take the experimental I_c without trapping as I_0 to make

simulations to fit experimental emitter bias dependent I_c with trapping to obtain the parameters A and B . As shown in Fig. 5(a), we have made the fitting for $I_{c,P}$ with different V_c from 0V to -0.1V using the data of $V_c = -0.3$ V as I_0 . Since the leakage current induced by V_c only gives a small constant background in the I_c vs. V_e curves, we have subtracted this background to be sure to correctly extract the fitting parameters.

As shown in Fig. 5(a), the good fit of the I_c vs. V_e curves is obtained by using only two parameters A and B and validates our interface trapping model. In Fig. 5(c), the fitted parameters A and B are plotted as a function of $1/V_c$. First, we found that the parameter A decreases quickly at high V_c . This means that the interfacial scattering efficiency η decreases with the electric field assuming that the density of traps N_T is constant. Second, we can extract precisely the binding energy E_b from the fitted parameter B . In our case, the non-linear variation of $\ln B$ vs. $1/V_c$ is due to a constant thermal detrapping term $\frac{1e^{-10}}{C\alpha} e^{-\frac{E_b}{k_B T}}$, which can be directly obtained from the fit of curve at $V_c = 0$ V to be 1.08×10^{-10} A. Then a least mean square fit of the variation of $\ln B$ vs. $1/V_c$ gives $B = 1.08 \times 10^{-10} + 2.38 \times 10^{-8} \exp(-0.22/V_c)$. As a recent study of metal-Si-metal heterojunctions has determined the tunneling characteristic length κ^{-1} in Si is about 21.7 nm,²⁰ we can then deduce the binding energy $E_b = 0.22 \frac{\kappa^{-1}}{d} = 1.59$ meV. This value is in good agreement with our previously estimated value of 1.7 meV from the transition temperature ($k_B T_{tran}$).⁴ Furthermore, we can fit the emitter bias dependent I_c in AP state with the same parameters A and B as in the P state (not shown), which means the interfacial scattering coefficient η is spin-independent. The bias dependent MC ratio can then be deduced from the simulated $I_{c,P}$ and $I_{c,AP}$ curves, as shown in Fig. 5(d). Our model well reproduces the MC ratio variation with different V_c , especially the increasing of MC ratio at high emitter bias with intermediate V_c .

The origin of the interface trapping is still under investigation. Recently, we have studied one MTT sample grown on the n-Si substrate which has been pre-annealed (600 °C

for 1 h) in ultra-high vacuum (1×10^{-9} Torr). This sample shows completely no interfacial trapping behaviors at low temperature. This is a strong argument to prove that the suppression of hot electron collector current is not a bulk Si behavior but strongly related to the Cu/Si interface. As already known, the Si surface after etching with HF solution is hydrogen passivated.²¹ The hydrogen atoms persist on the Si surface unless a high temperature annealing is performed.²² Our results indicate that the traps are located at very shallow energy of ~ 1.6 meV below the Si conduction band minimum (CBM) at the Cu/Si interface. Therefore, it is very probable that the interfacial traps are related to the residual hydrogen atoms at Cu/Si interface. Although the definitive identification of interface traps still requires more chemical structure analysis and dynamic measurement to determine the density of traps, our conclusions in this paper and the demonstration of the capability to electrical control of interface traps would not be changed.

When the interface traps are activated at low temperature, the Coulomb repulsing force due to the Rutherford scattering process will certainly change the lateral momentum $k_{//}$ of incident hot electrons. Since electrons should obey $k_{//}$ conservation rules when they cross the metal-semiconductor interface,^{23–25} it is difficult for the scattered hot electrons to find accepting states in X and L valleys with a finite $k_{//}$ distribution in the projected Si 2-dimensional Brillouin zone.²⁶ Therefore, most of the scattered hot electrons are reflected at the interface which results in a reduction of collector current. In our interface trapping model, the coefficient η is used to describe the proportional suppression of collector current with the number of occupied traps ($N_T P_T$). This coefficient is attributed to a combination effect of the Rutherford scattering cross section and semiconductor k-space collimator aperture.²⁷ In our case, we have found a similar η for fitting the bias dependent I_c curves in P and AP configurations, indicating a spin-independent scattering of the interface traps. To further examine the depolarization of spin state of injected hot electrons after interface scattering, we need to collect the hot electrons injected into the second n-Si substrate and employ the Cu/NiFe collector to analyze the spin state.^{19,28}

In summary, we have demonstrated an electrical control of interfacial trapping of hot electrons for MTT on wafer-bonded Si substrate. The interfacial electron trapping can be controlled by applying a small electric field across the Cu/Si

interface and the MC ratio can be restored at low temperature.

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