Extending the Frequency Range of the Direct Power Injection Test: Uncertainty Considerations and Modeling Approach

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***Abstract*—This paper evaluates and discusses the current frequency limitation (up to 1 GHz) of the Direct Power Injection test. An extension of its frequency range, based on uncertainty considerations and proper modeling, is then suggested.**

***Index Terms*—DPI, Immunity, Integrated Circuits, EMC Modeling, ICIM**

I. Introduction

THE frequency range considered for electromagnetic immunity aspects in all domains tends to increase steadily. In fact, the evolution of electromagnetic environment, with more and more radio communication systems above 1 GHz, leads to take into account these higher frequencies sources in EMC-compliant electronic design. Nowadays, most automotive systems must comply with immunity requirements defined up to 3 or 4 GHz such as [1], [2]. In this frequency range, the most efficient coupling mechanism is the field-to-harness or field-to-PCB phenomenon. This is related to the ratio of the disturbance wavelength over the coupling object size. This means that disturbances at the integrated circuit level are mainly propagated in conducted mode and, in most cases, direct coupling on an integrated circuit (package or die), is negligible. Therefore, the Direct Power Injection (DPI) test method is the best suited technique to characterize an IC. This standard [3] is only defined up to 1 GHz, and several characteristics of the set-up are responsible for this limitation. This paper intends to develop a technique which allows the extension of this method up to 3 GHz. The aim of the DPI characterization is either to validate a device or to provide data for immunity modeling. In both cases, previous works demonstrated that the immunity of an integrated circuit is realted to the transmitted power criterion [4]. The frequency extension must then be performed with the constraint of providing a well known, accurate and reproducible transmitted power to the IC. The objectives of this paper are thus to identify the main critical characteristics which must be dealt with in order to extend the DPI frequency range, and to highlight the limitations of a full experimental approach. These limitations will be identified and evaluated in Sect. 2. Then, a mixed experimental-modeling approach will be detailed in Sect. 3. Finally, in Sect. 4, a comparison between both techniques will be drawn.

II. Limitations of a full experimental approach

This section intends to discuss the experimental approach used to extract the transmitted power to the device when applying the standard DPI set-up. This set-up is presented in Fig. 1.

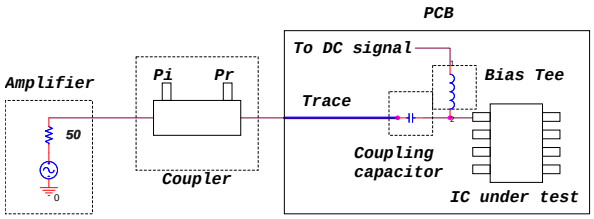

Figure 1. DPI test set-up

With an experimental approach, the transmitted power can be measured using a bidirectional coupler. Incident and reflected powers can then be measured in order to estimate the transmitted power, as follows:

$$P_t = P_i - P_r \tag{1}$$

Two major limitations have been identified with this technique and will be exposed in this paper. The first one concerns the lack of accuracy of the transmitted power, due to the fact that this value is issued from injected and reflected powers generally very close of each other. This is caused by the impedance mismatch onto which the injection is generally performed, leading to a high reflection coefficient. The second point concerns the fact that the transmitted power estimated by this technique corresponds to the power transmitted to the whole PCB and not only to the IC itself. A part of this power is dissipated not only in the injection path (losses in PCB injection traces and in the coupling capacitor), but also in the load structure including the bias tee.

In order to evaluate the errors induced by these parameters, a simulation-based approach, using a Spice model developed within the framework of [4] whose main characteristics will be described hereafter. Several impedance configurations are considered at the IC location: 1 Ω, 1 kΩ and real-world impedances of integrated circuits. The 1 Ω and 1 kΩ configurations will be analyzed in a frequency range between 1 MHz and 10 GHz. The real-world load impedances correspond to the 12V pin of a LIN transceiver and the 1A pin of a 74HC08. For these components, the models are only valid up to 3 GHz. The equivalent model that will be used is provided in Fig. 2.

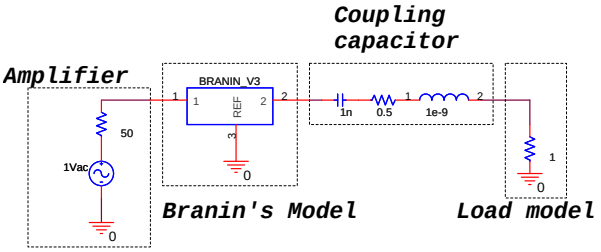

Figure 2. DPI equivalent schematic

- The amplifier is modeled by a voltage source with a 50 Ω impedance. The coupler and cable characteristics are not considered in the model, since it can be assumed that their influence can be eliminated during the experiment through a correct preliminary calibration. Furthermore, the power being measured at the coupler level, generally located close to the PCB, the effect of these parameters is transparent. The source is arbitrarily fixed at 1 V (corresponding to a 7 dBm incident power).
- The PCB trace is modeled using a transmission line. It corresponds to the one designed on the PCB used in [4] (22 mm trace length and 50 ohm impedance). In order to enhance accuracy, a Branin model [5] is implemented, taking into account all the frequency dependent characteristics that could influence the transmission behavior (skin effect, dielectric variations, inductance variations...). This model is built from measurements performed on a trace of this PCB, making it possible to extract the $\alpha(f)$, $\beta(f)$ and Z_c(f) characteristics of the transmission line.
- The coupling capacitor is modeled from a 1 nF X7R ceramic capacitor with its parasitic elements. Typical parasitic values are considered in this investigation.
- Finally, the load model is issued from S-parameter measurements in the case of real-world loads.

A. *Uncertainty on the power transmitted to the PCB*

Incident and reflected powers are usually measured with a power meter on each port of the coupler. For this analysis, it can be assumed that the uncertainties of the coupler characteristics are negligible and that the power to be measured has a correct S/N ratio (for a typical wattmeter, the minimum measurable level is about -60 dBm). The measurement error is then only related to the accuracy and uncertainty of the power meter probe. From Eq. 1, giving the transmitted power, the uncertainty equation for this value can be established:

$$P_t \pm \Delta P_t = P_i \pm \Delta P_i - P_r \pm \Delta P_r \tag{2}$$

The incident power, P_i, is a constant value in this analysis, and is linked to the e=1 V source in Fig. 2 by:

$$P_i = \frac{e^2}{4.R} \tag{3}$$

By simulation, the power transmitted to the complete PCB can be extracted from the complex voltage and current on this point:

$$P_t = \frac{1}{2}.\left(U.\overline{I} + \overline{U}.I\right) \tag{4}$$

The reflected power corresponding to the one measured at the coupler level is finally obtained from Eq. 1.

For various impedance configurations at the IC location (identified as loads in Fig. 2), the uncertainties on the transmitted power can then be estimated. The typical uncertainties of power meters are about ± 2.6 % in this frequency range [6]. In the case of the 1 ohm load impedance, the incident and reflected powers corresponding to those measured and concerned by the uncertainty aspect can be evaluated (Fig. 3). By applying the uncertainty calculation on the transmitted power, the tolerances on the computed value can be identified (Fig. 4).

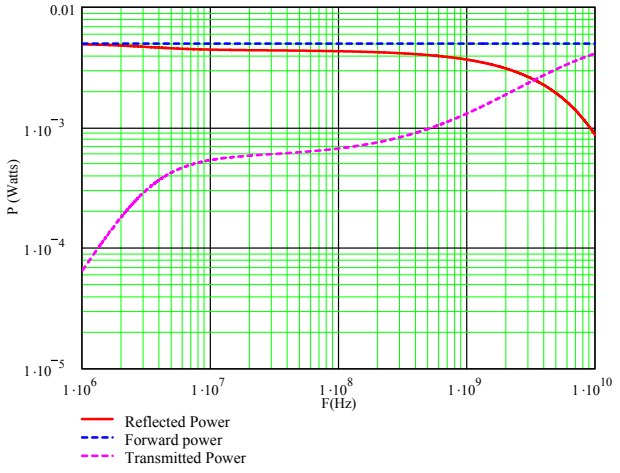

Figure 3. Powers at the PCB input - 1 ohm configuration

It can be noted that below 3 MHz, in the previous configuration, the uncertainties are in the same range as the transmitted power to be measured. This barely means that this power can not be evaluated correctly and highlights an important limitation of this approach. The same work is performed for all the load configurations previously defined, and the synthesis of the uncertainty (in dB) is given in Fig. 5.

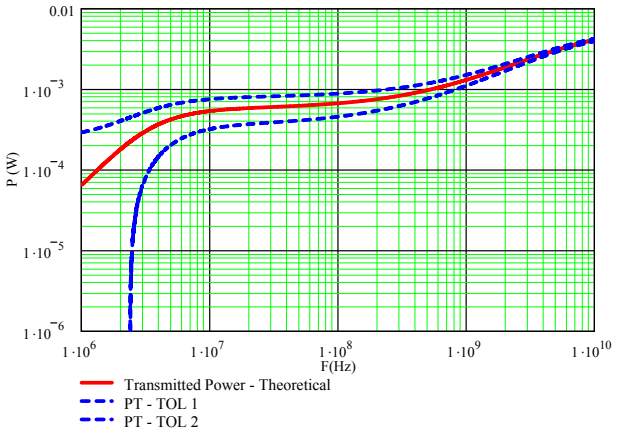

Figure 4. Transmitted power with tolerances at the PCB input location - 1 ohm configuration

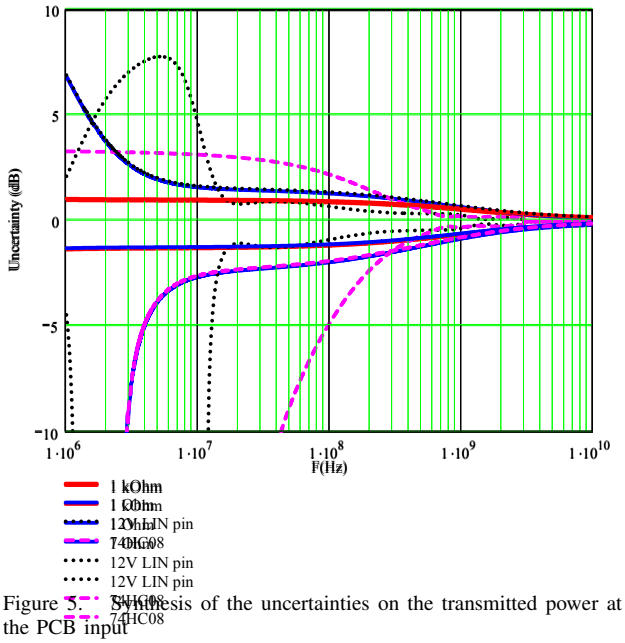

Figure 5. Synthesis of the uncertainties on the transmitted power at the PCB input

B. Comparison between powers transmitted to the PCB and the IC

The other parameter that must be analyzed is the difference between powers transmitted to the PCB and to the IC. The power transmitted to the IC is the only valid criterion to evaluate the influence of intermediate elements in the DPI injection path. With the configuration described in Fig. 2, the difference between these powers can be plotted for various configurations (Fig. 6).

Several comments can be done on these results:

- The difference between these transmitted powers tends to increase with frequency.
- Up to 3 GHz, and for practical cases, the difference is lower than 3 dB. This must be added to the uncertainty on transmitted power at higher frequencies.
- This evaluation does not take into account other effects such as the influence of trace length, capacitance characteristics (ESR) and bias tee impedance, which could also amplify discrepancies.
- With several resistive loads, important differences between transmitted powers can be observed, reaching 10 dB at 3 GHz and increasing further with frequency. Since real-world components can not provide an exhaustive overview of this issue, these results still have to be considered.

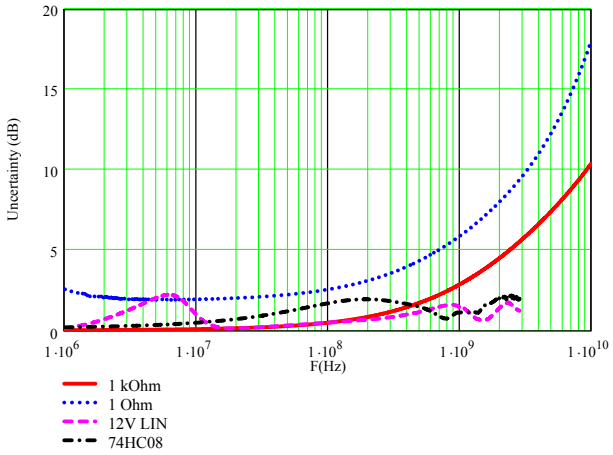

Figure 6. Power transmitted to the PCB and the IC - Synthesis

C. Influence of the bias tee

In a practical consideration, the DPI standard suggests the use of a bias tee impedance higher than 400 Ω in the frequency range of interest. However, this recommendation is inadequate and, using the same approach as before, the general trend of the error caused by this condition can be estimated. By simulation, the power transmitted to the device under test with or without the bias tee is compared. The difference in dB is then given for each load configuration and for a pure 400 Ω resistive bias tee (Figure 7).

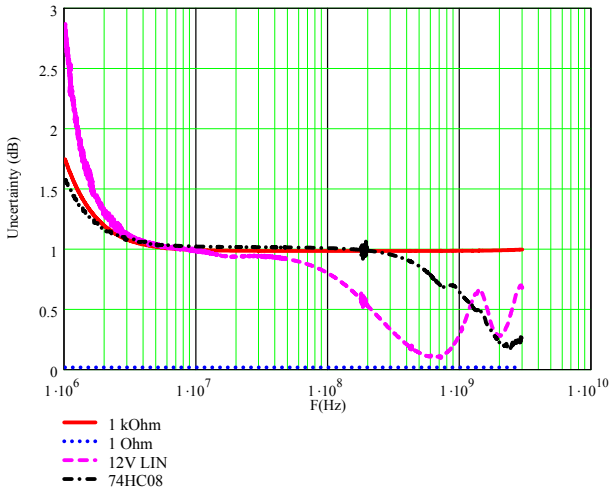

Figure 7. Difference in transmitted power due to the bias tee (R=400 Ω)

The same analysis is performed on a bias tee structure based on the use of inductors (Figure 9). This second bias tee was designed for the application in [4] and consists of the series association of 2 ferrite beads with a 47 µH inductance. Considering PCB parasitics and layout characteristics, this makes it possible to obtain the equivalent impedance given in Fig. 8.

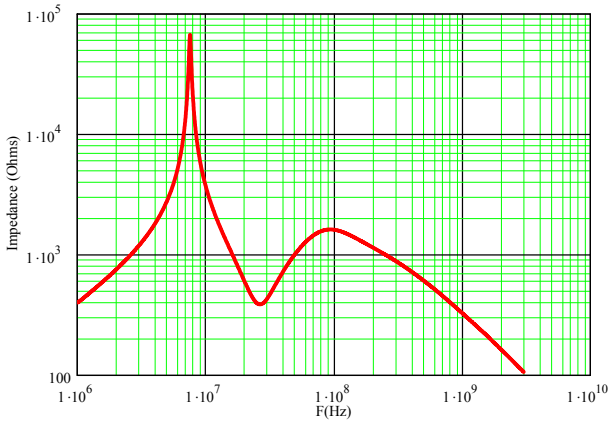

Figure 8. Impedance of the bias tee structure (inductance based)

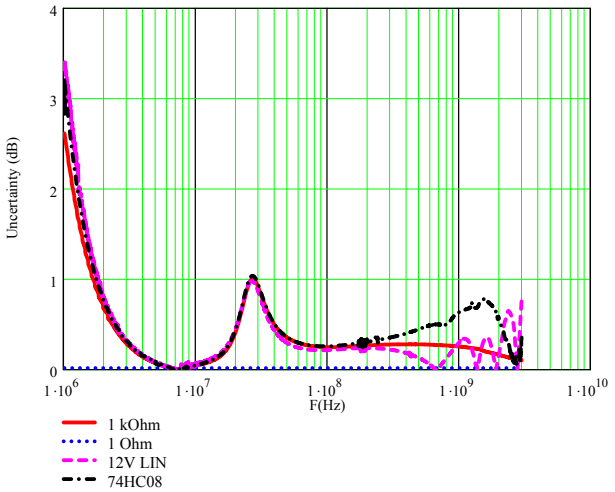

Figure 9. Difference in transmitted power due to the bias tee (inductance based structure)

- A 3 dB approximative deviation can be observed in low frequency, where the input impedance of the device is generally high (significantly more than 400 Ω). In this range, the 400 Ω objective looks inadequate. In practice, the bias tee impedance should be linked to the load impedance (5 or 10 times the impedance of the device under test). However, a bias tee structure based only on inductors and capable of such performance in a wide frequency range is difficult to design.
- At higher frequencies, the 400 Ω objective seems to be reasonable and consistent with the typical impedance observed in practice for integrated circuits. Even for real-world bias tee characteristics providing only 100 Ω at 3 GHz, the error generally observed is about 1 dB.

III. Mixed experiment- and simulation-based approach

In order to manage and extract the power transmitted to the device, a mixed approach, which does not require major changes to the DPI standard method, is suggested. This method is based on the traditional DPI test, in which only the incident power at the input of the PCB is extracted during the measurement phase. Through a complete modeling of the PCB and the DPI test set-up, the power transmitted to the device can be obtained by simulation.

The objective of this part is to estimate the uncertainty and accuracy on the evaluation of the power transmitted to the device obtained by this technique, and compare it with the errors coming from a full experimental approach.

The power transmitted to the device is given by the following relation:

$$P_t = \left(1 - |S_{11}|^2\right).P_i \tag{5}$$

In this equation, the incident power and the S_{11} parameter correspond to the actual load characteristics. It must be noted that this power does not correspond to the incident power at the PCB input which can be measured, but to the incident power at the DUT location. Nevertheless, since the transfer function is linear, it can be assumed that the same uncertainty needs to be considered for both locations. This leads to the following expression of the uncertainty calculation:

$$\Delta P_t = P_t.\left(\frac{-2.\Delta\,|S_{11}|}{1 - |S_{11}|^2} + \frac{\Delta P_i}{P_i}\right) \tag{6}$$

in which the contributions of each error source can be easily identified. The uncertainty on S_{11} is linked to the accuracy of the network analyzer. Taking into account typical performances, and in particular those specified in [7], the accuracy on the transmitted power can be estimated. With this approach, it can be assumed that, since each part of the PCB and of the IC is modeled, the only uncertainty sources on the transmitted power are related to the model of the device under test and to the incident power at the PCB input. The uncertainty on S_{11} depends on the value of S_{11} itself according to the characteristic specified in [7]. These characteristics lead to a limitation in this approach, which can be expressed either in terms of S_{11} range or impedance range. Since the uncertainty on S_{11} is about ± 0.02 for extreme values, this means that values between 0.98 and 1 are barely undefined.

The S_{11} range to be considered for ICs is then specified between -0.98 and 0.98. This corresponds to an impedance between 0.5 Ω and 5 kΩ. This correlates the observations and comments in [8], [9]. In practice, the impedances of common ICs are generally within this range (except in low frequency).

This evaluation requires the S_{11} coefficient corresponding to the load under test and the incident power at the load input. The first parameter is the one measured in order to generate the model, according to [4]. In order to estimate the incident power at the IC input, which is only needed for this uncertainty evaluation, the following method can be used:

The power transmitted to the load (Pt) can be extracted by simulation. Moreover, the load impedance can be determined (ideal test case or extracted from VNA measurements). The incident power information is then obtained by inverting Eq. 5. From these data, the

uncertainty on the transmitted power value due to the S_{11} uncertainty can be estimated (Fig. 10).

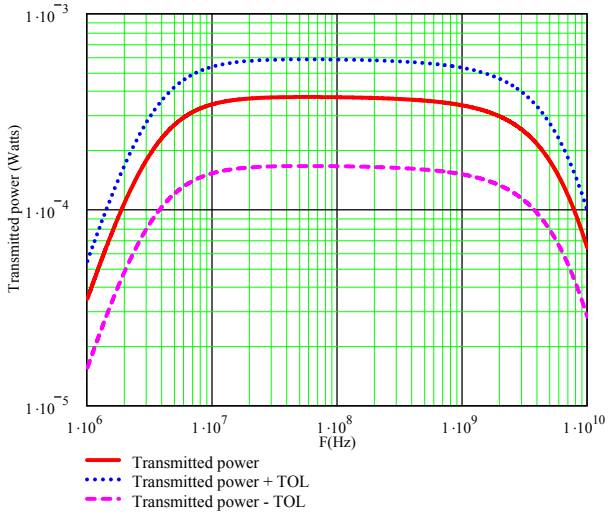

Figure 10. Uncertainties on the power transmitted to the IC due to S_{11} uncertainties

Using the same technique for all load conditions provides the results displayed in Fig. 11.

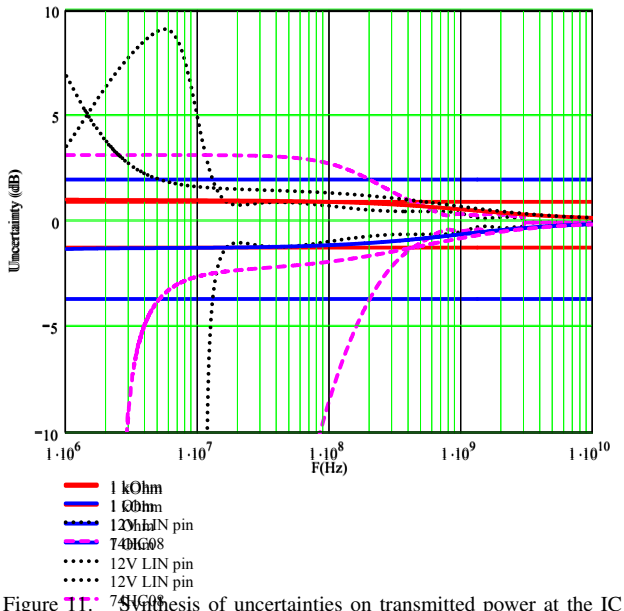

Figure 11. Synthesis of uncertainties on transmitted power at the IC input - Mixed approach

IV. Comparison between Experimental and Mixed Approaches

With the experimental approach, the different uncertainty sources identified and their influence on the transmitted power to the IC are summarized in Table I. The frequency range is splitted into 3 domains to enable a comparison with the mixed approach.

The last line provides the evaluation of the total uncertainty on the power transmitted to the IC, that must be compared with the mixed approach.

In the mixed approach, it is assumed that there are no errors due to the transmission path and the bias tees, since they are considered in the simulation model used to extract the transmitted power. Therefore, the uncertainty is only linked to the S11 accuracy used for IC modeling, and to the accuracy of the external incident power.

This finally leads to the following comparison between the experimental approach and the mixed approach (for worst case considerations).

Table I
Uncertainties per error source - Experimental approach

Uncertainty per error source	Frequency range		
	Low (1 MHz - 100 MHz)	Medium (100 MHz -1 GHz)	High (1 GHz - 3 GHz)
Bias tee	4 dB	1 dB	1 dB (but risk for higher freq.)
Difference between PCB and IC inputs	2 dB	2 to 8 dB	2 to 10 dB
Transmitted power measurement	+ 8 dB -∞	+ 2 dB - 5 dB	1 dB
Total	+ 14 dB - ∞	+ 5 to +11 dB -8 to -14 dB	4 to 12 dB

Table II
Uncertainties of both approaches

Uncertainty per Error Source	Frequency range		
	Low (1 MHz - 100 MHz)	Medium (100 MHz -1 GHz)	High (1 GHz - 3 GHz)
Experimental approach	+ 14 dB - ∞	+ 5 to +11 dB -8 to -14 dB	4 to 12 dB
Mixed approach	+ 9dB - ∞	+ 3 dB - 8 dB	2 dB
Benefit of the mixed technique (worst case)	5 dB	8 dB	10 dB

V. Conclusion and Discussions

The uncertainties estimated on the transmitted power are more or less the same with both techniques presented in this paper. Since the basic principle of a network analyzer is to measure powers also with an internal coupler, to observe the same behavior is an expected result. As soon as the impedance becomes too high or too low, accuracy becomes difficult to manage.

Nevertheless, the second technique has the advantage of taking into account the errors that could be induced by a fully experimental approach (bias tee / injection path characteristics...). In particular, when frequency increases, the management of bias tee characteristics becomes more and more difficult (high impedance in a wide frequency range). This finally provides a small advantage for the mixed technique.

In the mixed approach, the global uncertainty is mainly due to the VNA limitations for high and low impedances. If the accuracy of the DUT model could be improved, this could clearly make the mixed technique even more useful. Currently, only the RF-IV method could be thought of, but it can only be used for one- port extractions [10].

In addition to the network analyzer technique, this could help covering a wider frequency range. This would make the design flow for an IC characterization more complex and would need to be evaluated.

Finally, the mixed approach makes it possible to deal with integrated circuit pins for which decoupling capacitors are functionally mandatory. Notwithstanding the fact that in such situations, huge differences can be expected between the powers transmitted to the input of the PCB or to the input of the IC, this can also lead to important variations in the results. Depending on capacitor values, technology and layout, these influences prevent the comparison among devices without extracting the power transmitted to the device. This is the last but not the least argument to promote the mixed measurement-simulation approach.

Finally, the authors would like to make a few comments on the current DPI standard, to be discussed within the framework of the standardization committee:

- "The traces should be as short as possible and typically 1/20 of the shortest wavelength". In practice, it is difficult to comply with such objective, particularly when extending the test up to 3 GHz. In fact, the traces should be 5 mm long max (for free space propagation) and about 2.3 mm for FR4 PCB propagation. In practice, and on the generic PCB that was built, traces are 22.65 mm long. It can be assumed that this limitation is not relevant with the mixed approach.
- The suggested coupling capacitor is 6.8 nF. Due to parasitic effects, bad transmission performance can be expected until 3 GHz. Even if this can be managed by simulation, the authors suggest the use of 2 capacitors in parallel (470 nF in parallel with 1 nF provides good results).
- The bias tee, also introduced as a decoupling network in the standard, is specified to be less than 400 Ω. In practice, this is inadequate and quite difficult to manage (or better) especially on a broadband frequency range. With the mixed approach, the main constraint is the extraction of an accurate model of the bias tee, and this seems to be a more reasonable objective to achieve. The higher its impedance (compared to the DUT impedance), the lower the requested accuracy. With a fully experimental approach, it is recommended that the bias tee impedance be greater than the DUT impedance by a factor of 5 or 10 (if possible).

REFERENCES

[1] Ford, "ES-XW7T-1A278-AC - Component and Subsystem Electromagnetic Compatibility - Worldwide Requirements and Test procedures," http://www.fordemc.com, 2003.

[2] PSA Peugeot Citroën, "B21 71110 ind C - Specification d'environnement des équipements électriques et électroniques - Caractéristiques électriques," 2008.

[3] *IEC 62132-4 - Integrated circuits Measurement of electromagnetic immunity 150 kHz to 1 GHz Part 4: Direct RF power injection method*, International Electrotechnical Commission Std., 2006.

[4] F. Lafon, M. Ramdani, R. Perdriau, M. Drissi, and F. de Daran, "An Industry-Compliant Immunity Modeling Technique for Integrated Circuits," in *EMC 09 Kyoto - International Symposium on Electromagnetic Compatibility*, 2009.

[5] F. Branin, "Transcient analysis of lossless transmission lines," in *Proc. IEEE, 55*, 1967, pp. 2012–2013.

[6] Rohde & Shwarz, *Rohde & Schwarz NRVD - NRV-Z5 power sensor - Specification*.

[7] Agilent, "Application Note - Agilent, ENA 2 and 4 Port RF Network Analyzers Data Sheet ," Tech. Rep., 2007.

[8] ——, "Application Note 5989-5935EN - Ultra-Low Impedance Measurements Using 2 - Port Measurements," Tech. Rep., 2007.

[9] I. Novak, "Measuring MilliOhms and PicoHenrys in Power - Distribution Networks," in *DesignCon 2000*, 2000.

[10] Agilent, "Application Note 1369-2, Advanced impedance measurement capability of the RF I-V method compared to the network analysis method," Tech. Rep., 2001.