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Dynamic Power Estimation of FPGA-based Wireless Communication Systems

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Abstract—The growing complexity of current and future wireless communication systems makes power estimation a challenging task for designers. Nowadays, it is required to estimate power very fast in order to explore and validate design choices as soon as possible in the design flow. In this paper, we propose a new dynamic power estimation methodology for FPGA-based systems. Our methodology aims to provide accurate and fast power estimations of an entire system prior to any implementation. It also aims at making design space exploration easier. We introduce a scenario-level in order to facilitate the comparison of domain-specific algorithms. This methodology relies on an IP power characterisation phase and a behavioural simulation of the modeled system using SystemC. We show the effectiveness of our approach on typical wireless communication systems which leads to a maximum absolute error lower than 6% compared to classic estimations.

Index Terms—FPGA, Dynamic power, Power estimation methodology, XPower, System modelling, SystemC, Wireless Communication, OFDM

I. INTRODUCTION

Nowadays, more than 12 billion internet-connected devices are already available worldwide. In a near future, a study in [1] shows that the number of such systems will explode in the context of the internet of things in which billions of devices (33 billion by 2020) will share information and communicate with each other, using different communication standards and protocols. The processing capabilities of such systems will also drastically increase due to the perpetual demand for higher throughput and increased functionality.

For several years, power has become one of the main topic for both academic and industrial companies. Although achieving a high level of performances still constitutes a primary objective, low-power design strategies are employed by designers to reduce power consumption. Indeed, embedded systems are generally relying on battery as unique power supply source and high performance systems cause heat dissipation, imposing a cooling process that can be very costly for small systems. In the wireless communication domain, power consumption is becoming a key metric in the context of green technologies.

Although ASICs (Application Specific Integrated Circuit) can achieve high performances in terms of speed and power consumption, these circuits usually require a time-consuming

development and expensive costs. A current alternative solution is to make use of FPGA (Field Programmable Gate Array) devices. Such devices represent an attractive technology that increases flexibility while still achieving high performances [2]. They also make it possible to implement complex systems due to their high density of gates and heterogeneous resources. Being generally used for fast ASIC prototyping at low-cost or as hardware accelerators for real-time applications, FPGA-based systems are generally made of IP (Intellectual Property) cores. Such cores enhance design reuse and speed up development time. They also contribute to reduce the time-to-market significantly which is also a critical point for designers.

FPGA power consumption is generally divided into static and dynamic power. Static power comes from leakage currents whereas dynamic power is generated by transistors' switching activity.

The purpose of this paper is to propose a new power estimation methodology for FPGA-based wireless communication systems (with a focus on the base-band processing). In this work, we deliberately chose to focus on hardware design without any software considerations. This paper is organized as follows. Section II deals with the related works on high-level power consumption estimation. Section III promotes our proposed methodology. Section IV provides results obtained by the application of our methodology. Finally, we conclude and discuss about prospects in section V.

II. RELATED WORKS

Today, as designers want to implement a complete system into a FPGA, they usually follow a generic top-down design flow which is divided into several well-identified levels, starting from a high level behavioural description of the design to end at the layout or technology level (in case of an hardware-only implementation). These description levels are common to all hardware design flows and are obviously adapted to wireless communication designs.

In literature, there are a lot of works dealing with power estimation. Low-level power estimation methodologies and techniques are reviewed in [3, 4]. Additional references dealing with low-power techniques for FPGA-based designs can be found in [5]. From these studies, it can be noticed that estimating power using low abstraction level methodologies or tools is a time-consuming task. Furthermore, working at a low

level of abstraction does not allow designers to perform efficient design space exploration since too many choices may be considered at this level. In parallel, taking a decision very late in the design process may lead to expensive re-design costs if constraints are not met. As a conclusion, low-level approaches may not be suitable anymore for fast power estimation of future systems composed of billions of gates.

As related by the ITRS, International Technology Roadmap for Semiconductors a solution is to move up in abstraction [27]. Nowadays, Electronic System Level (ESL) has emerged and seems to give the keys to make the design of future systems easier. At system level, early decisions can be taken and may have a more significant impact than lower-level decisions on the overall system performances. Although a lot of tools make it possible to work at this level, few of them consider early power and performance estimations for FPGA-based systems.

In the wireless communication domain, theoretical performances of the algorithms are usually evaluated at high level i.e. at the algorithmic level. Several tools and languages can be employed such as the Matlab software environment from Mathworks[6] which is widely used in the community. However, this tool requires an additional package to complete the FPGA chip development such as System Generator or DSP builder, respectively from Xilinx and Altera. This approach can be really time-consuming for large designs and DSE (Design Space Exploration) becomes limited due to the prohibitive number of subsequent implementations. The flow has to be re-run from scratch at each configuration of the system.

Also based on Simulink/Matlab, an academic add-on tool called 'PyGen' is presented in [7]. The proposed approach aims to feedback power and performance details of each module of the system from lower levels (the tool enables the synthesis of parametrized designs for FPGA using System Generator tool). Although power estimations are relatively accurate, the time spent during the implementation steps seems to be prohibitive and not convenient for DSE when considering large complex systems. Furthermore, when considering streaming application models, authors assume that all the modules are active throughout the processing which is not necessarily the case. For example, the activity may depend on the application behaviour and the synchronization elements between each module.

In [8-12] are listed the main behavioural level tools and EDA (Electronic Design Automation) environment for modelling, simulating, prototyping that are used in the signal processing and wireless communication domains. Although very powerful, these tools generally do not allow designers to get any information related to the energy spent by the algorithms.

In fact, since no implementation decision is taken at this level, it would be a total nonsense to think about obtaining accurate power results using some of such tools.

In general, as designers desire to get a first estimation of their circuits' consumption, they often make use of analytical power models or eventually spreadsheets if more hardware-oriented specifications are considered [14-16]. In all these

works, power models are derived from datasheet values, real measurements or are possibly based on other works presented in the literature. The accuracy of the power estimation is generally not the priority and the main goals are to determine a global trend in terms of performances to achieve.

From a more hardware-oriented point of view, spreadsheets have been created by FPGA vendors such as XPE (Xilinx Power Estimator) from Xilinx [18] and Power Play from Altera [17] to provide early power estimations prior to any implementation. These tools are based on the user design specifications and are dedicated to a FPGA vendor technology. This approach makes use of analytical formulas to determine the average power consumption based on given parameters such as the number of resources, the clock frequency, the signal activity, the voltage, etc. Spreadsheet estimations can be refined throughout the design implementation flow, right after the design synthesis as more implementation details are known. When considering a large and complex system, power consumption of the overall system is usually determined by summing the power contribution of each block. Although useful for quick power estimations of small hardware blocks (such as multipliers, adders, etc.) the spreadsheet approach may not be well appropriate to estimate the power consumption of larger complex systems. Moreover, it does not enable to consider time and dynamic effects that may occur during the execution of the application.

As Matlab/Simulink or LabVIEW, programming languages such as C/C++ or high level description languages such as System-Verilog are also widely used to model and determine theoretical performances of communication systems. At this level of description, designers often describe their system by connecting a set of custom building blocks that are able to exchange data in a concurrent way.

In literature, most of the approaches enabling power estimation at ESL are based on SystemC [9]. This modelling language consists of a C++ library and an associated simulation kernel. SystemC is widely used and allows designers to model a system by describing both hardware and software parts in a common language. It supports several degrees of refinement where implementation details can be represented or omitted. Models can also be either functional or pure performance models. In the last case, correct timing is usually ensured by some additional control. High-level simulation can be performed thanks to the SystemC kernel which makes it possible to run cycle-accurate simulation. Considering power, SystemC does not basically support the power estimation of the modeled system and power information has to be integrated.

So far, different techniques have been proposed in the literature in order to evaluate power. Some of them use power models which have been developed from either analytical or simulations results [21-23]. In [20], power is estimated using power state machine (PSM). In [24] a methodology is presented to estimate power of FPGA designs using power models that are available at different levels of description.

Estimating power using macro-models is another solution described in [25] where SystemC is used to model the system while macro-models link power consumption values to signals'

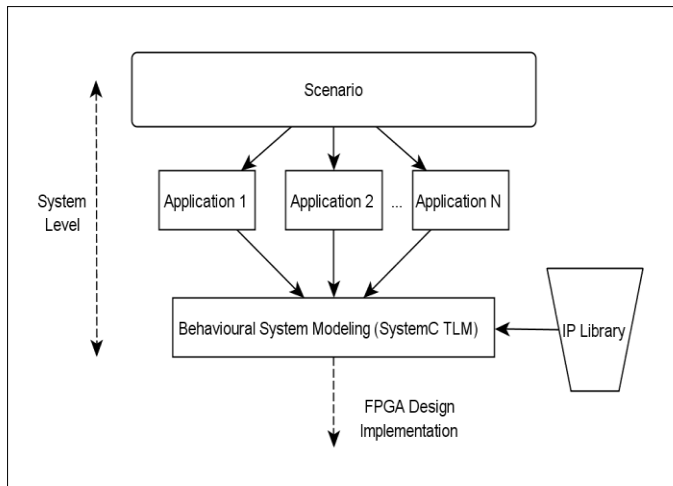


Fig. 1. Introduction of the scenario-level

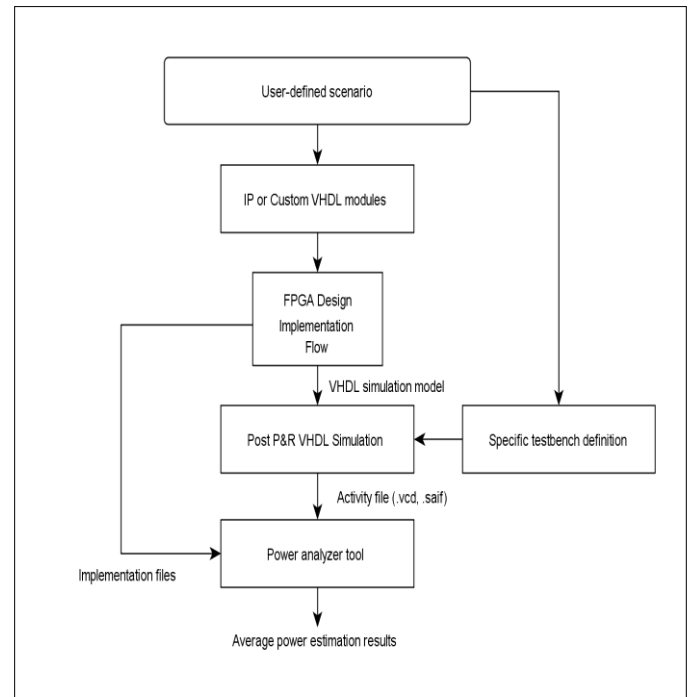


Fig. 2. IP Characterisation phase using XPower

statistics. A tool called ORINOCO is also used in [26] for the macro-modelling of fine-grain components such as adders, multipliers. This tool finally performs a high-level power estimation of small combinatorial designs.

Most of the approaches that have been described previously are addressing high-level system modelling and simulation. These studies make it possible to estimate more or less accurately the power of a system. We can also notice that there is always a trade-off between guaranteeing a fast simulation and estimating the power accurately.

At low-level, power estimation is usually time-consuming and not adapted to large and complex systems. However, the power estimation is relatively accurate due to detailed information about the system. At high level, power estimation may be a hard task to perform due to the lack of information. Power can be estimated from analytical power models or from results coming from the literature. Although very interesting in practice, these results may not be well adapted to the design of large complex systems since available studies are generally performed on specific targets and are not easily scalable. Several approaches require dedicated tools to realize the design implementation of an entire system in order to estimate the power consumption accurately. This prevents an efficient design space exploration.

From our knowledge, there is also a lack of high-level tools that enable to perform an efficient comparison between several configurations of FPGA-based systems in terms of power consumption, especially in the wireless communication domain. To circumvent these issues, we propose a new methodology, dedicated to FPGA-based wireless communication designs, striving to provide the following key points:

- Provide fast feedback of accurate power estimations from low level components to the behavioural level.
- Introduce the notion of scenario which enables to efficiently compare several algorithms

- Avoid prohibitive and time-consuming design steps by focusing on sub-components (IP Intellectual Properties or hand-coded VHDL modules) to build the overall system.
- Consider IP core temporal activities depending on the application
- Make the design space exploration much easier by optimizing the simulation time.

III. METHODOLOGY

Our proposed approach aims to rapidly provide accurate power estimations of an entire system only by focusing on each sub-element. This approach is performed in two steps: an IP characterisation phase and a global system modelling using SystemC.

The proposed methodology is also based on the definition of an additional scenario-level as described in the fig. 1. This level has been thought to facilitate the comparison of applications in the wireless communication domain in terms of performances and power consumption. Since it constitutes the first step in the design flow, designers may rapidly explore design choices for a FPGA target without entering the classic implementation flow that is often time consuming and error prone. With this approach, designers can easily compare various algorithms and validate hardware choices prior the implementation phase.

A. IP Characterisation

In the proposed approach, we made the assumption that a system can be fully represented by a set of high-level models connected to each other. Each model in the library consists of several hardware IP configurations (C_i) (i from 1 to n)

corresponding to a given set of parameters (data width, clock frequency, etc.). For each Ci configuration, the library holds the corresponding synthesized RTL description whereas the high-level model implements its behaviour. The RTL description may be expressed using a hardware description language such as VHDL or VERILOG or directly taken from a vendor library. In the latter case, each IP requires an additional controller in order to configure and manage it.

As depicted in fig. 2, each hardware IP, which corresponds to a specific parameterization of its high-level model, is then fully characterised by the different steps that constitute the design process. Design implementation is performed throughout the synthesis, mapping, place and route steps. Note that these steps are performed for a specific FPGA device that has a given number of resources and specific timing properties. In this study, we make use of the Xilinx ISE 14.4 tool. The implementation settings that can have a significant impact regarding the power estimations have been set to a standard-level in order to limit hardware optimizations. Power and performances optimizations are not the primary objectives of the methodology but it provides relative estimation values to perform algorithmic comparison.

After the IP design implementation, a post Place And Route (PAR) VHDL simulation model is generated. This file provides accurate information about delays and timing based on the final netlist. Furthermore, glitches can be recorded during its simulation. At this step, a low level power analyzer is used such as XPower Analyzer (XPA) from Xilinx. ModelSim 10.1c [13] is used as simulator and generates the activity file (Value Change Dump file .vcd or .saif file) capturing all internal signal activities. Test-benches are configured according to the user-defined input parameters and generate appropriate signals in order to record the internal activity when the IP is active and when the IP is idle.

During the simulation, we consider input patterns which are either, randomly generated binary data, or typical data. The XPA tool delivers average power consumption estimation that is composed of several terms as described by equation 1:

$$P_{\text{DYNAMIC_IP}} = P_{\text{CLOCK_IP}} + P_{\text{LOGIC_IP}} + P_{\text{SIGNAL_IP}} + P_{\text{I/Os_IP}} + P_{\text{BRAMS_IP}} + P_{\text{DSP_IP}} \quad (1)$$

With $P_{\text{CLOCK_IP}}$ the average power consumed by the clock network (including buffer and routing resources), $P_{\text{LOGIC_IP}}$ the average power consumed by all CLBs, Configurable Logic Blocks (including LUTs, FFs), $P_{\text{SIGNAL_IP}}$ the average power consumed by the interconnect, $P_{\text{I/Os_IP}}$ the average power consumed by input/output pins (which may be suppress when considering internal IP), $P_{\text{BRAMS_IP}}$ and $P_{\text{DSP_IP}}$ the average powers consumed by specific memory and Digital Signal Processing (DSP) blocks respectively.

Note that the characterisation phase has to be performed ideally for each configuration of an IP and for a specific device. In practice, only a set of configurations is actually available in the library that already contains tenths of cores. To reduce the number of configurations to analyze, a current work aims to extrapolate the results from specific IP configurations

to build a more global model by studying the trend of the power consumption according to several criteria (data size, frequency, IP specific parameters, etc.). In this way, designers will have the possibility to explore a large design space based on a minimum set of tests.

Furthermore, the IP characterisation time effort is relatively moderate due to the automation of the design process with scripts. It is also possible for designers to use these scripts in order to estimate the power consumption of a custom IP configuration and then extend the library.

B. System Modelling using SystemC

During the second step of the proposed methodology, the system is entirely modeled using SystemC. We choose this library for the considerations mentioned in section II.

For each hardware IP, we have developed the corresponding high-level model with respect to its intrinsic parameters. Moreover, all of the high-level models were built around a specific implementation model which is generic and common to all components. The implementation model is composed of a control path and a data path.

Regarding the data path, the IP functionality is basically described at the algorithmic level, in SystemC. When no detailed information is available, this description only relies on an usual representation of the IP functionality. However, an interesting feature of SystemC is that it supports both floating point and fixed point data representation. Moreover, some IP vendors also provide bit-accurate C models of their hardware IPs. They can be easily integrated into high-level models in order to provide bit-accurate results. In this way, it allows designers to evaluate the impact of data quantization choices through bit-accurate simulations.

Each IP control path is modeled as a Finite State Machine (FSM). The FSM states evolve in function of both input control signals and user-defined IP configuration parameters. They deliver output control signals that can be connected to the inputs of the associated high-level models. Note that, no implementation details are required because we only focus on the IP behaviour which is generally governed by few key signals (clock enable, input data valid signal etc.). Basically, such information is available directly from IP data-sheets. By the introduction of key signals, cycle accurate behaviour can be modeled.

An additional module called 'Power Monitor' has been devised, which aims to compute the time-activity coefficients of every IP in the system. These coefficients represent the percentage of time during which the IPs are processing data or are in an idle state. They are computed according to the evolution of the control signals along the behavioural simulation.

Finally, the dynamic power consumption of the entire system can be estimated by considering the power contribution of each IP that constitutes the system. This contribution has been quantitatively measured in the first step of the methodology and modulated according to the IP activity that has been measured in the second step during the high-level simulation.

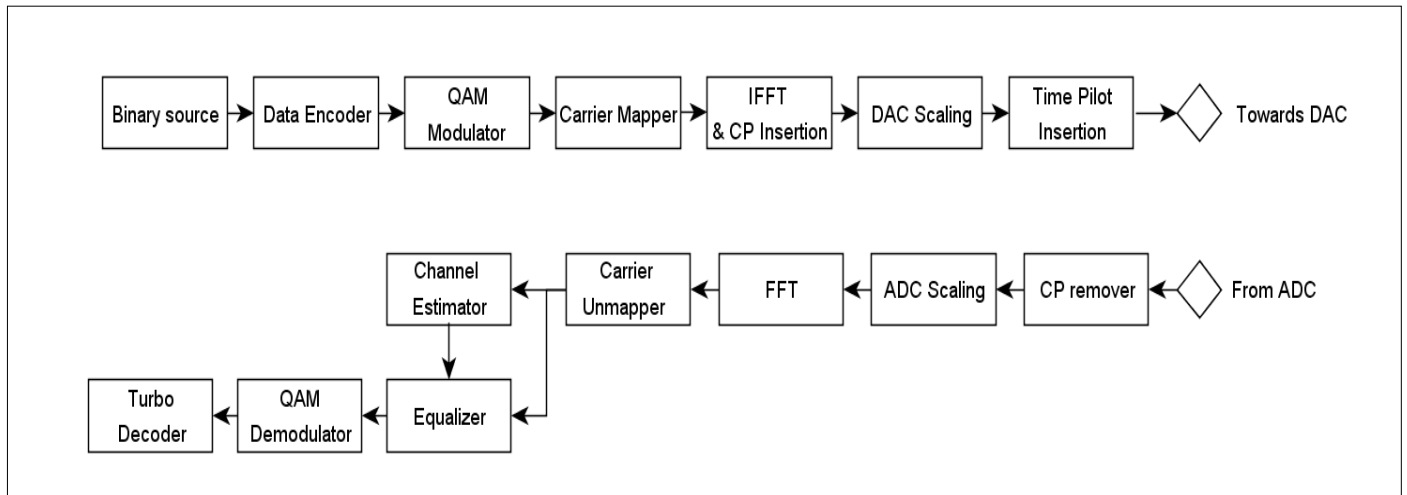


Fig. 3. Scheme of the developed SISO-OFDM communication chain

TABLE I. USER-DEFINED PARAMETERS FOR THE SISO-OFDM APPLICATIONS

Scenario Parameters	Application 1	Application 2	Application 3
Channel Coding Rate	NO	1/3	1/3
Code Block Size		1024	1024
QAM Modulation	QPSK		
(D)FFT Size	256	256	2048
Cyclic Prefix Length (in QAM Symbols)	32	32	256
Used Sub-carriers	256/256	256/256	2048/2048
Data Quantization	10 bits	14 bits	14 bits
Frame Type	1 OFDM symbol pilot every 10 OFDM symbols of data		
FPGA	Xilinx Virtex-6 LX240T		
Clock Frequency	50 MHz		

IV. USE CASES

In order to illustrate the use of the proposed methodology, we have developed a Single-Input Single-Output (SISO) OFDM communication chain in VHDL, depicted in fig. 3. It is a typical wireless communication scheme based on OFDM (Orthogonal Frequency Division Multiplexing) modulation which is a widely used modulation technique for transmitting data over wireless channels. The information is spread over several orthogonal sub-carriers at low data rate which makes transmission very robust to multipath fading. For example, OFDM is currently used in LTE or WiMAX technologies.

The transmitter is composed of a source which provides binary data to send. Data can be sent to the channel encoder if it is used or immediately processed by the QAM modulator. It aims to deliver complex I/Q QAM symbols according to the input binary symbols. The modulator supports QPSK, 16QAM and 64QAM modulations. The following module is called

TABLE II. POWER ESTIMATION RESULTS OF THE 3 SISO-OFDM APPLICATIONS

		Proposed Methodology (mW)	XPower (mW)	Abs. Error (%)
Application 1	TX	49.65	50.97	2.66
	RX	71.54	69.59	2.8
Application 2	TX	68.76	65.48	5
	RX	266.84	263.52	1.26
Application 3	TX	100.04	98.73	1.32
	RX	308.11	308.38	0.1

Carrier Mapper. It aims to allocate modulated symbols to the corresponding sub-carriers. Indeed, as in real systems, all of the sub-carriers are not used and can be canceled in order to avoid degradations in the corner band for example. Then, an OFDM modulation is performed using IFFT and a cyclic prefix is added. Output OFDM symbols from IFFT can be scaled by the DAC-Scaling module according to the Digital-to-Analog converter resolution. The last block of the transmitter realizes the time pilot insertion which will enable channel estimation at the receiver side.

The receiver performs the dual operation starting with removing the cyclic prefix and ADC data scaling. Then, FFT is computed and carrier un-mapping only keeps the data sub-carriers. Finally, channel estimation is performed on every dedicated OFDM pilot symbol and then data sub-carriers are equalized according to channel coefficients. QAM demodulation is then performed to retrieve the binary data and channel turbo decoding can be performed if it is used.

All the communication chain was described in VHDL and some blocks are IP cores were taken from Xilinx. The chain is highly configurable in function of user-defined scenario. In this way, both hardware-specific and high-level parameters can be defined. As example, a user can set the data quantization (number of bits to represents the QAM complex symbols) of

every modules, the Fast Fourier transform size, the modulation, the type of frame, the FPGA target, the frequency etc.

Several parameters of interest were defined and 3 applications were implemented and then tested. They are summarized in Table I.

After applying the proposed methodology, average dynamic power consumption results have been obtained for the 3 applications. Estimations from our methodology are compared with XPA estimations for the entire design. Results are given in Table II and correspond to the average power estimations without considering IOs dynamic power and without dynamic power related to additional implementation buffers. Simulation length was set to 5ms.

Power estimations obtained with the proposed methodology are close to the overall power consumption. It demonstrates the effectiveness of the proposed methodology according to three user-defined applications.

The results also underline the benefit of the definition of the scenario level. This level facilitates the comparison of different applications in terms of power consumption by determining the common parameters between them in a formal way. Depending on the user-defined choices, these parameters can be related to both hardware-oriented and/or higher level parameters.

Another key advantage of the proposed methodology is to provide very fast power estimation. As an example, the gate-level simulation of the SISO-OFDM communication chain can take several hours or even days to simulate few milliseconds for one configuration whereas it only takes few seconds or minutes using the system model. The gain is even more important during design space exploration when several configurations have to be tested.

V. CONCLUSION AND FUTURE WORKS

In this article, we have shown that the proposed methodology makes it possible to compare various algorithms in terms of power consumption at high level of abstraction. Additionally, the modularity of SystemC also allows designers to simulate those different configurations and schemes and validate their behaviours. Finally, one of the benefits of our methodology consists in speeding up the algorithms comparison without requiring a time-consuming development of the overall system. The major point of the methodology consists in characterising each IP individually in terms of power consumption and to make the results available at high level to take in account the activity time that is imposed by the user scenario.

The characterisation effort is not prohibitive thanks to the automation of the design process using scripts and power consumption results are saved into a specific power library that may obviously be re-used by the designer.

As future work, we will focus on algorithm comparison of MISO-OFDM and MIMO-OFDM systems in terms of power consumption.

Specific considerations of performance metrics such as BER (Bit Error Rate), throughput will be under study. Different standards such as 3GPP Long-Term Evolution (LTE) are currently being investigated. Another perspective of study

will be to model the power amplifiers and RF stages which play a significant role in the power consumption of wireless communication systems.

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