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# Dynamic Power Evaluation of LTE Wireless Baseband Processing on FPGA

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**Abstract**—Mobile networks and user equipments continuously evolve to circumvent the data traffic growth and the increasing number of users. However, the complexity and heterogeneity of such systems (3G, LTE, LTE-A, etc.) makes power one of the most critical metric. In this context, power estimation has become an unavoidable task in the design process. In this paper, a dynamic power estimation methodology for FPGA-based systems is presented. It aims at providing accurate and fast power estimations of an entire system prior to its implementation. It also aims at making design space exploration easier. We introduce an innovative scenario-level in order to facilitate the comparison of domain-specific systems. We show the effectiveness of our approach on several LTE baseband configurations which leads to a low absolute error, compared to classic estimations. It also exhibits a high speed-up factor which is determinant during design space exploration.

## I. INTRODUCTION

Today, the data traffic that is generated on mobile networks continues to grow rapidly. According to [1], global mobile data increases of 69% in 2014 and it will have a compound annual growth rate of 57% from 2014 to 2019.

To deal with these issues, mobile networks and user equipments tend to constantly adapt their processing capabilities. Among all possible solutions, a popular example is the LTE standard. The complexity of systems like LTE makes their design and development a challenging task, especially when they are implemented in embedded systems in which specific constraints have to be taken into account (power, size, performance, etc.). The number of parameters that can have an impact over power consumption makes the power estimation even more difficult. As the new technologies clearly enhance the performance in terms of throughput, QoS, it also implies a higher power consumption and more heat dissipation.

One of the most popular families of digital circuits in embedded systems are the Field Programmable Gate Arrays (FPGA). These devices represent an attractive technology and make it possible to implement complex systems due to their high density of gates and heterogeneous resources. As compare to ASIC that can achieve better performance [2], FPGAs offer more flexibility. FPGA-based systems can be made of IP (Intellectual Property) which are hardware cores that facilitate design reuse and speed up development time. Their power consumption is generally divided into static and dynamic power. Static power comes from leakage currents whereas dynamic power is generated by the transistors switching activity as soon as the circuit is active.

In wireless communication systems, complexity of baseband processing is still increasing and estimating power and performance of such systems has become a hard task. Moreover, the power consumption depends on system parameters (e.g. the number of antennas, the modulation and coding scheme, the type of frame to process, etc.) as well as technological parameters (e.g clock frequency, data width, the FPGA type, its speed, etc.).

The purpose of this paper is to propose a power estimation methodology for FPGA-based wireless communication systems. Its objectives are multiple : 1) it aims at facilitating the design space exploration and providing fast power estimation at high level 2) it aims at considering dynamic IP time activities that depend on the application and the testbench which have a deep impact on the power estimation. In this work, we deliberately chose to focus on hardware design without taking any software considerations into account. Moreover, we decided to only focus on the baseband processing. The study of RF circuits will be out of scope of this study.

This paper is organized as follows. Section II deals with the related works on high level power estimation. Section III promotes our proposed methodology. Section IV provides results that have been obtained by applying our methodology on a LTE DL SISO-OFDM system. Finally, we conclude and discuss about prospects in section V.

## II. RELATED WORKS

Power estimation in FPGAs has been a wide topic of research for several decades. The various related techniques are commonly classified according to the abstraction level of the system to implement i.e. the level of details to describe this system.

Generally, as designers want to implement a complete system into a FPGA, they follow a generic top-down design flow, described in Figure 1. This multi-levels flow starts from a behavioural description of the design and ends at the layout level in which the bit-stream is generated. Note that these description levels are common to all hardware design flows and are obviously adapted to wireless communication designs.

It has already been noticed that estimating power at low-level of abstraction or performing real measurements can obviously deliver accurate results, but is also very time-consuming. This precise estimation relies on the fact that the system is completely defined at this last level. This also forces

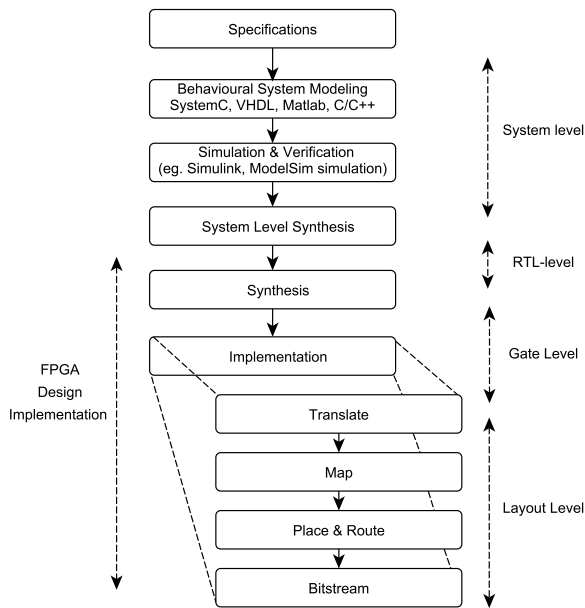


Fig. 1. Representation of the different abstraction levels from specification to FPGA bit-stream generation

designers to take a decision very late in the design flow. For this reason, it is clear that low-level approaches are not suitable for fast power estimation of future systems composed of billions of gates.

At System level, early decisions can be taken and may have a more significant impact than lower level decisions on the overall system performance and power consumption [3]. This is especially true when the primary objectives are the design of low-power systems. Although a lot of tools make it possible to work at this level, few of them actually enable both power and performance estimations because implementation details are not available at this level.

In the wireless communication domain, a system is usually described using modelling and simulation tools such as the Matlab/Simulink tool from Mathworks [4] which is widely used in the community. Other tools such as Ptolemy [5], Labview [6], Cadence System development Suite [7] are some examples of behavioural-level tools and Electronic Design Automation (EDA) environment for modelling, simulating, prototyping that are used in the signal processing and wireless communication domains.

Although very powerful, some tools basically do not integrate power estimation in their design flow. These tools do not allow designers to get any information related to the energy spent by the algorithms. For example, Matlab basically does not enable power estimation without an additional package to complete the FPGA chip development such as System Generator from Xilinx.

To address the lack of detailed information at high level, power and performance details can be feedback from lower levels to Matlab/Simulink based on the synthesis of param-

eterized designs for FPGA using the System Generator tool [8].

Another way of obtaining global estimation of circuits consumption consists in using general analytical power models. In [9], [10], power models or estimations are derived from datasheet values, real measurements or are possibly based on other works presented in the literature. The accuracy of the power estimation is generally not the priority since the main goals are to determine a global trend in terms of performance to achieve.

Other approaches are based on specific power models in which hardware is totally defined. In [11], the development of multi-level power models enable to estimate power of FPGA designs all along the design development in function of the available information at each level. Power models are built using the Functional Level Power Analysis (FLPA) methodology [12], [13]. Another power modelling approach is described in [14]. The methodology called FLPAM, allows to model area and power of FPGA-based Custom IP cores. The authors focus on modelling the dynamic power (clock, logic, signal, I/O) of the different component of the FPGA and on performing non linear regressions in function of system variables such as area, frequency etc. The overall dynamic power is then estimated from these parameters, for each IP in the design.

Power models of IP cores for Multi-Core System-on-Chip targets, are built from low-level simulations and mode recognitions based on key signals in [15]. Although very interesting in practise, this approach seems too power-oriented and does not take into account other metrics such as the global performance of the system.

FPGA vendors have also contributed to the development of early power estimation tools called spreadsheets as Xilinx Power Estimator (XPE) [16] from Xilinx. The objective of these tools is to provide early power estimates based on the user design specifications, prior to any implementation. Average power consumption is estimated using analytical formulas based on parameters such as the number of resources, the clock frequency, the signal activity etc. Spreadsheet power estimations can be refined throughout the design implementation. Nevertheless, obtaining power estimations is generally a long and tedious task, especially when large and complex systems are considered.

An efficient way to deal with system complexity consists in using high level languages such as C/C++ or high level description languages e.g. System-Verilog or SystemC [17]. As an example, SystemC consists of a C++ library and its associated simulation kernel which enables to run cycle-accurate simulations. SystemC seems to be convenient to model hardware designs. However, it does not basically enable power estimation and additional information has to be provided. To this purpose, power can be estimated using macro-models [18] or Power State Machines (PSM) [19].

Finally, as related in the previous examples, power estimation in FPGAs can be performed using many methodologies, modelling techniques or languages. It can also be performed

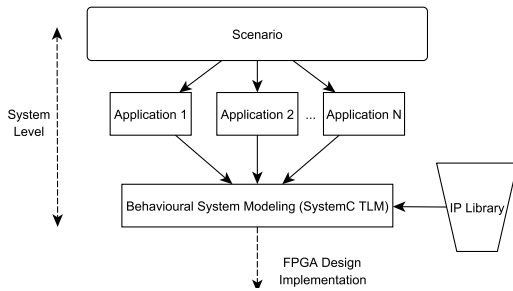


Fig. 2. Introduction of the scenario-level

at different levels of abstraction. At system level, power estimation may be a hard task, due to the lack of information, and may lead to poor accuracy. Power can also be estimated from generic analytical models or from values coming from the literature. Although very interesting in practice, exploiting these results may not be well adapted to the design of large and complex systems since available studies are generally performed on specific targets and are not easily scalable. Several approaches require dedicated tools to realize the design implementation of an entire system in order to estimate the power consumption accurately. This prevents an efficient design space exploration. From our knowledge, there is also a lack of high-level tools that enable to perform an efficient comparison between several configurations of FPGA-based systems in terms of power consumption and performance, especially in the wireless communication domain. Power modelling of cores is also interesting but it usually do not consider the performance of the overall system.

### III. PROPOSED METHODOLOGY

The proposed methodology is based on the assumption that any system can be represented by a group of hardware blocks such as IPs that are dedicated to a specific function e.g. Fast Fourier Transform (FFT). The main idea consists in providing power estimations of a global system, only by taking accurate information from each of its sub-elements. Each sub-element has been fully characterized and is available in a library. One of the main purpose of this approach is to prevent high development time of the entire system and related costs by encouraging models re-use.

The critical entry point of the methodology is the innovative definition of a scenario. This term has already been introduced in [20], [21] but refers to a different concept as in this work. In our case, a scenario refers to a set of parameters which are common to several applications in the same domain. It is composed of systems and hardware-oriented parameters which have an impact over power and/or performance.

An example of scenario in the wireless communication domain may refer to the modulation type, the coding scheme, the IFFT size, and also technological parameters such as the clock frequency, the FPGA target, the data quantization etc. It constitutes the meta-model of the system. As depicted in

Figure 2, each application corresponding to a defined set of parameters is considered as an instance of a scenario.

The proposed methodology is performed in two stages: an IP characterization phase and a global system simulation using SystemC as modelling language. The first stage of the methodology consists in building a library of systemC IP that have been fully characterised in terms of power and behaviour at both low and high levels. To this purpose, we use a classical low level power estimation tool from Xilinx called XPower Analyzer (XPA) that enables to estimate the average power consumption and describe the behaviour of each IP at system level.

A classical characterisation flow has been applied to each IP in order to obtain accurate power estimation. A post-place and route VHDL simulation model, including timing properties, is generated under the Xilinx design software environment called ISE (v14.4). This model is then simulated using the Modelsim SE-64 10.1c [22] tool in order to record the internal activities of all signals that constitute the IP. Based on specific test-benches, two simulations are performed. The first one is performed when the IP is active and the other one when the IP is idle. Finally, power is estimated using XPA in a classical way based on the activity file and additional implementation files i.e. constraint and design netlist files. Note that XPA delivers a complete report on the average power used by clock, logic, signals, memories, DSP blocks, etc.

The characterisation process using XPA and the timing simulation have to be re-run several times for each set of parameters. The characterisation process is effective when all power estimation results have been obtained for every IP that are used in the system. This first stage is quite tedious but has been relieved by the use of automated scripts that also spare time and reduce the number of errors.

After obtaining the power metrics for each IP configuration, this information is added to SystemC models that have been built. All IPs share the same implementation model that consists of a data path and a control path. These paths can be described at different levels of abstraction regarding the expected accuracy and the simulation speed. A major contribution of the work is the introduction of key signals that aim at identifying at high level if the IP is active or not and thus determine which power model has to be considered. Indeed, two patterns of test that are applied to a given circuit can lead to very different power consumption results. In a real system that is made of several IPs, the behaviour of one IP can have a large impact on the others. The importance of taking into account the timing activities of each IP based on the application parameters are exhibited in Figure 4. From this figure, it can also be noticed that different sets of IP parameters can lead to different timing behaviours and finally to different power consumption models. Although XPA delivers average power consumption results, dynamic effects of the application can be considered with our approach.

The second stage of the methodology is described in Figure 3. The system is built by connecting the SystemC models that have been developed during the first stage. Once the SystemC

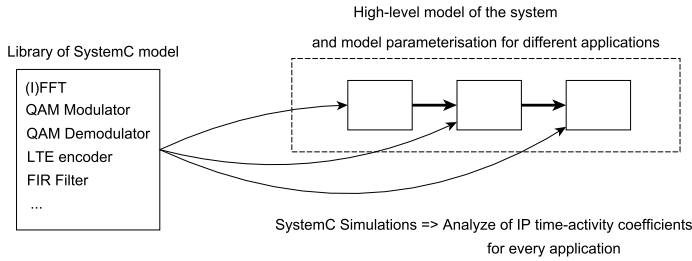


Fig. 3. High-level system modelling and simulation using SystemC

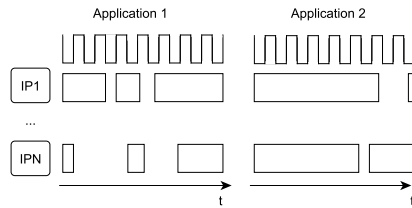


Fig. 4. IP time-activities for different applications

model of the entire system is realized, the users can define their applications i.e. instances of a scenario by setting up the system parameters. Simulations are then performed and time activity coefficients of all the IP models can be obtained. Finally, the dynamic power consumption of the entire system can be estimated by considering the power contribution of each IP that constitutes the system.

Thanks to the proposed methodology, several systems as LTE or WiMax baseband processing can be studied. Each block that composes such systems has to be characterized and then modelled using SystemC. A library of hardware and SystemC models is already being developed.

#### IV. USE CASES

Long-Term Evolution (LTE) is the fourth generation (4G) of radio technology that has been standardized by the 3GPP cooperation. The main objectives of LTE aim at reducing the latencies, improving throughputs while dealing with an increased number of users.

In order to meet these objectives, the LTE physical layer combines several technologies such as Orthogonal Frequency Division Multiple Access (OFDMA) for downlink (DL) and Single Carrier Frequency Division Multiple Access (SC-FDMA) for Uplink (UL).

According to the standard [23] and to an overview presented in [24], the main OFDM parameters in LTE are summarized in Table I.

The LTE frame, with a 10 ms duration, is built around different physical channels and signals that carry and exchange specific data between a base station and the user mobile equipment. Two frame structures are defined in LTE. We focus on the structure of type 1 that supports Frequency Division Duplex (FDD) mode whereas type 2 uses the Time Division

TABLE I  
MAIN DOWNLINK OFDM PARAMETERS IN LTE

Spectral Bandwidth (MHz)	1.4	3	5	10	15	20
Sub-carrier spacing	15 kHz					
Used sub-carriers	72	180	300	600	900	1200
Used Resource Blocks	6	12	25	50	75	100
(I)FFT Size	128	256	512	1024	1536	2048
OFDM length	66.67 $\mu$ s (without Cyclic Prefix)					
Cyclic Prefix length	normal: 5.21 $\mu$ s (1st symbol) then 4.67 $\mu$ s extended: 16.67 $\mu$ s					

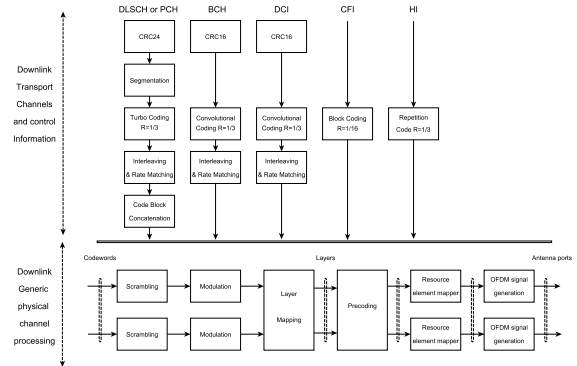


Fig. 5. LTE TX Downlink processing for each physical channel without references and synchronisation signals

Duplex (TDD) mode. As depicted in Figure 5, the channel concept enables to identify the specific type of data that are transmitted on the radio interface. For DL, there are 6 physical channels and 2 types of physical signals. We focus on Physical Downlink Shared CHannel (PDSCH) that is dedicated to user data.

Different processes (modulation, coding, etc.) are performed according to the nature of the physical channels as shown in Figure 5. Physical Signals are generated by the physical layer and are known at the receiver. They distinguish Reference Signals (RS) that are allocated both in time and frequency and enable channel estimation, beamforming, channel demodulation and Synchronisation Signals (SS) that are mainly used for time and frequency synchronisation, CP length determination, cell search, etc.

As depicted in Figure 6, we have developed a simplified LTE DL transmitter that corresponds to the PDSCH processing (user data) and CS. The description has been made using the VHDL hardware description language.

The transmitter is composed of a Xilinx IP called *DLChannelEncoder* that adds checksum i.e. crc, enables transport block segmentation, channel coding, performs rate matching and code block concatenation. Then, binary data are sent to the scrambler that mixes the binary stream with a cell-specific pseudo-random sequence. A QAM modulation is then performed in order to map the binary stream into I/Q complex symbols. Cell-Specific Reference Signals (CRS, also named as pilots) are generated by a dedicated block. The resource

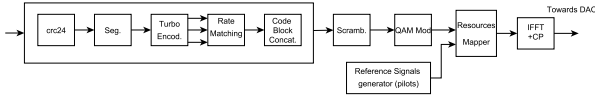


Fig. 6. Scheme of LTE TX DL processing for PDSCH channel in SISO configuration

TABLE II  
DEFINED SCENARIOS AND APPLICATIONS

Scenario	Appli. 1	Appli. 2	Appli. 3	Appli. 4
Channel Coding	Rate=1/3 Code block size = 1024			
QAM Modulation	QPSK			
(I)FFT Size	256	512	1024	2048
Data quantization	14 bits			
FPGA Type	Xilinx Virtex-6 LX240T			
Clock Frequency	50 MHz			

TABLE III  
POWER ESTIMATION RESULTS AND ESTIMATION TIME OF THE 4 APPLICATIONS

	Proposed Methodology		XPA		Abs. Error %	Speed Up Factor
	mW	s	mW	s		
Appli. 1	83.63	1.18s	77.14	1h12	10.83	x3661
Appli. 2	100.38	1.42s	101.54	2h45	1.14	x6971
Appli. 3	127.41	2.45s	127.15	8h16	0.21	x12146
Appli. 4	143.27	3.91s	139.89	15h30	2.41	x14271

mapper aims at generating the corresponding LTE frame as defined in the standard. Finally, the OFDM modulation and cyclic prefix insertion are performed.

For this system, some assumptions have been made:

- the simulation time corresponds to the generation of half of the LTE frame (70 OFDM symbols, 10 slots)
- some parameters for the CRS generation have been set such as the ID cell
- all the RB used for PDSCH and CRS are considered ; data from other channels are deliberately set to 0.

A scenario has also been defined in order to efficiently compare different applications in terms of power and performance. This is summarized in Table II. It can be noticed that (I)FFT sizes are different for the 4 studied applications.

Each hardware IP that composes the hardware system has been characterized independently and SystemC models have been built according to the proposed methodology. Simulations have been performed at high-level for the 4 applications and corresponding IP time-activities have been obtained. Finally, the results based on the proposed methodology have been compared with classical XPA estimation that have been performed on the entire system. Results are provided in Table III for the different applications.

It can be noticed that power estimations resulting from our methodology are close to the XPA results. The maximum

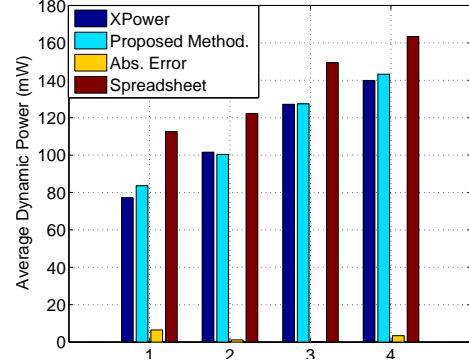


Fig. 7. Average TX dynamic power for the 4 applications

absolute error is around 10% (due to relatively small power estimation values). A comparison is also performed with the results obtained by a typical spreadsheet approach (sum of average powers) that are indicated by the red curve. Our methodology clearly outperforms the classical way of power estimation. Moreover, as described in Table III, we estimate the power consumption of the different applications in few seconds. Note that cycle accurate simulations took hours using both Modelsim and the XPA tool, in a classical way. Moreover, we did not consider the time spent for the design implementation that is also time-consuming as compared to our approach that only requires the compiling of the SystemC models.

According to the Figure 7, if the power consumption related to the circuit is only considered, application 1 may be selected, at first glance, because it consumes less power than the others. In addition to power, domain-specific metrics can also be evaluated very fast in the proposed approach. For example, the Energy Efficiency (EE) of a wireless communication system can be used to evaluate the capacity of a system to transmit the maximum of data with a minimum of energy. EE is usually defined as follows in a SISO (Single Input Single Output (SISO)) channel:

$$EE(\text{bit}/J) = \frac{C(\text{bit}/s)}{P_{Total}(W = J/s)} \quad (1)$$

with  $C$ , the average channel capacity in SISO configuration:

$$C = W.E[\log_2(1 + \frac{|h|^2 P_t}{N_o})] \quad (2)$$

with  $W$  the bandwidth,  $h$  the channel fading coefficient,  $N_o$  the normalized unilateral spectral density of noise,  $P_t$  the power allocated for data transmission.  $P_{Total}$  is the average total power ( $P_{Total} = P_c + P_t$ ) with  $P_c$ , the average power consumption of the circuit.  $P_c$ , is often neglected or omitted when large base stations (BS) are considered. However, this power consumption is no longer negligible for micro, pico or femto BS [25]. In our case, we take into account the power consumption of the baseband processing during the EE evaluation.

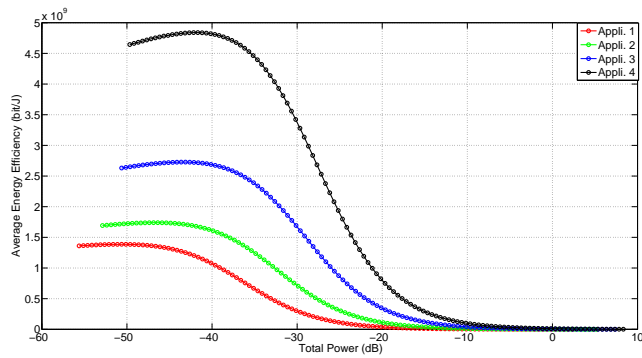


Fig. 8. Energy Efficiency versus Total Power for the 4 applications

As shown in Figure 8, the EE was computed for the 4 applications. It can be noticed that the EE of application 4 is higher than the others. This is due to the largest bandwidth and thus the largest capacity. However, more hardware resources are used for application 4 which leads to a higher power consumption. As previously mentioned, if only power is considered, application 1 should be selected. According to the EE metric, the application 4 has to be favoured. This clearly underlines the benefit to take into account both high and low-level details when such metrics are evaluated.

## V. CONCLUSION AND FUTURE WORKS

In this paper, we have presented a system-level power estimation methodology for FPGA-based designs that are built around IP hardware blocks. The methodology has been evaluated on the LTE DL physical layer and provides fast and accurate power estimations. The introduction of the scenario concept enables to efficiently observe the impact of one parameter or another on the power consumption and the performance. Moreover, domain-specific metrics can be studied such as the energy efficiency based on realistic values. Finally, the proposed methodology allows to compare several systems in an efficient way in order to obtain the best trade-off between consumed power and performance.

As future works, the proposed approach will be used to compare several baseband processing schemes of various wireless communication systems such as LTE and WiMAX. Extended configurations such as multiple antennas systems will be investigated. Moreover, we aim at integrating additional power consumption models of RF stages in order to consider all the elements of a wireless communication system and provide an overall power estimation.

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