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Computer-aided reliability-aware approach for analog/mixed integrated circuits and systems

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Résumé

The paper introduces the technology scaling induced reliability problems. Based on BSIM4 transistor model, nominal ageing simulation and statistical methods are integrated as an efficient computer-aided approach that applies to reliability analysis of analog/mixed circuits and systems. The ageing varied response surface modeling (RSM) is proposed to represent both ageing and process variations induced degradation. Dynamic comparator is used to verify the proposed method. Furthermore, it is discussed that the proposed method is competent for reliability study in Analog and Mixed-Signal (AMS) circuits and systems.

1. Introduction

The continuing scaling of CMOS technology brings the SoCs into new conditions. Integrated circuits and systems meet reliability challenges [1]. Reliability problems mainly include dynamic effects (i.e. temperature variations), spatial effects (i.e. manufacturing process variations) and temporal effects (i.e. ageing effects). These problems impact the ICs performance and their service lifetime. Traditionally, circuits/systems are often designed conservatively (e.g. leaving large design margins, worst case design) to guarantee reliability. However, these overdesign strategies are pessimistic.

AMS circuits/systems show a trend of high-integration and complexity in current nanometer technologies. Systems such as sigma-delta analog-to-digital converters (ADCs), RF frontends are constituted with many blocks (e.g., sensors, analog circuits, digital logic circuits, processors). Various blocks that appear on a chip with ultra scaled CMOS technology bring reliability bottlenecks. The development of proper reliability-aware approach is very essential.

In this paper, we present a computer-aided reliability approach for reliability simulation of analog/mixed ICs and systems. The rest of the paper is organized as follows. Section 2 presents different reliability problems. Section 3 illustrates our approach. In Section 4, a op-amp in 65nm CMOS technology is used to demonstrate the proposed method. The method is discussed with AMS/RF circuits/systems. Finally, conclusions are posed in Section 5.

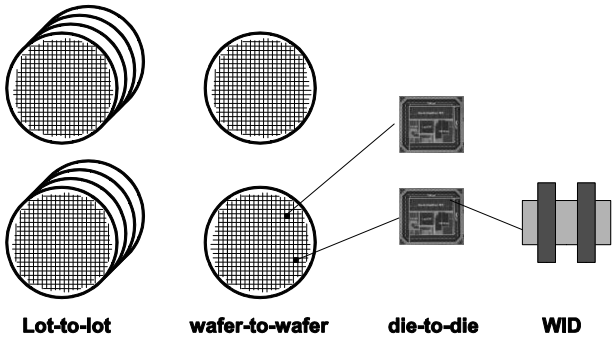

Figure 1: Parametric process variations: lot-to-lot, wafer-to-wafer, die-to-die. Intra-die variations (WID) occur within a die.

2. Previous work

2.1 Ageing effects and process variations

In this paper, Hot Carrier Injection (HCI) and Negative Bias Temperature Instability (NBTI) are considered as the main ageing effects. HCI emerges from the shrinking of transistor dimension and the electric field increasing in the channel. When HCI happens, the hot electrons overcome the potential barrier and inject into gate oxide due to high lateral electric field near the drain, which result transistor parameters shift (e.g. threshold voltage (V_{th}), mobility (μ_n)) over time. For NBTI, when negative gate bias is applied to PMOS, the transverse electric field is generated. The generation of the interface trap will cause an increase in V_{th} in PMOS transistor.

On the other hand, transistor parametric process variations can be divided into two main categories: physical variations and environmental variations [2]. As shown in Figure 1, physical variations exist during SoCs manufacturing phase, which can be further decomposed into: lot-to-lot, wafer-to-wafer, die-to-die and intra-die (within die, WID) variations. Environmental variations include the fluctuations in supply voltage, environment temperature and switching activity, which arise during the usage of ICs.

2.2 Reliability of analog/mixed circuits and systems

Reliability problems of AMS circuit/systems have been considered in many published work. In [3], a design for reliability method is proposed and developed for AMS/RF circuits. A digital controlled oscillator (DCO) has been studied. Ageing degradation can be improved by

applying design for reliability methods. In [4], a continuous-time (CT) second-order sigma delta modulator with return-to-zero (RZ) feedback (see Figure 2) is implemented. Reliability study on the building blocks shows that feedback loop is less reliable than loop filter. DAC is the most sensitive block.

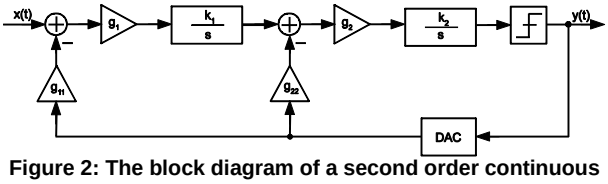

Figure 2: The block diagram of a second order continuous time Sigma-Delta modulator. At circuit level, we have OTAs in loop filter, comparator (quantizer), digital-to-analog converter (DAC) and clock phase generator.

3. The simulation method and framework

As shown in Figure 3, the co-evaluation flow begins with ageing model selection (HCI and NBTI). The schematic of designed circuit and the stress time are the input of the ageing simulation process [5][6]. With ageing degradation models, after extracting fresh netlist of designed circuits, a transient simulation is performed to generate an aged circuit netlist. On the branch of process variation, after filter out less important BSIM4 parameters, selected parameters are set up with a proper DoE mode. Ageing effect and process variation are evaluated by circuit simulator. Nominal simulation with transient and DC analysis is performed at transistor level. Other analysis such as AC, PSS and Monte-Carlo can be performed with saved aged circuit netlist (degradation information included). Simulation data processing is followed in order to plot response surface. RSMs are used to help designers to obtain intuitionistic reliability information at circuit design phase. For ageing-sensitive circuits, varied RSMs are used to estimate ageing and variability. Meanwhile, for ageing-immune circuits, a fixed RSM can supply variability information to designers [7]. Relevant statistics methods for BSIM4 parameters are presented in Table I.

RSMs can display graphically the mathematical relationship between BSIM4 process parameters and circuit performance. It can help designers estimate varied and aged circuit performance efficiently. The key point of RSM is to select a proper tradeoff between estimation accuracy and computational cost. Sometimes, using linear model is hard to achieve adequate accuracy, quadratic model or even cubic model is required. The accuracy of RSMs can be evaluated by root-relative-square error (RMSE).

Table 1: Statistical methods and functions in general

Statistical methods	Functions
Correlation analysis	Screen out uncorrelated BSIM4 process parameters
Regression analysis	Screen out less significant BSIM4 process parameters
Design of experiments (DoEs)	Simulate circuit performance with controlled experiments
Response surface Modeling (RSMs)	Map BSIM4 process parameters to performance parameters

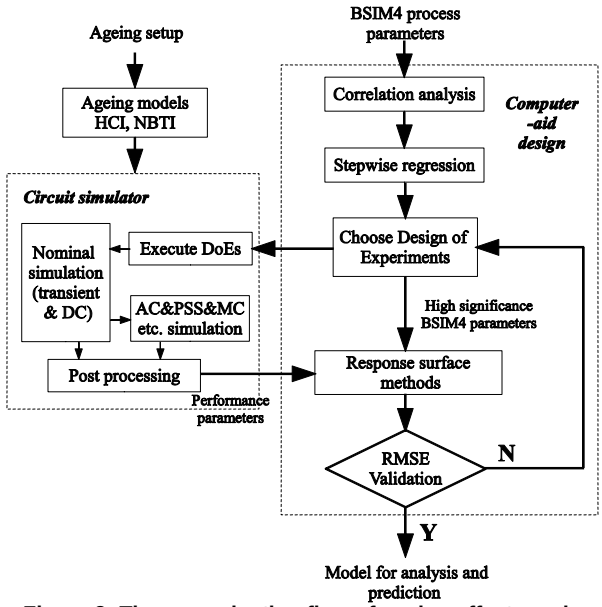

Figure 3: The co-evaluation flow of ageing effects and process variations.

4. Evaluation and discussions

At circuit level, the proposed approach is evaluated with a dynamic comparator (see Figure 4) and a folded-cascade single stage op-amp (see Figure 5), both are with 65nm CMOS technology. Reliability simulation of HCI and NBTI effects is performed with ELDO simulator [8] (maximum ageing time = 20 years). The comparator shows immunity to HCI and NBTI effects. For process variation, the process induced variation in offset voltage is shown in Figure 6. Comparing to Monte-Carlo (MC) process variation analysis, better computational efficiency is achieved. This method can help designers know the detailed variation of certain parameters (i.e., V_{th0}, u_0) at physical level. Figure 7 shows the RSM in op-amp which related V_{th0} and T_{ox} (oxide thickness) to DC gain.

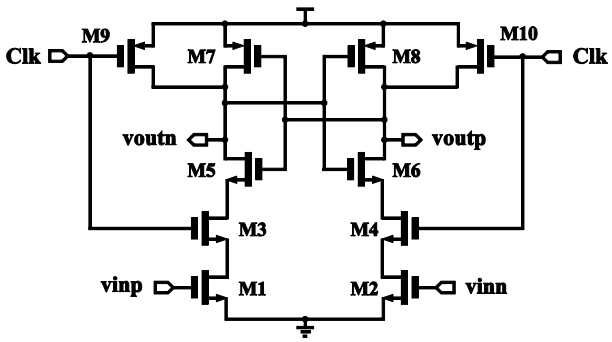

Figure 4: The schematic view of the dynamic comparator

With hierarchical behavioral modeling and bottom-up approach, this method can be extended to AMS circuits/systems. Behavioral modeling is applied to extract circuit non-ideal effects of each building block and then simulate the performance at the system level. Bottom-up approach is to model a system with an ascending order. Starting from the low-level (e.g. physical level), individual devices in the system are designed in detail and then linked to high level, until the

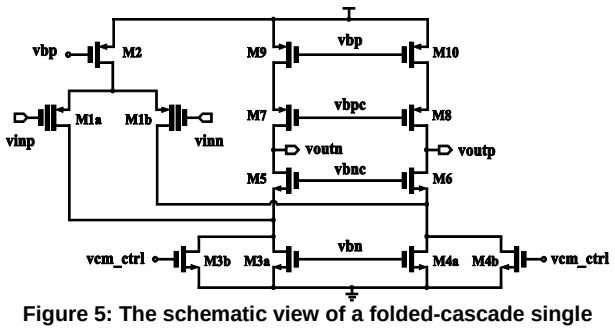

Figure 5: The schematic view of a folded-cascade single stage op-amp

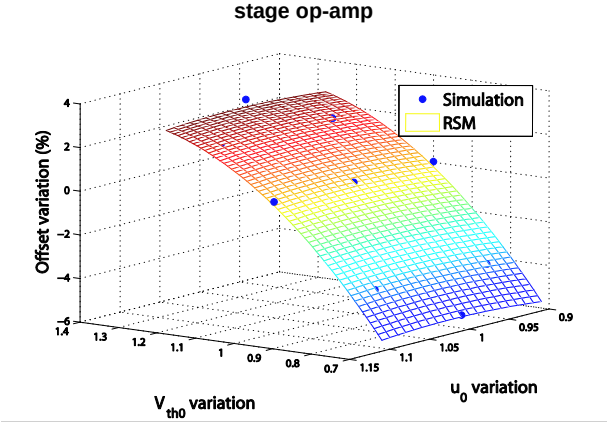

Figure 6: Dynamic comparator: RSM between BSIM4 parameters and circuit performance

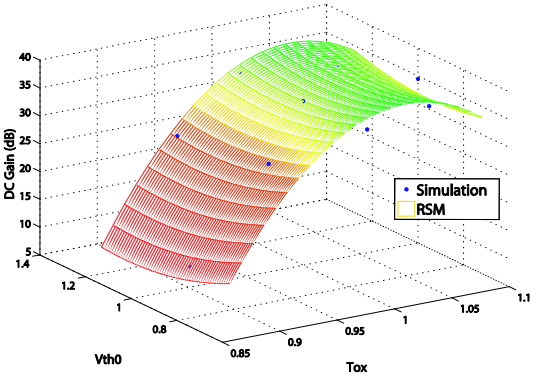

Figure 7: Op-amp: RSM between BSIM4 parameters and circuit performance

high-level system design is finished. Reliability information in Figure 6 and 7 can be propagated to the system level. The comparator and op-amp are behavioral simulated in a CT sigma delta modulator. The performance is simulated by sigma-delta toolbox [9]. Another RSM (see Figure 8) is plotted between

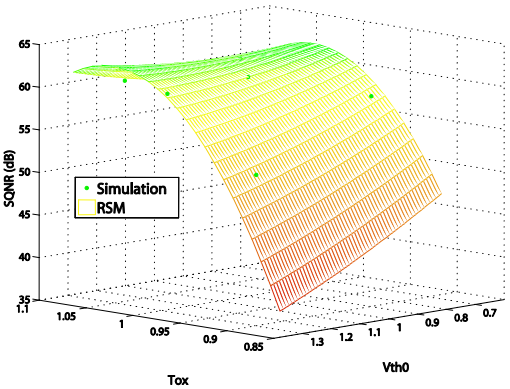

Figure 8: RSM reflects process parameter to ΣΔ modulator performance (SQNR)

physical level and system level. We find that the variations of t_{ox} influences system performance. A 8% shift of t_{ox} can degrade SQNR from 60.5 dB (ideal case) to 43 dB.

In the view of computation efficiency, it costs 17 runs of circuit level simulation (8 runs to find critical parameters, 9 runs with DoE). With this proposed methodology, in total it takes 45 minutes to get reliability performance (process variation and time dependent ageing degradation) of the designed ΣΔ modulator.

5. Conclusions

In this paper, reliability problems have been studied in AMS integrated circuits and systems. A reliability aware simulation method has been proposed and verified in 65nm CMOS circuit. RSM is used to display graphically the reflection from BSIM4 parameters to circuit performance. Reliability simulation methods for AMS/RF systems have been discussed. It can help designers get the process variation and ageing information in an early stage. Thus reliability information can be provided in an early stage of design loop. Efficient computation is achieved to help designers know detailed variation of critical process parameters.

6. Acknowledgments

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