Key parameters design for online battery electrochemical impedance tracker

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European Battery, Hybrid and Fuel Cell Electric Vehicle Congress
Brussels, Belgium, 2nd - 4th December 2015

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Abstract

New applications in transport and energy storage require the use of Lithium-ion batteries. Advanced battery management systems including electrochemical impedance measurement are studied for the determination of the state of the battery, the prediction of the autonomy, the failure and security management. Taking into account constraints of cost and simplicity, we propose to use the existing electronics of current control and we evaluate the effect of the electronics design on the performance of a frequency evolutionary estimation of the electrochemical impedance. This recursive method relies on a wideband active approach and provides both an accurate estimate of the impedance in the frequency area and a tracking of its temporal variations. Benefits are the limitation of the data memory required and the amount of operations that can be completely carried out by a target such as a microcontroller. We propose a methodology to design the key parameters of electronics in function of the frequency band of interest and the desired accuracy. We highlighted that electronics of conventional BMS can host this tracking algorithm, with analog to digital converters of 10 bits or more, having an analog stage to adapt their dynamics, and that microcontrollers can be enough powerful to perform calculations, both in terms of number of operations and speed of execution. This design strategy has been applied to define a prototyping environment for a BMS based on an ARM microcontroller which is expected to provide the tracking impedance of a battery every 250 ms with less than 0,5 % of error.

Keywords: lithium battery, BMS, impedance spectroscopy

1 Introduction

New applications as electric or hybrid transport, smart grid energy storage or connected objects require the use of batteries. Most of the time, Lithium-ion batteries are the chosen technology because of their outstanding performance such as high volumetric energy density, long calendar and cycle lifetime, and low self-discharge rate [1]. Efficient battery management system (BMS) is then important for the determination of the state of the battery, the prediction of the autonomy of the powered device, the management of the failure and the security. Classical BMS are systems which embed state estimators based on external measurements such as the current i(t) flowing through the battery, the voltage u(t) across its terminals and its surface temperature [2]. From

these quantities, the electrochemical impedance of the battery can be evaluated. It is a useful parameter representative of the dynamics of electrochemical systems [3], which is also studied to non-invasively diagnose the internal temperature [4] and the state of health [5] of the battery. Its integration within BMS is thus a major issue to improve the management of batteries. Various solutions are proposed for this integration, like using an electrical charger [6], or the power converter of the device [7], or the motor control [8] or more specific electronics [9]. Taking into account the constraints of cost and simplicity required in the intended applications, we propose to use the existing electronics of current control and we study the conditions for the integration of a frequency evolutionary estimation of the electrochemical impedance [10]. Therefore the goal of this study is to evaluate the effect of the electronics design on the performance of this estimator. All this work is conducted through representative simulations of a lithium nickel manganese cobalt oxide (NMC) battery of 2.2 Ah capacity from Samsung.

2 Impedance estimation

The method proposed for the impedance estimation provides both an accurate estimate of the electrochemical impedance in the frequency area and a tracking of its temporal variations.

2.1 Wideband identification

The process is based on a wideband active approach, as a small quantity of current is added to the main polarization current imposed on the battery. The waveform of the current is chosen to enable an excitation of the system over a flat wide frequency band. Among the variety of broadband signals we selected the pseudo-random binary sequence (PRBS) because of its frequency wealth and ease of integration [11]. Such a square signal can indeed be imposed on the battery repeatedly through a simple control of the transistor already present in BMS and usually used for the balancing stage. Then the voltage response is measured, and after suppression of the open current voltage (OCV) of the battery, the estimation process identifies its frequency response. This identification method is based on Fourier transforms and a local averaging strategy.

If the battery behaves as a linear and time invariant (LTI) system, its electrical impedance Z(f) can be defined by the ratio given in Eq. (1) between the cross power spectral density (CPSD) $S_{ui}(f)$ between voltage and current, and the power spectral density (PSD) $S_{ii}(f)$ of the current [12].

$$Z(f) = \frac{S_{ui}(f)}{S_{ii}(f)} \text{ if } S_{ii}(f) \neq 0 \quad (1)$$

We first estimate the two PSD $S_{ii}(f)$, $S_{uu}(f)$ and the CPSD $S_{ui}(f)$. The data are divided into blocks of same length by using a time window, and their discrete Fourier transform (DFT) is computed by using the fast Fourier transform algorithm.

2.2 Strategies of tracking

After an initialization step, the impedance is continuously updated using new blocks of data thanks to a recursive equation. Two strategies of averaging are considered. Both provide a fine tracking of the temporal evolution of the impedance, and the same quality of averaging if we equalize the equivalent noise bands of the two methods.

2.2.1 Sliding widow averaging

Data are averaged on N blocks sliding over the temporal signals. The estimator (Eq.2) is given by the CPSD for the k^{th} block.

$$\hat{S}_{ui_k}(f) = \frac{1}{N}\sum_{n=k-N+1}^{k} \hat{P}_{ui_n}(f) \quad (2)$$

A recursive version of this average relation as defined in Eq.3 allows a tracking of the impedance evolution with time (or block of data).

$$\hat{S}_{ui_k}(f) = \hat{S}_{ui_{k-1}}(f) + \frac{\hat{P}_{ui_k}(f) - \hat{P}_{ui_{k-N}}(f)}{N} \quad (3)$$

The first result of impedance estimation is provided after the processing of N blocks of measurement, and following estimation updates are available at the end of each new block of data. The equivalent band noise of the sliding window approach is equal to 1/N.

2.2.2 Exponential averaging

This second approach involves a forgetting factor (a) whose value controls a trade-off between the convergence time and the final estimation error. Eq. (4) gives the algorithm necessary to recursively estimate the CPSD $S_{ui}(f)$. Finally the battery impedance is estimated by the ratio of the estimated CPSD and PSD.

$$\hat{S}_{ui_{-1}} = 0$$
$$\hat{P}_{ui_k}(f) = A * U_k(f) I_k^*(f)$$
$$\hat{S}_{ui_k}(f) = a\hat{S}_{ui_{k-1}}(f) + (1-a)\hat{P}_{ui_k}(f) \quad (4)$$

where A is a normalization factor, * denotes complex conjugation, $U_k(f)$ ($I_k(f)$ respectively) is the DFT of the k^{th} block of voltage (current respectively), $Pui_k(f)$ is the cross-periodogram of the k^{th} block of voltage and current samples, and $a \in [0;1]$ is the forgetting factor. The equalization of the equivalent noise bands of the two approaches described in this paper is done by linking the forgetting factor (a) to the number of blocks (N) through Eq.5:

$$a = \frac{N-1}{N+1} \quad (5)$$

3 Design methodology

The methodology proposed to design the BMS components is described in Fig.1. It consists in the selection of the main algorithm and electronics parameters in function of the requirement for the estimation of the impedance (i.e. frequency band of interest, frequency resolution of the complex impedance, accuracy of the estimate, output refresh rate, time response or convergence delay).

3.1 Choice of tracking strategy

Tables 1 and 2 list selected key parameters of the tracking algorithm. Some are related to tracking performances (as convergence time for the first impedance estimation, update delay for the next impedance values) and others to electronics design (as memory size and number of elementary operations involved in calculating an estimate).

Table1: key parameters of tracking algorithm based on a sliding window averaging

Memory size	N blocks
Convergence time to R%	$N\frac{R}{100} - 1$
Update delay	1 block
Noise band equivalent	1/N
Number of operations	N*N_FFT additions N_FFT/2 multiplications

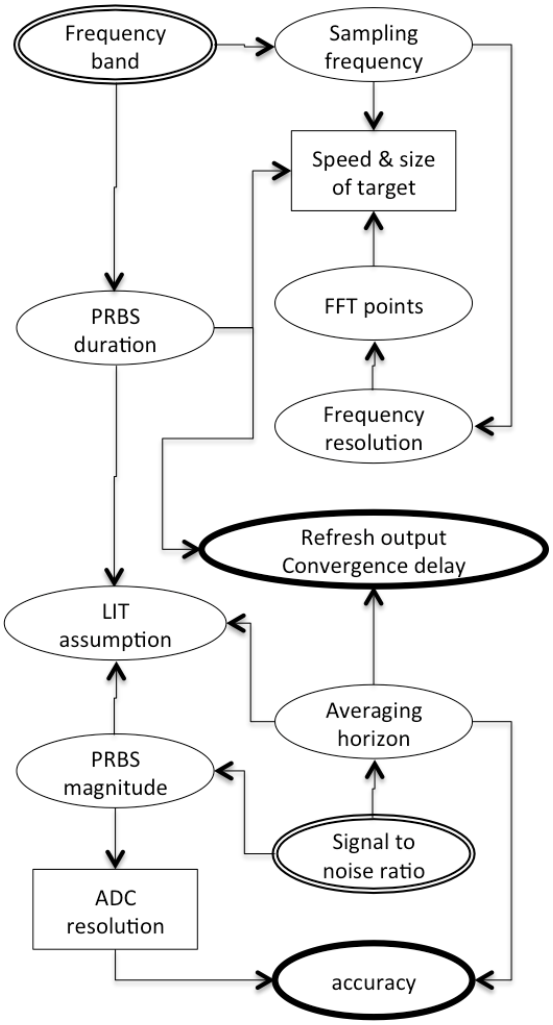

Figure1: Design methodology (double line: input, thick line: output, square: electronics parameters)

Table2: key parameters of tracking algorithm based on an exponential averaging

Memory size	2 blocks
Convergence time to R%	$\left(ln(1-R/100)/ln\left(\frac{N-1}{N+2}\right)\right) - 1$
Update delay	1 block
Noise band equivalent	(1-a)/(1+a)
Number of operations	2*N_FFT additions 4*N_FFT multiplications

The update delays of both averaging strategies are the same as a recursive implementation is chosen.

In regards to the time required to provide the first estimate, a sliding window filtering is more interesting than an exponential averaging as the convergence time is lower. For example, as shown in Fig.2, the convergence time to 95 % of the final value of a sliding window filtering with N = 100

blocks is less than 100 s, whereas it reaches 150 s for the exponential approach on the same average conditions (i.e. a = 0,98). Thus, if the application requires just an estimate on request from time to time, this strategy can be effective to provide a fast response.

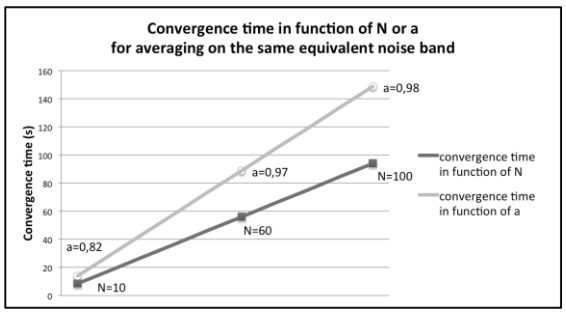

Figure2: convergence time to R=95 % of the final value in function of the number of blocks (N) of the sliding window approach or the forgetting factor (a) of the exponential approach for an averaging on a same equivalent noise band

Depending on the target, especially if a microcontroller is used, real and imaginary parts of complex variables are considered separately. The main steps of the algorithm are the centering of the measurement blocks and the computing of the DFT. This requires on the whole a small number of operations for both approaches that can be completely carried out by a target such as a microcontroller, if the frequency band and the tracking rate are not too high.

Finally, the main advantage of the exponential averaging tracking is to limit the amount of data required for the estimation. Indeed only few blocks of data (current, voltage and intermediate quantities) need to be stored in the embedded memory as this recursive approach requires only the last block of the cross-periodogram and the previous block of the CPSD. The memory size is thus drastically reduced. Despite a delay in the convergence time of the algorithm for the first estimate, an exponential averaging is therefore preferred for the integration of the tracking algorithm on electronics, especially if the frequency band of interest for the determination of the electrochemical impedance is high (as higher sampling rate leads to higher number of points to process).

3.2 Key parameters of the design

The approach for fine electronics specifications consists in the evaluation of the effects of some key parameters of the design on the error between a known impedance and an estimated impedance. To represent a simplified electrical behaviour of the battery, a model with constant thermal condition based on an electrical equivalent circuit is used, with a known impedance ($Z_{ref}(f)$). A polarization current with a predefined PRBS is applied at the input of the model, and the voltage output is evaluated. This two simulated signals are used as inputs for the frequency identification method to provide the estimated impedance ($Z_k(f)$). Design parameters (see Table 3) are applied to the process and modify the quality of the estimate. For example, measurement noises are considered as realizations of an additive centered Gaussian white noise on current and voltage, and the effect of the digitalization is modeled by a quantization of the measurements and a uniform noise whose power spectral density depends on the quantization step.

Table3: list of the key parameters and values used for the simulations

Measurement noises on current & voltage	Signal to noise ratio [25;18;10;4] dB
ADC parameters for the quantization of current & voltage	Number of bits [8;10;12;14;16;18;20; 22;24]
Sampling frequency for a PRBS addressing a frequency band with an upper frequency Fmax	[2;5;10;15;20;25] *Fmax
OCV compensation	Either with a constant voltage
Or with a linear model of the voltage with time	
DFT parameters	[128;256;512; 1024;2048]

For each simulation, only one parameter varies while others are fixed to their best value. We quantify and compare the effect of each parameter through a relative error on the impedance (Eq. 6), defined in the frequency domain as the root mean squared error expressed as a percentage, averaged over the entire frequency band, and taken for the block k just after the convergence time which is driven by the forgetting factor involved in Eq. 4.

$$\boldsymbol{RMSE_k = 100\sqrt{\frac{\int_{f\in B}|Z_{ref}(f)-\hat{Z}_k(f)|^2 df}{\int_{f\in B}|Z_{ref}(f)|^2 df}}} \quad (6)$$

4 Design results

4.1 Sensibility to design parameters

Errors on impedance due to the effects of the design parameters stay globally low, which means that the estimated impedance is rather close to the known impedance. Nevertheless, the solution varies more or less around the true value. As en example, Fig.3 (resp. Fig.4) presents the effect on the Nyquist plot of the estimated impedance of the number of bits of the digitization of the signals (resp. the number of DFT points). Assuming no aliasing (low pass filtering) and that the input dynamic of the digitizer is adapted to the variation of voltage to acquire, at least 10 bits (resp. 12 bits) of quantization could provide an error inferior to 1 % (resp. 0.1 %) on the impedance.

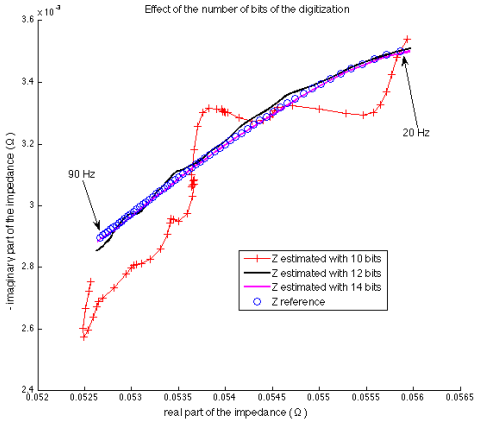

Figure3: effect on the Nyquist plot of the estimated impedance of the number of bits of the digitization

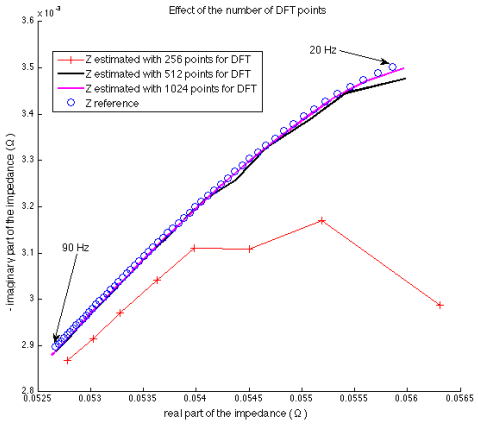

Figure4: effect on the Nyquist plot of the estimated impedance of the number of DFT points

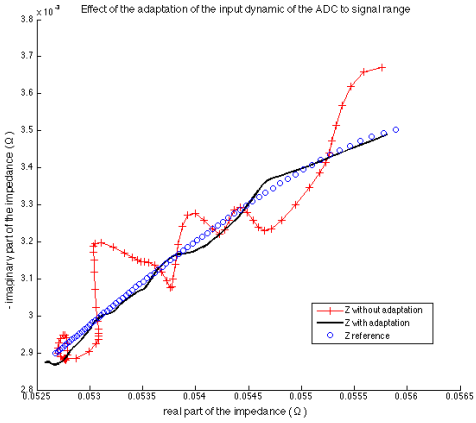

Figure5: effect on the Nyquist plot of the estimated impedance of the adaptation (or not) of the input dynamic of the ADC to signal range

This specification corresponds to more efficient converters than those typically used in BMS dedicated to the monitoring of the voltage of cells, but remains accessible. If the dynamic of the analog-to-digital converter is not adapted (as illustrated on Fig.5) to the signal range, especially the voltage extend, at least two more bits are required for a given accuracy, depending on the voltage level and the range of the converter. It is therefore essential to add an analog stage for the adaptation, even roughly, of the input dynamic.

Similarly, errors due to the choice of the number of DFT points indicate that 512 points is enough to deliver a good accuracy ($RMSE_k$ < 0.1 %). This quantity limits the amount of memory for the tracking, and the required computational time, with respect to the choice of the rate of sampling. Basic targets, like low power and low cost microcontrollers, could thus be considered if the frequency band of interest and resolution stay limited.

The analysis of other results shows that the frequency sampling can be reduced, as long as the Nyquist criterion is observed. OCV compensation can be limited to the subtraction of a constant (like the mean of the voltage input) with no degradation on the impedance estimate. This compensation is therefore reduced to a low complexity stage. Such an operation is sufficient as long as the duration of a block of measurements remains short in regards to OCV variations (typically a few seconds). For longer duration, finer OCV compensation implies fitting the low frequency variations of the voltage with a higher-order function (as a polynomial).

4.2 Filtering setting

The forgetting factor adjusts the noise filtering level on the estimation. That is what Fig.6 illustrates, as errors on the estimate increase with the level of noise for a given forgetting factor, and decrease as the forgetting factor tends to 1 for a given signal to noise ratio, especially as the noise level is high and requires a great filtering.

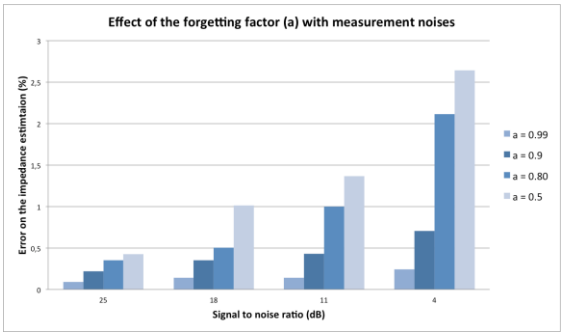

Figure6: effect of the forgetting factor on error $RMSE_k$ on the estimated impedance for noisy input signals

But a compromise needs to be found between a strong averaging (corresponding to a close to 1), meaning that past events strongly affect the current estimate, and a short convergence delay with high capabilities of tracking (corresponding to a close to 0) but with more noise sensitivity.

5 Application on a microcontroller

Finally, these design considerations have been applied to define a prototyping environment for a BMS including the impedance tracker described previously. We have chosen a microcontroller unit from the 32 bits ARM family [13] with a flash memory of 32 Mo, analog-to-digital converters and a CAN communication interface.

Our simulation and design tools allowed us to ascertain that the key parameters settings are suited to both provide a correct tracking of the impedance measurement (error near 0,3 % for a band of interest covering 20 to 90 Hz, with a tracking rate of 250 ms) and fulfil the timing constraints driven by the frequency band in which the impedance is estimated. All calculations are done while a new block of data is acquired, that is to say in less than 250 ms. Indeed table 4 gives the main results obtained on the prototype, for the timings of each task (a parallel execution is used through real time operating system), the frequency resolution provided in the frequency band of interest, and the size of the memory dedicated only to variables used by the tracker algorithm.

Table4: results of the integration of the impedance tracker on a BMS platform

Sampling frequency	500 Hz
Number of points used for DFT (Radix-2)	512 points
Frequency resolution of the impedance estimate	1 Hz
Computation time of each DFT	62 ms
Computation time of each impedance estimate	135 ms
Delay time of CAN transmission	20 ms
Memory size (RAM)	16 ko

6 Discussion

The design methodology proposed is powerful to fit the key parameters of both algorithm and electronics to the main requirement of the impedance estimator, whether the output refresh rate or the convergence time or the frequency resolution. Some complementary information can also be added to focus on a more specific requirement. For example, the determination of the complex impedance value at a specific frequency or on a particular point in the Nyquist plot (like the point where the imaginary part of the impedance is null) can primarily constrain the design. Moreover, if the electronics is not combined with an external power supply, i.e. the battery under test supplies BMS components itself, an additional requirement on the consumption related to the process can limit the duration of the impedance tracker algorithm.

7 Conclusions

In conclusion, we have developed a methodology to design the key parameters of electronics dedicated to the impedance tracking of a battery, in function of the frequency band of interest and the desired accuracy. We highlighted that electronics of conventional BMS can host this tracking algorithm, with converters of 10 bits or more, having an analog stage to adapt their dynamics, and that microcontrollers can be enough powerful to perform calculations, both in terms of number of operations and speed of execution. This methodology will soon be applied for electronics

design in the European collaborative project 3Ccar funded by the ECSEL Joint Undertaking.

Acknowledgments

This project was supported by the French ANR via Carnot funding.

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