

N2S3, a Simulator for the Architecture Exploration of Neuromorphic Accelerators

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1 Introduction

With the end in sight for Moore's law and the end of Dennard's scaling, the computing community has to find radically new computing architectures to fulfill the needs of Big Data and Cloud Computing [1] while dealing with the energy consumption limits.

It is well recognized now that artificial neural networks are such a promising architecture. The project we are involved in, in an interdisciplinary cooperation with teams from computer vision and from nanoelectronics, is to study the suitability of memristors to build a neuromorphic accelerator for computer vision.

2 Memristors as synapses for artificial spiking neural networks

The synapses, the interconnections between neurons, are an essential component of spiking neural networks that present at the same time the role of memory (by storing the weights) and the site of computation. The nanoelectronic community has discovered the way to build memristive devices and has shown that their physical behavior can mimic very efficiently the behavior of the synapses in the brain. In this work, with the latest proposals to use memristive nano-devices as synapses, we are going to implement efficient unsupervised learning rules like Spike Timing Dependent Plasticity (STDP). The idea is to use Leaky Integrate and Fire (LIF) neurons in different topologies of networks (Restricted Boltzmann Machine, Winner-take-all, ...) to make a neuromorphic accelerator suitable for

approximated and cognitive computing. We have identified the key requirements of an architecture exploration framework for a memristor based neuromorphic accelerator. The framework should provide a mean to explore the topology of the network (layered structure as in deep learning or cyclic connections as in reservoir computing, configurability of the topology), the information coding schemes, the learning methodology, and the suitability of the various memristive devices. The unique properties in memristor nano-devices such as, extreme scalability, flexibility, and ability to remember the last state make the memristor a very promising candidate to apply as a synapse in neuromorphic hardware platforms. Thanks to close collaborating with IEMN (nano-electronics in the University of Lille) we propose to study the suitability of different kinds of memristors (TiO_2 , NOMFET, magnetoresistive, magnetoelectric) to build a spiking neural network accelerator. Due to the already demonstrated suitability of NOMFET [2] to play the role of a synapse, we will use it as our first model.

3 N2S3 (Neural Network Scalable Spiking Simulator)

The most popular neural network simulators in neuroscience community such as Neuron, Brian or NEST can provide different levels of abstraction [3]. However, they are clock-driven and the model of memristor as a synapse is not considered. Xnet [3] is an event-driven simulator but its capabilities do not address some of our requirements such as scalability and concurrency. Furthermore, Xnet is not available to us.

The main requirements we have concerning our

simulator are: scalability to allow the simulation of large networks, and flexibility to allow the modeling of various memristive devices and circuit architectures. These requirements have imposed several design decisions:

- We will use an event-based simulation using the AER representation for efficiency and for compatibility with the existing jAER software project [4].
- We will use analytical models. Indeed, solving differential equations is too costly for large scale simulations.
- The programming language should allow a simple expression of extensibility, thus an object oriented language.
- The architecture of the network is based on the actor model. This fits well the domain (one actor per neuron or synapse, using messages to communicate spikes) and allows a full expression of the concurrency available in the circuit.
- The synchronizations will be adaptable, from a single priority queue to guaranty the fidelity of the simulation to no synchronization at all for a fully concurrent simulation, and many possible intermediate synchronization schemes.

These design choices have lead to the current implementation based on the Scala programming language [5] and the Akka actor library [6].

Event-based simulation allows the system to respect the low activity density of spiking neural networks therefore to consume low energy. Regarding to properties of SpiNNaker [7] architecture such as concurrency and event driven parallel architecture, we believe that after some modifications of N2S3 it could be a suitable candidate to run on SpiNNaker machine.

We will show on the final presentation or poster the first results we will have using the N2S3 simulator on classical examples such as the recognition of handwritten digits using the MNIST database.

References

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