



HAL
open science

Optimization of a MOS–IGBT–SCR ESD protection component in smart power SOI technology

Houssam Arbess, Marise Bafleur, David Trémouilles, Moustafa Zerarka

► To cite this version:

Houssam Arbess, Marise Bafleur, David Trémouilles, Moustafa Zerarka. Optimization of a MOS–IGBT–SCR ESD protection component in smart power SOI technology. *Microelectronics Reliability*, 2015, 55 (9-10), pp.1476-1480. 10.1016/j.microrel.2015.06.138 . hal-01238569

HAL Id: hal-01238569

<https://hal.science/hal-01238569>

Submitted on 5 Dec 2015

HAL is a multi-disciplinary open access archive for the deposit and dissemination of scientific research documents, whether they are published or not. The documents may come from teaching and research institutions in France or abroad, or from public or private research centers.

L'archive ouverte pluridisciplinaire **HAL**, est destinée au dépôt et à la diffusion de documents scientifiques de niveau recherche, publiés ou non, émanant des établissements d'enseignement et de recherche français ou étrangers, des laboratoires publics ou privés.

Optimization of a MOS-IGBT-SCR ESD protection component in smart power SOI technology

H. Arbess^{a,c}, M. Bafleur^{a,b}, D. Trémouilles^{a,b}, M. Zerarka^{a,b}

^aLAAS - CNRS, 7 avenue du colonel Roche, F-31400 Toulouse, France

^bUniv de Toulouse, LAAS, F-31400 Toulouse, France

^cUniversity of Bordeaux, Bordeaux Institute of Technology, IMS Laboratory
CNRS UMR 5218, F-33400, Talence, France

Abstract : A MOS-IGBT-SCR component that was proposed in a previous paper to increase the device robustness and the cost of ESD protection circuit is optimized in this paper. In order to improve its latch up immunity, several variations of geometrical parameters that have been simulated using TCAD Sentaurus Device in another previous paper have been implemented and compared in this paper. The drift area, the form factor, and the proportion of P⁺ sections inserted into the drain are the main parameters, which have a significant impact on the latch up immunity. TLP characterization, and curve tracer measurements have been carried out to evaluate the proposed solution. Holding current increases up to 70 mA and holding voltage up to 10 V.

1 Introduction

The electrostatic discharge (ESD) has always been one of the highest reliability concerns in the integrated (IC) manufacturing industry. With the continuous miniaturization process, the integrated circuits become more and more vulnerable to ESD. The miniaturization of the ESD protection blocks is one of the greatest challenges of smart power technologies. Silicon On Insulator (SOI) technologies allow extending the operational temperature range while providing the necessary isolation between components with a reduced silicon area.

SOI technology is becoming more and more attractive to manage very high voltage blocks, to reduce parasitic NPN effect and to increase Integrated Circuit (IC) speed as well as for applications operating at high temperature [1], [2].

Electro Static Discharge (ESD) protections occupy a significant silicon IC area. Using a LDMOS as main ESD protection component is not optimal due to its high on-resistance, but it could be the only solution for some technologies.

In a previous work, we proposed a new ESD component (MOS-IGBT-SCR) and improved it in order to increase ESD performance and improve the latch up immunity [3] [4]. ESD performance was excellent but margin to prevent latch up was not satisfying. In this paper, an optimized version of this structure is discussed and experimentally validated.

As the technological parameters of the used technology (TFSMART1: SOI smart power technology) cannot be changed, we explored various layout-design solutions such as the device topology or the architecture.

2 Structure description and preview solution

The chosen technology is a smart power SOI one (TFSMART 1) provided by Telefunken Semiconductors [5]. This technology parameters are detailed in [3].

The device under study is a MOS-IGBT-SCR component. It is built by implementing, within the structure of the N-LDMOS, a lateral IGBT formed by inserting in the drain region both N⁺ and P⁺ diffusions (Fig. 1). The initial NLD MOS is composed of two 150 μm-width fingers with central drain diffusion, the body being connected to the source. Three silicon runs have been realized in order to optimize the MOS-IGBT-SCR structure. The principal problem of this device is the control of the SCR triggering [6]–[9]. Results of the first two runs are discussed in [3], [4].

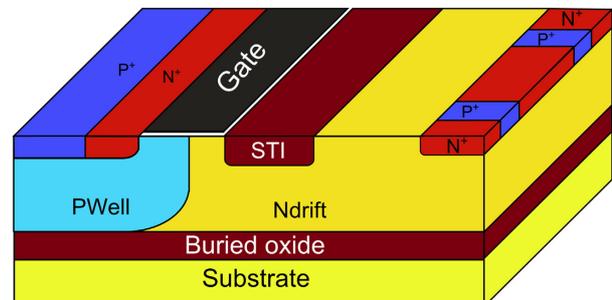


Fig. 1: Mixed structure MOS-IGBT-SCR

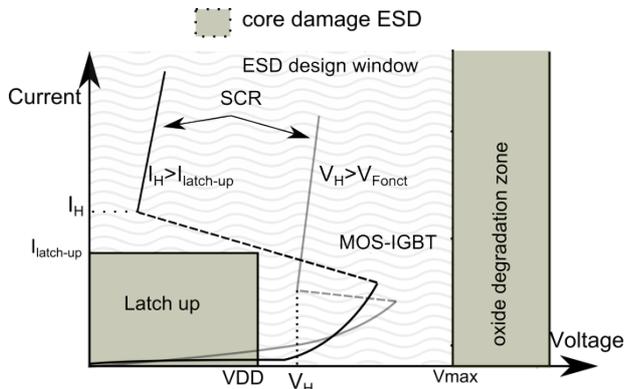


Fig. 2: I-V characteristics of SCR as ESD protection component. This schematic shows the safe operating area of the SCR and the danger zone.

In a previous work [4], we proposed and studied several layout variations (different P^+ diffusion proportions in the drain, different configurations of the IGBT section in the drain and the reduction of the channel width). They resulted in a clear but insufficient experimental improvement of the holding current and voltage after triggering. Indeed, the minimum holding current of the SCR to avoid any latch up is equal to 100 mA [8] (Fig. 2). The highest obtained holding current was equal to 50 mA. The holding voltage was also very low (< 3 V).

3 Proposed new solutions and results

To assess the ESD behavior and robustness of the proposed structures, TLP measurements were carried out at wafer level on a Celestron TLP (50Ω) test bench. A calibration is performed before starting the measurement to eliminate the series resistances due to setup wire connections. TLP pulses have 100 ns duration and a rise time of 1 ns. To evaluate the holding current and holding voltage level, curve tracer has been used on tens of components. Three or four components have been tested for each configuration. The three chosen configurations in this study are the 1P2N (33 % IGBT), 1P4N (20 % IGBT) and 3P1N (75 % IGBT). This choice can be explained by the fact that the obtained results in the previous silicon run exhibited the maximum and the minimum holding current for the 1P4N and 3P1N respectively, and the best ESD performance for the 1P2N. The results confirmed that the effect of P^+ diffusion percentage in the drain, corresponding to the IGBT one, has the same effect as shown and explained in [4].

The new architectures were achieved using two distinct approaches. The first one is to increase the holding current so as it is greater than 100 mA. The second one is to increase the holding voltage so as it is

greater than the power supply of the block to be protected, here 5 V.

After carrying out TCAD simulations using Sentaurus Device and based on previous results obtained in [3], [4], [10], three major topological modifications have been applied in order to make this component latch-up compliant:

- A- Channel reduction
- B- Form factor
- C- N drift length

The variation of holding current, holding voltage and robustness for the different configurations are studied and discussed in the following sections.

3.1 Channel reduction

Due to the significant improvement obtained with a channel reduction of 20% [4] (implemented by replacing 20 % of the N^+ source diffusion by a P^+ one), we decided to explore the increase of this percentage up to 40% (Fig. 4).

The compared configurations are: without channel reduction, 20% channel reduction, 30% channel reduction and finally 40% channel reduction.

Using an analog curve tracer, the holding current and holding voltage values were measured. Indeed, the curve tracer apply a sinusoidal voltage on the device through a serial resistance: during the increasing part of the sinusoid, the device is triggered-on and on the decreasing one the holding current and voltage are revealed by the voltage increase while the current is decreasing (Fig. 3).

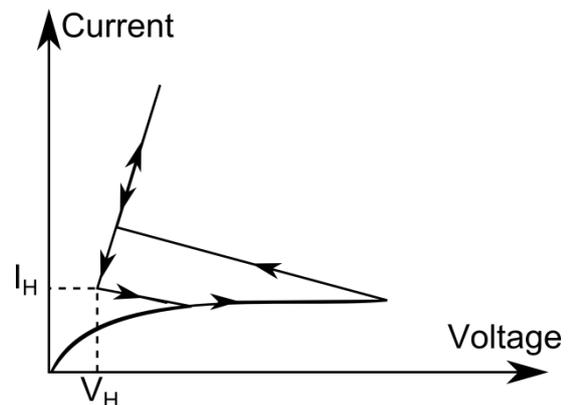


Fig. 3: Schematic presentation of electrical characterization using curve tracer showing the evolution of the characteristics

Fig. 5 shows the channel reduction impact on the characteristics of the MOS-IGBT-SCR structure 1P2N (33% IGBT) at room temperature and with $V_{GS} = 5$ V. In this figure the holding current increases from 32 mA up to 66 mA when the channel reduction varies from 0 up to 40%. Indeed the channel reduction topology helps

decrease the Pwell resistance and as a result, increases the holding current that is by definition, the current level under which the SCR turns off.

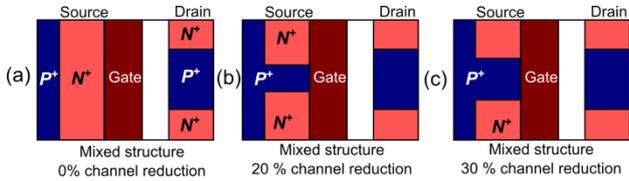


Fig. 4: Source side optimization of 1P1N (50 % IGBT) mixed structure (a), mixed structure with 20 % (b) and 30 % (c) channel reduction.

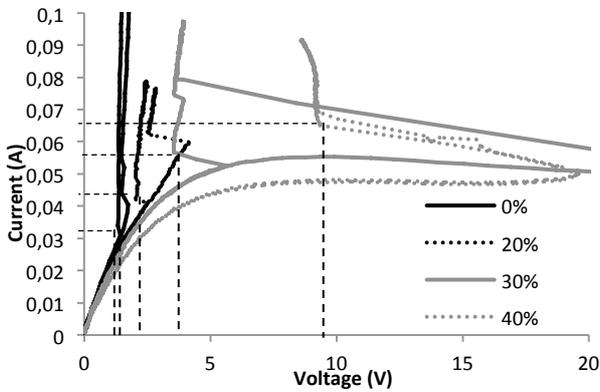


Fig. 5: Channel reduction effect to the holding current for the MOS-IGBT-SCR structure 1P2N (33 % IGBT) at room temperature and with $V_{GS} = 5V$.

The effect of this parameter variation on the holding voltage was also studied. Increasing the channel reduction from 0 % to 40 % induces an increase in the holding voltage from 1.5 V up to 9.5 V (Fig. 5). Indeed, the increase of the holding current makes the voltage drop greater for the same N drift resistance.

However, concurrently to its positive effect on the holding current and holding voltage, the channel reduction shows a negative effect on the device robustness (see Fig. 6). Indeed, the channel reduction lowers the SCR action since it tends to locally cancel the NPN bipolar transistor. This phenomenon increases the current focalization and results in a premature failure. However, for the structure 3P1N (75 % IGBT), this detrimental effect is much less important and the robustness decreases from 10.2 A down to 6.3 A (see Fig. 6) that corresponds to 9.7 kV HBM level.

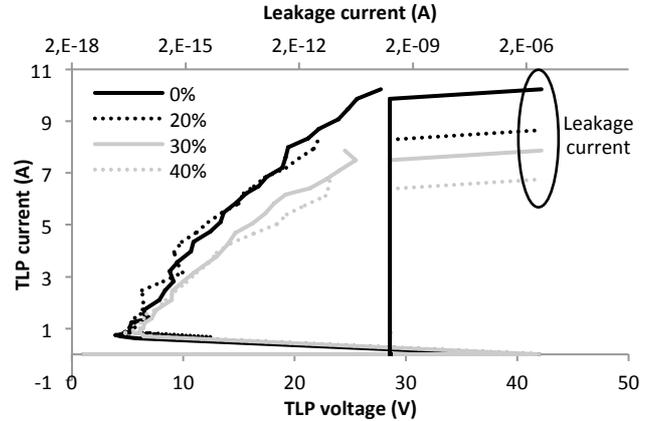


Fig. 6: Effect of channel reduction from 0 to 40 % to the TLP characteristics of the 3P1N (75% IGBT) structure.

3.2 Form factor

The second parameter that allows increasing the holding current, is the form factor. Indeed, in the case of long fingers, despite the gate biasing and the resulting homogenous current across the channel there is a high risk to have a current focalization upon the triggering of the SCR [11]. Therefore, the idea is to split the structure in two or three parallel ones in order to have the same total width as the initial one. Reducing the width of the fingers decreases the probability of current focalization. However, to guarantee homogeneous triggering of the structure, the access resistances to these parallel structures need to be carefully balanced. To assess the impact of this parameter, three configurations have been implemented. The initial one (init) is the initial structure width ($150\mu m * 2$ fingers), the second one is made up of two structures of $75\mu m$ in parallel (D2) (Fig. 7) and finally by putting three structures of $50\mu m$ in parallel. Fig. 8 shows the results of the three configurations for the structure 1P2N (33% IGBT) with channel reduction equal 30%, at room temperature and for $V_{GS} = 5V$. The holding current increases from 57 mA to 67 mA when the structure is divided in three parallel devices.

Fig. 9 shows the variation of the TLP characteristics versus the form factor. The robustness increases from 4 to 7.2 A when the initial single-finger structure is compared to the three-fingers one having the same total width. This result confirms undoubtedly that, there was a current focalization in the initial structure probably due to imbalanced parasitic resistances. As a result, the form factor can be used to partially compensate the robustness decrease induced by the channel reduction topology.

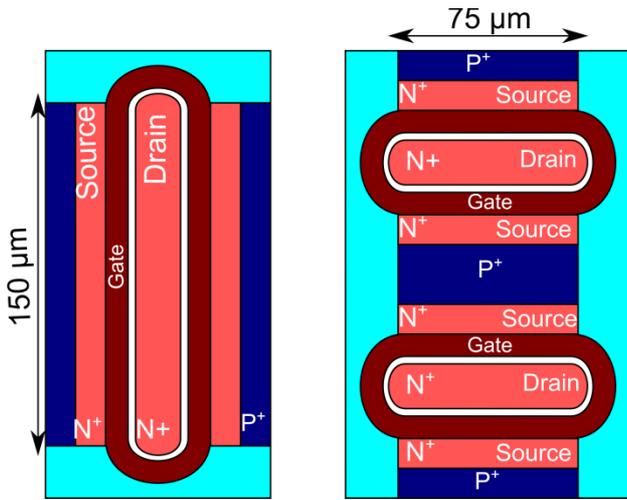


Fig. 7: Two components with the same total width (init) and different form factors (D2).

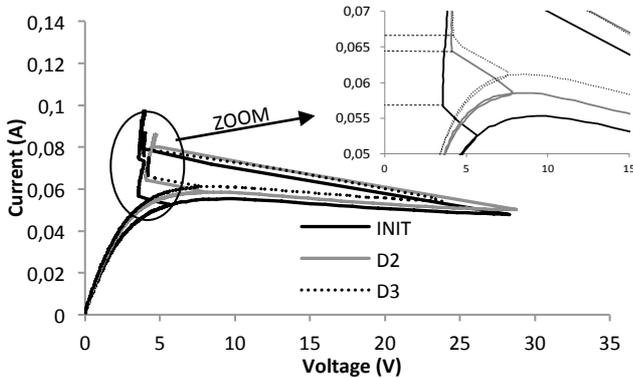


Fig. 8: Form factor effect on the holding current for the structure 1P2N with channel reduction equal to 30% at room temperature and for $V_{GS} = 5V$. (INIT, D2 and D3 present successively the structure with a single finger, two fingers in parallel and three fingers in parallel, all having the same total width.

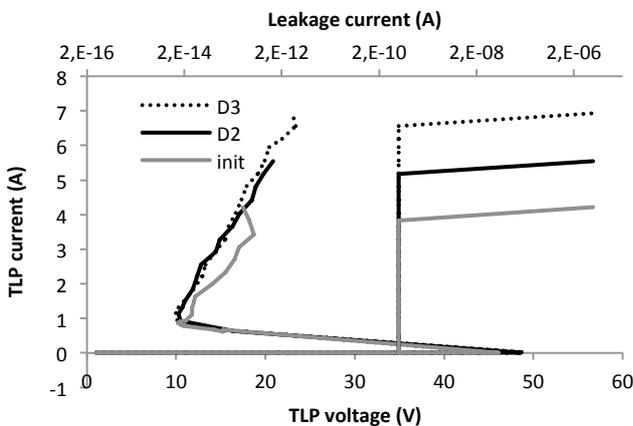


Fig. 9: Form factor effect on the ESD robustness for the structure 1P2N with channel reduction equal to 30% at room temperature

and for $V_{GS} = 0V$.

3.3 N drift length

The final parameter that allows optimizing this device is the N drift length. Therefore, increasing the N drift length would result in a higher voltage drop, for a given holding current. Three configurations have been designed in addition to the initial structure INIT (Ndrift width = 2 μm): P2, P4 and P6 (initial Ndrift length plus 2, plus 4 and plus 6 μm , respectively).

Table 1 shows the holding voltage and holding current using the curve tracer. It can be noticed that, these configurations have a non-linear variation effect on the holding voltage and holding current values. As shown on the TLP I-V characteristics of the 1P2N structure with a channel reduction of 30 %, presented in Fig. 11, the impact on the ESD robustness is very important. It increases from a value of the failure current I_{t2} of 4.5A for the initial structure up to almost 8 A for the structure P6. This confirms that, the increase of the N-drift improves the current homogeneity without degrading the on-resistance of the structure.

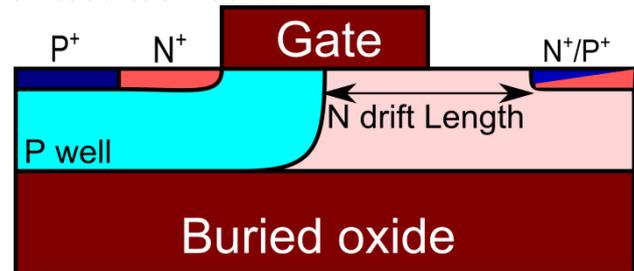


Fig. 10: Cross sectional view of MOS-SCR structure with presentation of the N drift length

According to these results, the best configuration to get the maximum holding current is to combine a large Ndrift length, a high channel reduction percentage and a form factor. Nevertheless, for cost efficiency, a trade-off has to be found between the induced silicon area increase and the targeted ESD robustness.

Table 1: Curve tracer measurement of the holding voltage and current of the structure 1P2N with channel reduction equal to 30% at room temperature, for $V_{GS} = 5V$ and different N drift lengths.

Configuration	INIT	P2	P4	P6
Holding voltage (V)	3.5	5.6	4.7	5.2
Holding current (mA)	56	60	70	70

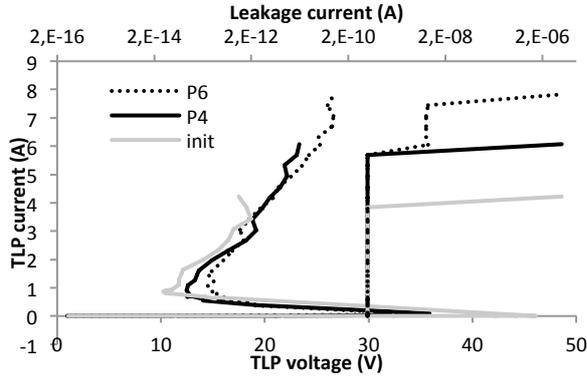


Fig. 11: TLP characteristics of the structure 1P2N with channel reduction equal to 30% at room temperature, for $V_{GS} = 0V$ and different N drift lengths.

4 Discussion

This component has been proposed as an ESD protection device in order to minimize the silicon footprint of this part in the integrated circuit. The highest holding current obtained in this work is equal to 70 mA. This value can be raised by increasing the component width. Indeed, for some configurations (1P4N with channel reduction higher than 30 %...), the component exhibits an early failure due to high power consumption (High I_H and high V_H). Therefore 150 μm width corresponds to a very small ESD protection component.

The highest holding current has been obtained with a biased gate. Therefore, a trigger circuit is needed to control this component. However, this circuit will be considered as a future work in order to have a complete power clamp.

5 Conclusion

We proposed further improvement for an innovative ESD protection structure presented in a previous work [4]. It is based on combining and properly controlling in a single structure a MOS, an IGBT and a SCR. This paper describes the optimization of these MOS-IGBT-SCR protection structures and their characterization.

Three new parameters (channel reduction percentage, form factor and drift zone length) were tested to study their influence on the holding current, holding voltage and the ESD robustness of the mixed component (Table 2).

With this layout optimization, the greatest measured holding current is smaller than 75 mA but this structure can be safely used to protect components working at 5V according to the obtained holding voltage that is greater than 5 V even if its holding current is lower than 100 mA.

Table 2: Summary of geometrical parameters effects on the holding current, holding voltage and robustness of the mixed structures

	Increase of channel reduction	Form factor decreasing	Increase of N drift length
Holding current	Higher	Higher	Higher
Holding voltage	Higher	---	---
Robustness	Lower	Higher	Higher

REFERENCES

- [1] G. Celler, « What is SOI? Do we really need it? ». MIGAS 2004, 2004.
- [2] F. Udrea, D. Garner, K. Sheng, A. Popescu, H. T. Lim, and V. I. Milne, « SOI power devices », *Electron. Commun. Eng. J.*, vol. 12, n° 1, p. 27-40, Feb. 2000.
- [3] H. Arbess, D. Tremouilles, and M. Bafleur, « High-temperature operation MOS-IGBT power clamp for improved ESD protection in smart power SOI technology », in *Electrical Overstress/Electrostatic Discharge Symposium (EOS/ESD), 2011*, p. 1–8.
- [4] H. Arbess, M. Bafleur, D. Tremouilles, and M. Zerarka, « Combined MOS-IGBT-SCR Structure for a Compact High-Robustness ESD Power Clamp in Smart Power SOI Technology », *IEEE Trans. Device Mater. Reliab.*, vol. 14, n° 1, p. 432-440, March 2014.
- [5] « SMARTIS 1, Design Manuel, Release: SIS1_0.32_071005, Atmel Germany Gmhb, October 7 2005 ». [on line]. Available on: <http://www.telefukensemi.com>.
- [6] V. Vashchenko, N. Olson, D. Farrenkopf, V. Kuznetsov, P. Hopper, and E. Rosenbaum, « Mixed device-circuit solution for ESD protection of high-voltage fast pins », in *Reliability Physics Symposium, 2007. proceedings. 45th annual. IEEE international, 2007*, p. 602–603.
- [7] V. A. Vashchenko, A. Concannon, M. ter Beek, and P. Hopper, « High holding voltage cascoded LVTSCR structures for 5.5-V tolerant ESD protection clamps », *IEEE Trans. Device Mater. Reliab.*, vol. 4, n° 2, p. 273-280, June 2004.
- [8] M. P. J. Mergens, C. C. Russ, K. G. Verhaege, J. Armer, P. C. Jozwiak, and R. Mohn, « High holding current SCRs (HHI-SCR) for ESD protection and latch-up immune IC operation », *Microelectron. Reliab.*, vol. 43, n° 7, p. 993-1000, July. 2003.
- [9] Y. Li, J. Li, and R. Gauthier, « Junction engineering for SOI SCR triggering and performance improvement », in *Electrical Overstress/Electrostatic Discharge Symposium*

(EOS/ESD), 2014, p. 1-8.

- [10] H. Arbess, « Structures MOS-IGBT sur technologie SOI en vue de l'amélioration des performances à haute température de composants de puissance et de protections ESD », Ph.D. thesis, Université Paul Sabatier - Toulouse III, 2012.
- [11] D. Pogany, D. Johnsson, S. Bychikhin, K. Esmark, P. Rodin, E. Gornik, M. Stecher, and H. Gossner, « Nonlinear dynamics approach in modeling of the on-state-spreading - related voltage and current transients in 90nm CMOS silicon controlled rectifiers », in *Electron Devices Meeting (IEDM), 2009 IEEE International*, 2009, p. 1-4.