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Correlation between transient evolutions of the gate and drain currents in AlGaN/GaN technologies

O. Lazăr^a, J.G. Tartarin^a*, B. Lambert^b, C. Moreau^c, J.L. Roux^d

^a *CNRS-LAAS (UPS), 7avenue du Colonel Roche, 31031, Toulouse, France*

^b *UMS, 91140 Villebon-sur-Yvette, France*

^c *DGA-MI, 35998 Rennes Armées, France*

^d *CNES, 31400 Toulouse, France*

Abstract

This work focuses on short term and long term time evolution of charges in the context of early identification of failure mechanisms in AlGaN/GaN High Electron Mobility Transistors (HEMTs). High power and high frequency devices are needed for new microwave applications, and large band-gap HEMTs offer a powerful alternative to traditional technologies (Si, GaAs, SiGe etc.); however, reliability issues still hamper the potential of these technologies to push their limits in terms of mean time to failure or junction temperature. This paper contributes to the investigation of transient behaviours of gate and drain currents over a large time scale for gallium nitride HEMTs; a correlation is found between the currents' evolution, in spite of the non-monotonic behaviour, and a model is given through a mathematical relationship. Charges under the gated zone of the transistor are found to evolve with time, and turn into command variations of the electron density in the 2DEG. This work addresses the consequences of charge dependent mechanisms on the drain current's drop, and thus of the output power.

Corresponding author.

tartarin@laas.fr

Tel: +33 (056) 133 7996; Fax: +33 (056) 133 6969

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1. Introduction

Microwave field has already seized the outstanding performances that new large band-gap materials, like gallium nitride (GaN) technology, can offer. Army and space industries find a great interest in developing this type of technology, which is able to propose solutions for high power, high frequency, robust electronic modules working under harsh environment, with overall lower DC consumption and higher power added efficiencies, in reduced sized packages.

AlGaN/GaN HEMT devices are sized to withstand high voltage and high current density at high temperatures when used in power amplifiers. Still, reliability is not totally mastered yet because of the complexity of electro-thermo-mechanical mechanisms which hardens a deterministic analysis of degradation phenomena. Hence, a complete characterization of this kind of device can only be achieved by using several cross-experiments, or by using destructive techniques in order to evidence the presence of defects. Even though destructive techniques provide information on the tolerated tough limits, it definitely does not allow concluding about the real impact of a specific defect on the transistor's electrical behavior. In this approach, developments of non-invasive (and so non-destructive) experimental techniques have been proposed in order to access the electrical signatures of the devices.

This work is based on a correlation that has been found between transients of gate and drain currents, with non-monotonic behaviors. Different devices have been tested, featuring high, medium and low gate leakage currents (varying from one to two decades in terms of I_{GS} magnitude). Impact of the static leakage current level on the electrical transient signatures is evaluated in the next study. Short term and long term evolutions of I_{GS} and I_{DS} are highlighted for different biasing conditions (increasing/decreasing V_{GS}).

Most of the papers focus their reliability studies on the degradation of the carriers density, without considering a possible evolution of the gated zone under the Schottky contact, along the gate fingers (i.e. wherefrom the channel's control). In some cases, the reduction on I_{DSS} can only be attributed to the channel's degradation, whereas in other cases it is associated to a change in the intrinsic command of the gate: the Space Charge Region (SCR) evolves as a consequence of charges fluctuations with time. Therefore, the challenge is to determine what physical mechanism is underlying the gate and drain currents evolution (transient evolution of traps and/or charges).

Our approach proposes to investigate the impact of charges between gate-source and source-drain terminals (both impacting the command), namely the leakage current I_{GS} , as well as the output current I_{DS} . To this end, the paper is divided into four main sections: the first section briefly describes the selected samples, whereas the second part summarizes the proposed method. Results are presented in the third paragraph, and an interpretation is also provided, before drawing conclusions of this work.

2. Devices' characterisation

Devices under Test (DUTs) are issued from a process in its development phase manufactured by United Monolithic Semiconductors; AlGaN/GaN HEMTs feature 18% of Al content, are grown by MOCVD on SiC substrate and present 4 gate fingers (0.5 μm length and 400 μm width). The gate mushroom structure is a Schottky diode, formed by a stack of Ni/Pt/Au metals. For this study, virgin devices have been tested for assessing the transient correlation existing between the gate current (for different leakage levels) and the drain current. Next, 3 representative

* Corresponding author. tartarin@laas.fr
Tel: +33 (056) 133 7996 ; Fax: +33 (056) 133 6969

Table 1
Main electrical parameters for the proposed DUTs

Device ID	I_{GS} in open drain configuration @ $V_{GS} = -9$ V ($\mu\text{A}/\text{mm}$)	I_{GS} @ $V_{GS} = -9$ V & $V_{DS} = 8$ V ($\mu\text{A}/\text{mm}$)	I_{GS} @ $V_{GS} = 0$ V & $V_{DS} = 8$ V ($\mu\text{A}/\text{mm}$)	I_{DS} @ $V_{GS} = 0$ V & $V_{DS} = 8$ V (A/mm)	V_{GS} @ the gate current inversion point, V_{GS-inv} (V)
#NL	-11	-36	-0.05	0.37	1.98
#L _{medium}	-244	-223	-0.23	0.36	1.89
#L _{high}	-1230	-1700	-2.8	0.4	2.03

devices are used as an illustration of the study for low, medium and high static I_{GS} levels as described in Table 1. Two leaky devices are submitted to tests, next labelled #L_{medium} and #L_{high} (respectively for medium and high gate leakage currents), as well as one non-leaky device (#NL) in order to have a comparative study between samples at different DC gate current levels. Values of the gate leakage currents are specified in open drain configuration (ambient temperature and $V_{GS} = -9$ V), and at $V_{DS} = 8$ V for two different states of the two Dimension Electron Gas (2DEG): pinched channel when $V_{GS} = -9$ V, and open channel when $V_{GS} = 0$ V. Information on the drain current is also provided for $V_{GS} = 0$ V and $V_{DS} = 8$ V). All the tested samples feature almost the same gate current inversion point V_{GS-inv} (in transistor configuration).

In spite of the highest leakage current featured at $V_{DS} = 8$ V, #L_{high} presents also the higher drain current (0.4 A/mm), i.e. 10% above the other devices. The leakage current of #L_{high} is almost one decade above that of #L_{medium} and two decades above that of #NL, whatever the electrical biasing conditions. Fig. 1 presents the static plots of $I_{DS}(V_{GS})$ and $I_{GS}(V_{GS})$ in transistor mode for the 3 HEMTs under test.

Next, the levels of the DC leakage currents for #L_{high}, #L_{medium} and #NL are discussed in order to determine a possible impact of the leakage level on the

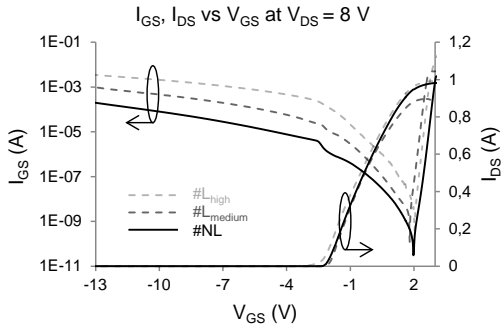


Fig. 1. Gate and drain currents versus V_{GS} for 3 DUTs: #L_{high}, #L_{medium} and #NL (at $V_{DS} = 8$ V).

electrical characteristics in the 2DEG (evolution of the electron density, thus evolution of I_{DS} and of the output power). It has already been proven the influence of charges localized above the channel (between gate and drain or between gate and source), or at the semiconductor interfaces and in the bulk [1], [2]; these charges can also be invoked for the increase in the gate leakage current under saturation biasing conditions [3]. Moreover, the presence of a higher amount of charges near the SCR could lead to a higher intrinsic V_{GS} , and could explain the 10% increase on I_{DS} for #L_{high} (associated with a slight shift on the threshold voltage).

Fig. 2 illustrates the gate and drain current evolutions for #L_{medium} here represented over a large

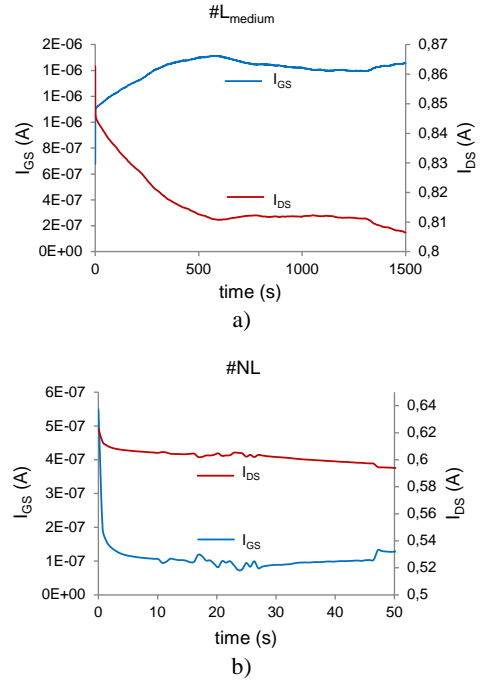


Fig. 2. Gate and drain current evolutions versus time: a) #L_{medium} at ($V_{GS} = 2.4$ V; $V_{DS} = 8$ V), over 1500 s, b) #NL at ($V_{GS} = 0$ V; $V_{DS} = 8$ V), over 50 s.

time scale (0 s – 1500 s), and for #NL given on a reduced time scale (0 s – 50 s) in order to have a better appreciation of several short term memory effects on I_{GS} and I_{DS} . From these two transient representations, it is obvious that a correlation exists between I_{GS} and I_{DS} for both 25 minutes experiment and for the rapid evolutions seen for #NL. It is then expected that these evolutions on gate and drain currents rise from the same electrical root cause.

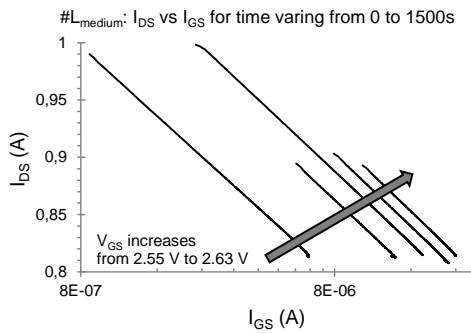


Fig. 3. Drain current versus gate current dependence at positive V_{GS} and $V_{DS} = 8$ V for # L_{medium} .

Next, characterizations have been performed under different biasing conditions (from open channel to pinch-off), for all devices from the batch. Fluctuations, although non-monotonic, still reveal identical trends for both I_{GS} and I_{DS} currents, as illustrated in Fig. 3. This behaviour is featured also for the other biases and means that the gate command affects simultaneously I_{DS} (i.e. the number of carriers in the 2DEG) and I_{GS} .

3. Model for time dependence correlation between gate and drain currents

Further, results on transient variations of gate and drain currents are more largely presented for # L_{medium} . Measurements are given for increasing gate biasing conditions: $2.55 \text{ V} < V_{GS} < 2.63 \text{ V}$ at $V_{DS} = 8 \text{ V}$ (Fig. 3). Hereinafter, analysis is carried out with the aim to determine the mathematical relationship existing between I_{GS} and I_{DS} . The representation in Fig. 3 leads to a logarithmical dependence law between instantaneous I_{DS} and I_{GS} currents (at instant i), over the entire period (0 s – 1500 s), according to equation (1):

$$I_{DS}(t_i) = a \cdot \ln(I_{GS}(t_i)) + b \quad (1)$$

Fig. 3 clearly evidences the presence of a time dependent process that affects both the drain and gate

currents. From an electrical point of view, this fact can be formalized as in Fig. 4, where I_{DS} and I_{GS} are represented versus V_{GS} . The dots represent the quiescent points of the DUT, whereas the sweeps on both sides of this quiescent point stand for time-dependent fluctuations. Then two main regions can be identified from this representation as follows:

- the zone before the gate current inversion V_{GS-inv} , associated to leakage mechanisms;
- the zone after the gate current inversion, where I_{GS} is modelled by the thermionic model.

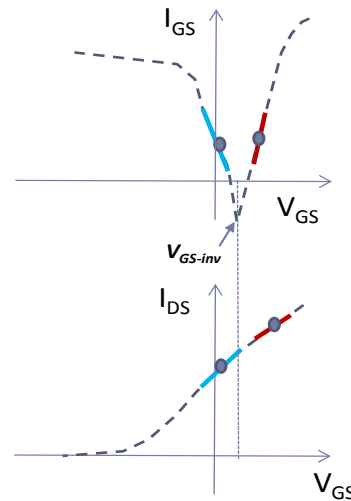


Fig. 4. Influence of the transient variations on the gate and drain currents, around the quiescent point (dot). The transistor is biased in the saturation region.

The next study is carried out for comparable I_{GS} levels for each device, but featuring different I_{DS} values, as stated in Fig. 4. Because the characteristics are considered in transistor configuration, the transconductance is different from zero for the two regions on both sides of V_{GS-inv} .

From the time domain variations (Fig. 2 a and b), it is clear that the evolution of the command with time affects simultaneously $I_{GS}(time)$ and $I_{DS}(time)$ according to the mathematical equation (1) and to Fig. 3. Then, this electrical transient effect can be attributed to variations of charges in the intrinsic region under the gate (at the interface of the piezo-electrical layers), as illustrated in Fig. 5. The effective voltage command $V_{GS-intrinsic}$ is directly affected by the transient evolution of the voltage generator $V_{charges}(time)$ under the gated zone of the device. From the suitable representation in Fig. 5, it is evident that charges evolution in this region is able to induce simultaneous variations on I_{GS} and I_{DS}

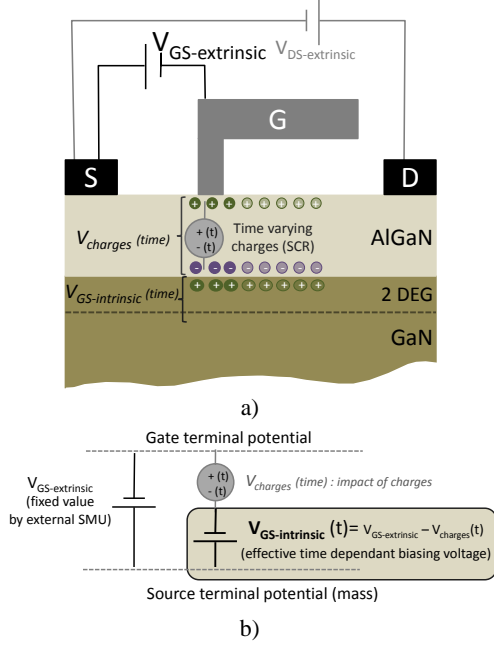


Fig. 5. Location of the active time-dependent charges under the gate (a), with its electrical representation $V_{charges}(time)$ generator: an intrinsic time-dependent voltage generator $V_{GS_intrinsic}$ (a and b) will induce a time dependence for I_{GS} and I_{DS} around the quiescent point.

around the quiescent point as depicted in Fig. 4. Because $I_{DS} = g_m \cdot V_{GS_intrinsic}$, the variations on the drain current are a direct consequence of time-dependent variations of the intrinsic gate voltage:

$$V_{GS_intrinsic}(time) = V_{GS_extrinsic} - V_{charges}(time). \quad (2)$$

Charges out of the controlled gated zone should not affect simultaneously I_{GS} and I_{DS} , and have no impact on transient measurements.

Prior to any data analysis, several measurements have been performed on each DUT at various moments, and for different voltage sweep conditions i.e. increasing/decreasing V_{GS} . Fig. 6 illustrates the variations of 'a' and 'b' coefficients from equation (1) versus this V_{GS} biasing procedure. Reproducible results are evidenced for 'a' coefficient, while 'b' parameter evolves depending on the increasing or decreasing V_{GS} sweep. Therefore, it can be established that 'a' is not sensitive to the initial state of the device, but is correlated only to its DC biasing quiescent point. As 'b' changes according to the previous electrical DC bias, this parameter is assumed to be affected by the initial conditions and cannot be interpreted as a reliable indicator associated to the concerned static V_{GS} . Next,

only 'a' is studied for each of the 3 DUTs.

Fluctuations on I_{GS} and I_{DS} are found to be reversible time-dependent processes, as different measurement campaigns that have been carried out still feature identical trends according to equation (1). Then, these time-dependent processes are not associated to permanent degradation state of the DUT. This behaviour is crucial when considering the device's stability in a circuit context. The lack of command stability in balanced-mixers, amplifiers or oscillators can result in unexpected performances of the circuit.

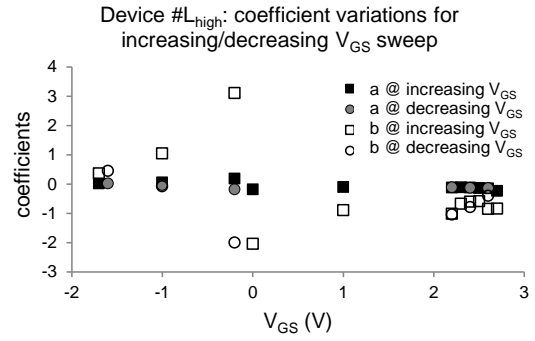


Fig. 6. Variations of 'a' and 'b' coefficients from equation (1) for increasing (square) or decreasing (bullet) V_{GS} DC bias. 'a' values are represented in filled markers and 'b' values are in unfilled markers.

Lastly, thermal transient effects are only sensitive during the first tenth of milliseconds after applying the bias, so interpretation of current fluctuations over the considered time range in this study are not attributed to thermal effects; moreover, as thermal effects do not significantly influence the gate current I_{GS} , the observed correlation between I_{DS} and I_{GS} would not occur under thermally activated transients on I_{DS} . Only electrical dependent processes are discussed next.

4. Interpretation

Several quiescent points have been investigated for the 3 DUTs. For each device and under both increasing/decreasing conditions, the logarithmical coefficient 'a' from equation (1) features a monotonic linear trend. All the tested devices reveal the same trend on the variation of 'a'-slope versus V_{GS} under increasing/decreasing sweep, for $V_{GS} > V_{GS_inv}$ (a wider voltage sweep for #NL and #L_{high}, from 2.2 V to 2.9 V, unlike #L_{medium} in Fig. 3).

An illustration of the behaviours for I_{GS} and I_{DS}

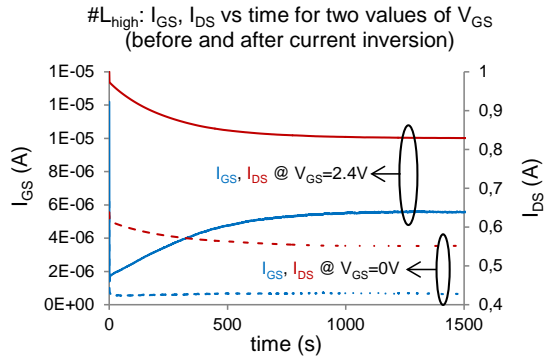


Fig. 7. Evolution of I_{GS} and I_{DS} for $\#L_{high}$ at $V_{GS} = 0$ V (dashed line) and at $V_{GS} = 2.4$ V (solid line). Representations of I_{GS} are given in blue and those of I_{DS} (at $V_{DS} = 8$ V) are given in red.

versus time is given in Fig. 7 at $V_{GS} = 2.4$ V (forward bias) and $V_{GS} = 0$ V (before the gate current inversion point) for $\#L_{high}$, both of them at $V_{DS} = 8$ V; this study is now carried out for comparable I_{GS} leakage levels for each device, but featuring different I_{DS} values. The subsequent relationships, as previously plotted in Fig. 3 for $\#L_{medium}$, result in linear trends of ‘ a ’-slope on both sides of the gate current inversion point, as exemplified in Fig. 8 and Fig. 9, respectively for $\#NL$ and $\#L_{high}$. From Fig. 8 ($\#NL$), the two trends of ‘ a ’-slope versus V_{GS} give an interception point at $V_{GS-inv} = 1.95$ V which corresponds to the inversion point of the gate current reported in Table 1. In a similar way, for lower values of V_{GS} (i.e. behind this inversion point, $0 \text{ V} \leq V_{GS} \leq 1$ V), $\#L_{high}$ reveals an interception at $V_{GS} = 1.9$ V. The value is still consistent with Table 1.

The interpretation of ‘ a ’-trend (slopes versus V_{GS}) is given as follows: the influence of charges under the gate is more efficient when the external $V_{GS-extrinsic}$ bias moves away from the inversion zone. Near the

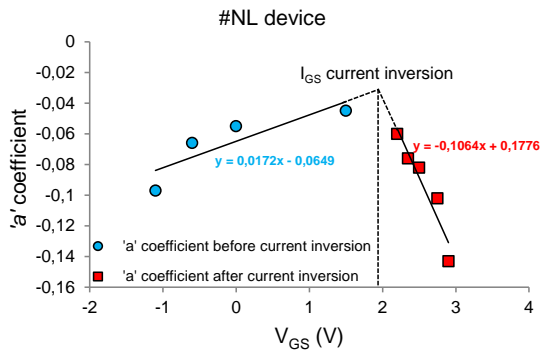


Fig. 8. Extractions of correlation coefficients ‘ a ’ for $\#NL$ device, biased at $V_{DS} = 8$ V.

inversion zone, ‘ $|a|$ ’-coefficient is at its lowest value, i.e. close to zero (no or weak influence of charges on I_{DS} - I_{GS} time dependent processes).

For $V_{GS} > V_{GS-inv}$ the Schottky diode works in its thermionic zone. Therefore, no difference is found between the 3 DUTs featuring different leakage levels in terms of ‘ a ’ coefficients versus V_{GS} . A same trend is featured and the slopes values versus V_{GS} exhibit identical values: -0.11 and -0.13 respectively for non-leaky device $\#NL$, and high leakage device $\#L_{high}$ HEMTs (red squares in Fig. 8 and Fig. 9).

For $V_{GS} < V_{GS-inv}$, the increase of ‘ $|a|$ ’ is more obvious for $\#L_{high}$ than for $\#NL$: ‘ $|a|$ ’ for $\#L_{high}$ is almost twice the value of ‘ $|a|$ ’ for $\#NL$. The negative sign of ‘ a ’ only concerns the relative variation of I_{GS} and I_{DS} .

Therefore, ‘ a ’ coefficient from equation (1) is evidenced as a strong indicator which translates the main gate current mechanism involved at a specific gate bias. The existing discontinuities from Fig. 8 and Fig. 9 concerning the values of ‘ a ’ clearly prove the fact that, depending on the gate bias (i.e. depending on the command), we are switching from a gate leakage mechanism to another one.

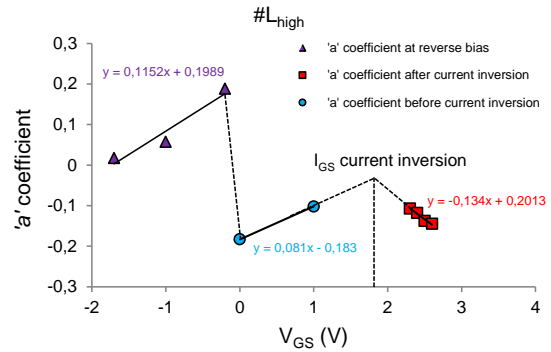


Fig. 9. Extractions of correlation coefficients ‘ a ’ for $\#L_{high}$ device, biased at $V_{DS} = 8$ V.

The incriminated charges in this current correlation through intrinsic voltage transient effects are positive or negative according to the upper or lower position of these charges at the interfaces of AlGaIn and GaN layers (Fig. 5): trapping/detrapping processes associated with acceptor or donor types of traps are activated during the test (0 s – 1500 s), with increases or decreases on I_{DS} - I_{GS} over short, medium and long time effects (large scale time constants). These important time variations of both I_{GS} and I_{DS} for $\#L_{high}$ are also consistent with Low Frequency Noise (LFN) measurements performed on these DUTs, featuring a

large number of generation-recombination centres on the drain current fluctuations, with large time constants (from several μs to few minutes) [4].

Fig. 9 illustrates a different behaviour, manifested at lower (negative) V_{GS} : $\#L_{high}$ features a new signature still convenient with the formulation given in equation (1). The discontinuity revealed for $V_{GS} < V_{GS-inv}$ is due to a change in the leakage mechanism. From $I_{GS}(V_{GS})$ measurements in Fig. 1, it can be stated that a different leakage mechanism is activated below -0.3 V (Fowler-Nordheim model substitutes to Poole-Frenkel representation). However, the same slope of ' a ' versus V_{GS} is extracted for the two zones in reverse bias conditions. These variations for $\#L_{high}$ (at 0.11 and 0.08) are estimated five times higher than that of $\#NL$ device (at 0.01). The increase on ' a ' dependency versus V_{GS} corresponds to the sensitivity of the device to time-dependent intrinsic voltage as depicted in Fig. 5 (thus to the fluctuations of I_{GS} and I_{DS}). Accordingly, a larger concentration of time-dependent charges under the gated zone is revealed for $\#L_{high}$, which in turn affects I_{DS} versus time and also P_{out} during the application of a RF signal. The selection of low-leakage devices will then be mandatory for this process in order to lower the drop of static and dynamic performances during time as evidenced on other GaN technologies [5].

5. Conclusions

This study focuses on transient correlations between gate and drain currents over a large time-scale. Effects of charges evolving with time (trapping/detrapping processes over short to large time constants) on the variation of gate and drain currents are evidenced; charges affect instantaneously the gated zone of the device, therefore I_{GS} and I_{DS} (through time dependence of the effective gate potential and, to a lesser extent, through the transconductance g_m).

The investigation also confirms the existence of different signatures of I_{GS} - I_{DS} time-dependent processes due to the presence of a lower or higher density of charges for low, medium and high leakage devices [3]. Our model allows to discriminate and to locate the gated zone under which the active charges are positioned, and to evaluate their influence on the transient stability of the quiescent point of the DUTs. The proposed model stands as an efficient non-invasive tool for improving the technological maturity of GaN devices. This study highlights the fact that the higher

the leakage is, the higher the charge density under the gate and the drop in the output power will be [5].

Our methodology can easily evidence the impact or the immunity of the leakage level to the degradation of static/dynamic performances of devices versus time. It can be also relevant for reliability assessment when different stresses are applied. Finally, this analysis at device level is also applicable to anticipate the time stability of the quiescent point once the transistor is used in its circuit context: the evolution of the 'static' I_{DS} with time will drastically affect the confidence level associated to the dynamic electrical signature of the RF circuit, and thus the reliability of the system.

Acknowledgements

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