Analysis of the three-chip switching cells approach for integrated multi-phase power converter combining monolithic and hybrid techniques: Experimental validation on SiC and Si power assembly prototypes

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Acknowledgements

This research work received financial support from the French National Research Agency (ANR). The project name is "ConvPlUS", ANR-13-JS09-0008-01, using the technological support of Renatech-LAAS and 3DPHI platforms. The authors are particularly grateful to Mr. Serge BONTEMPS, from Microsemi Power Modules, France, for providing power MOSFET and power diode Silicon dies.

Keywords

« Power hybrid integration », « Monolithic integration », « Packaging », « Commutation loop », « Stray inductance », « SiC power converter », « Insulated gate bipolar transistor (IGBT) », « 2D simulations »

Abstract

In this paper, the authors present a novel integration approach for multi-phase IGBT module, based on both monolithic and hybrid integration methods. In this proposed “3-chip” approach, the discrete switches are integrated into three generic monolithic multi-pole power chips and assembled with a judicious packaging. This reduces significantly the commutation loop area and so the stray inductance responsible of overshoot voltage and common-mode dv/dt effect. The operating modes of the multi-pole chips were validated in an inverter application by 2D simulations under mixed-mode Sentaurus™. In order to characterize the commutation loop of the 3-chip approach, two prototype power modules with different technologies (Si and SiC dies) have been realized on PCB substrates. The stray inductances were measured using a precision impedance analyzer (frequency analysis). A double-pulse characterization was also performed to illustrate the effect of stray inductance reduction at the turn-off (temporal analysis). For comparison purposes, two “classical” power converters have been also realized and analyzed. According the results, measurements and analytic estimates, the proposed packaging design allows reducing the stray inductance by at least a ratio of two as compared to the classical layout.

Introduction

Power electronic modules constitute one of the driving forces towards modularization and integration of power electronic systems [1] [2]. For instance, commercial IGBT power modules include single-phase leg and three-phase inverter, which utilize two or six pairs of anti-paralleled IGBT and freewheeling diodes. The packaging technology of power modules is mainly based on wire-bond technology. Stray inductance is a major concern in the design of IGBT packages and power stages with both high switching speed and high power handling requirements. Stray inductance inside a module package includes the inductance of electrode, inductance due to bonding wires and inductance due to substrate pattern [2].
The domain of power hybrid integration aims at producing a power electronics which is more compact and more reliable. One solution consists in the reduction of the commutation loop stray inductance.

Several contributions were reported for the stray inductance reduction. These approaches are based on the improvement in the structure of the package to reduce the parasitics of the module [1-4].
The proposed approach is an original concept in which the converter performance is improved through the integration both at the semiconductor level and at the power assembly level. Indeed, the power switches are judiciously integrated within three different monolithic power chips and a new assembly is devised so that to reduce the stray inductance of the commutation loop and its dv/dt effect with respect to ground.

Illustration of the proposed three-chip integration approach

The proposed approach allows the realization of a multi-phase IGBT based converter using only three generic independent power chips (Fig. 1a) [5-8]. For the high-side, the IGBTs and diodes are monolithically integrated in a single multi-pole Common Anode power chip (Fig. 1e) [5]. This monolithic chip is based on the vertical integration of multiple Reverse Conducting IGBT (RC-IGBT) [9-11]. For the low-side, the IGBTs are monolithically integrated in a vertical single multi-pole power chip (Fig. 1c). Likewise, the diodes are monolithically integrated in another vertical single multi-pole power chip (Fig. 1d). The backside of the low-side power chips (multi-pole IGBT and multi-pole Diode power chips) are relatively thick P^+ substrates which allows one to envisage the use of dielectrically filled deep trenches [12-15] for insulation between IGBTs and between diodes that share the same N- drift region within each power chip.

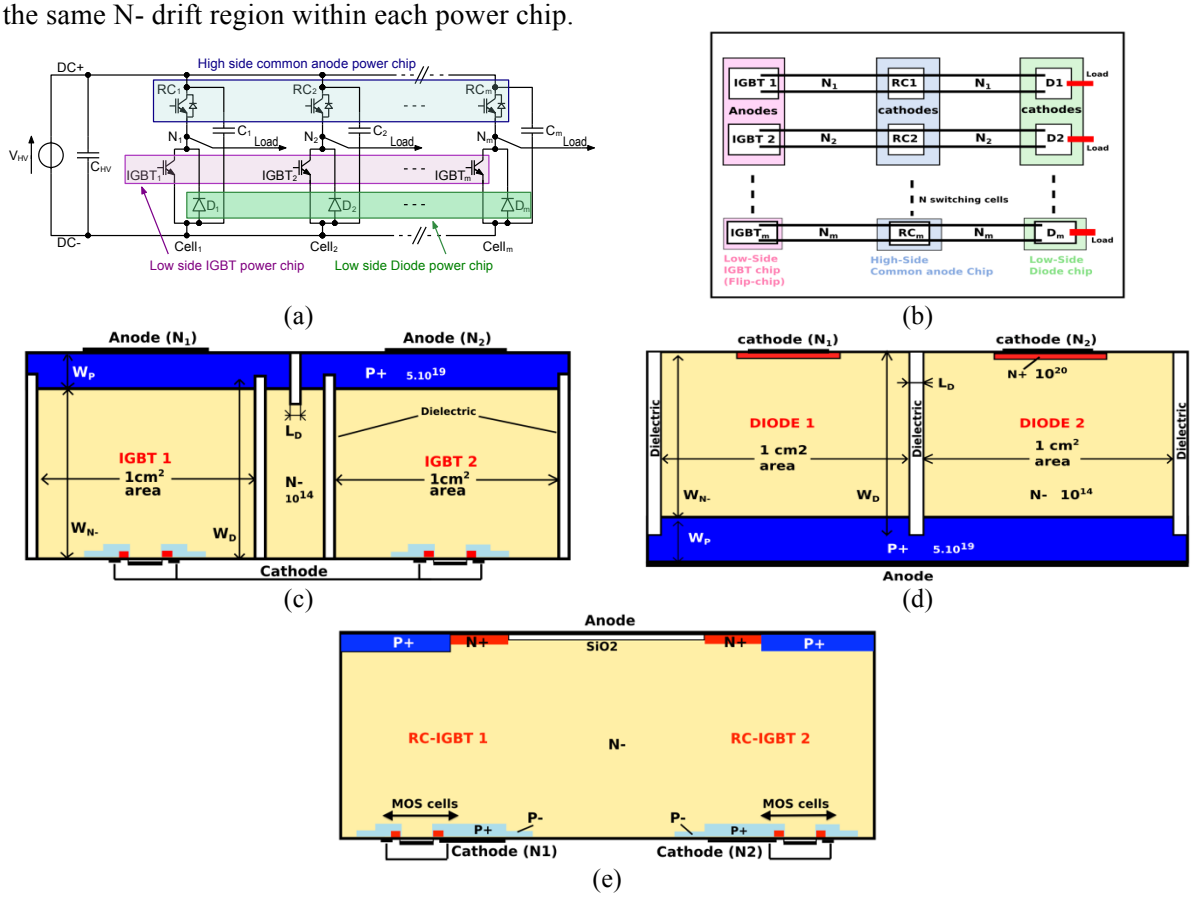


Fig. 1: (a) Three-chip integration approach, (b) top view of the targeted three-chip assembly for the multi-phase converter. Cross-sectional view of the proposed multi-pole power chips applied to an H-bridge converter: (c) multi-pole IGBT chip, (d) multi-pole Diode chip and (e) multi-pole Common Anode chip (the concept of the Common Anode chip was already presented).

Concerning the packaging, the three chips are placed so that the stray inductance of the switching cell is minimized. This is possible by placing the low-side IGBT multi-pole chip on one side of the common anode multi-pole chip and the low-side diode chip on the other side of the common anode chip as shown in figure 1b. Based on the fact that the load connection is at the top of one of the two low-side chips, no high dv/dt appears on the assembly substrate avoiding then any high frequency

leakage current through this one. The combination of a low stray inductance and a low common-mode leakage current is an interesting issue when considering fast Si power devices and WBG components. It should be noted that the three-chip approach is a generic approach which can be easily extended to a power converter consisting of "X"-phase. Thereby, the number of chips and the commutation loops remain unchanged as compared with the case of the H-bridge converter.

Application of the proposed 3-chip integration approach for an H-bridge converter

We study the three-chip approach in an H-bridge converter. To highlight the advantages brought by the 3-chip approach, two solutions are considered: the realization of a conventional H-bridge (Fig. 2a) and the realization of a 3-chip based H-bridge (Fig. 2b).
The conventional H-bridge uses four RC-IGBTs. For the validation of the 3-chip approach on an H-bridge, we use one Common Anode chip for the high-side but, for the low-side we use two discrete IGBTs and two discrete diodes. Common Anode chip, RC-IGBTs and IGBTs were realized in our micro and nanotechnology platform and characterized [5].
The operating modes of the three monolithic multi-pole power chips and their association within an H-bridge converter have been studied by 2D simulations. The results are presented in the following section.

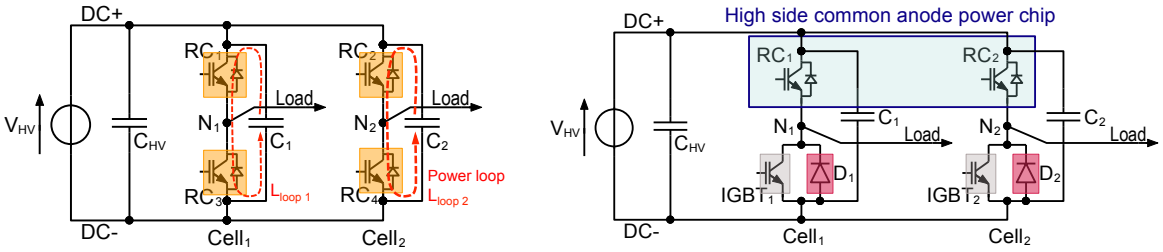


Fig. 2: (a) Conventional H-bridge, (b) 3-chip based H-bridge.

Validation of the three-chip based H-bridge by 2D simulations

Sentaurus™ 2D simulations were carried-out in order to validate the operating modes of the monolithic power chips. The operating modes of the common anode chip were already validated in previously reported works [5]. So we will focus on the operating modes of the two new monolithic multi-pole structures composed of IGBTs or diodes. We validated their operating modes separately in a simplified switching circuit. The simulation conditions and results are presented hereafter. It should be noted that in these two multi-pole monolithic structures, the active area of each section is of 1 cm^2 (see Fig. 1c and Fig. 1d).

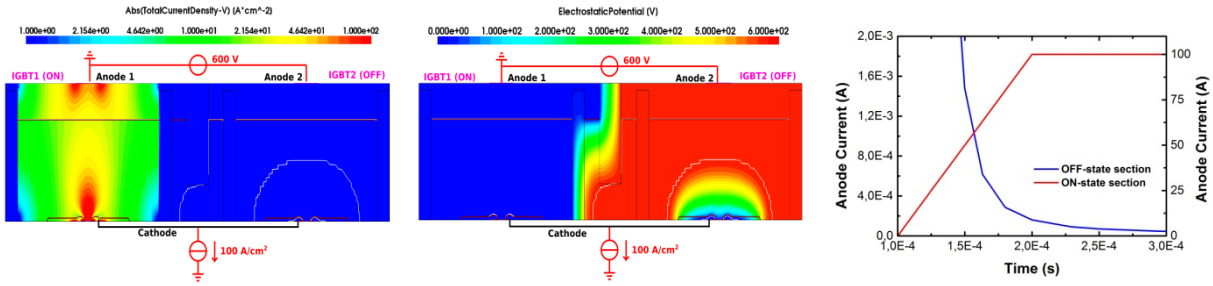
Table I. Geometrical parameters used for 2D simulations of multi-IGBT chip and multi-diode chip

Parameters	Description	Value (µm)	
		IGBTs chip	Diodes chip
W_N-	N_{drift} thickness	140	200
W_D	Trench depth	180	240
L_D	Trench width	70	40

Common cathode multi-IGBT power chip

This structure has three electrodes: two anode electrodes and one cathode electrode which is common for the two IGBT sections. In this inverter application, when one section is in ON-state, the other adjacent section is in OFF-state. So, this structure must support the applied anode1-anode2 voltage. Insulation between the two IGBT sections is achieved by dielectrically (oxide for 2D simulations) filled trenches that are placed between the IGBT sections. The simulation conditions are the following: a 600 V DC voltage is applied between the anode electrodes and a DC current supply of 100 A/cm^2 is

connected to the common cathode electrode. The left IGBT section is in ON-state with a gate bias of 15 V, the right IGBT section is in OFF-state with the gate-to-cathode voltage being set at 0 V. Figure 3a shows the current density distribution in ON-state IGBT section. Figure 3b shows the equipotential lines in OFF-state IGBT section. We can see that the right section is in OFF-state and a space charge expands in the N^- region between the dielectrically filled trenches. The leakage current in the OFF-state section is about 46 µA. The used trench depth in simulations is of 180 µm.



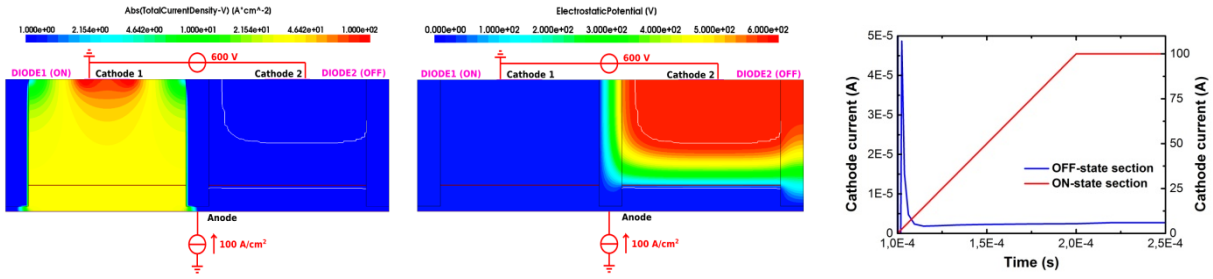
(a) (b) (c)

Fig. 3: (a) Distribution of current density, (b) equipotential lines distribution, (c) leakage current in OFF-state section.

Common anode multi-PiN-diode power chip

This structure has also three electrodes: two cathode electrodes at the top side and one anode electrode common to the two diode sections at the backside. This structure was chosen because it enables a direct top-to-top side connection with the common anode chip by means of one wire-bonding link without a flipping operation. This structure must support the applied voltage between the two cathode electrodes. To validate the operating modes, simulation conditions are the same as previously: a 600 V DC voltage is applied between the cathode electrodes and a DC current supply of 100 A/cm^2 is connected to the common anode electrode.

Figure 4a shows the distribution of current density in ON-state section of the multi-diode chip. Figure 4b shows the equipotential lines in OFF-state section of the multi-diode chip. We can see that the right diode section is reverse biased and space charge expands mainly in the N^- region. The leakage current in OFF-state section is about 2.7 µA. The trench depth used in simulations is of 240 µm.



(a) (b) (c)

Fig. 4: (a) Distribution of current density, (b) equipotential lines distribution, (c) leakage current in OFF-state section.

H-bridge converter

Once the operating modes of the two monolithic structures have been validated, we associated them with the common anode chip to realize an H-bridge chopper as shown in Figure 2b. The results are shown in figure 5. A 100 A DC-current source is inserted between the switching cells. A 600 V DC-voltage source is applied between the anode electrode of the common anode chip and the cathode electrode of the multi-pole IGBT chip. The IGBTs are controlled using a dead time of 1 µs.

(a) (b)

Fig. 5: (a) Simulated inverter circuit resulting from the association of the three monolithic chips, (b) zoom on switching phase.

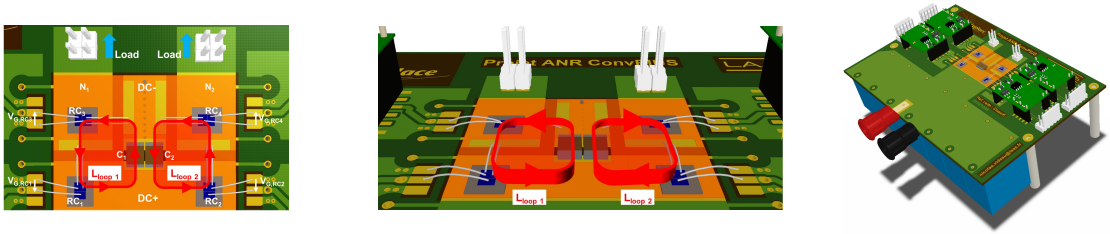
Packaging for the proposed 3-chip concept

Description of the power modules: conventional H-bridge and 3-chip H-bridge

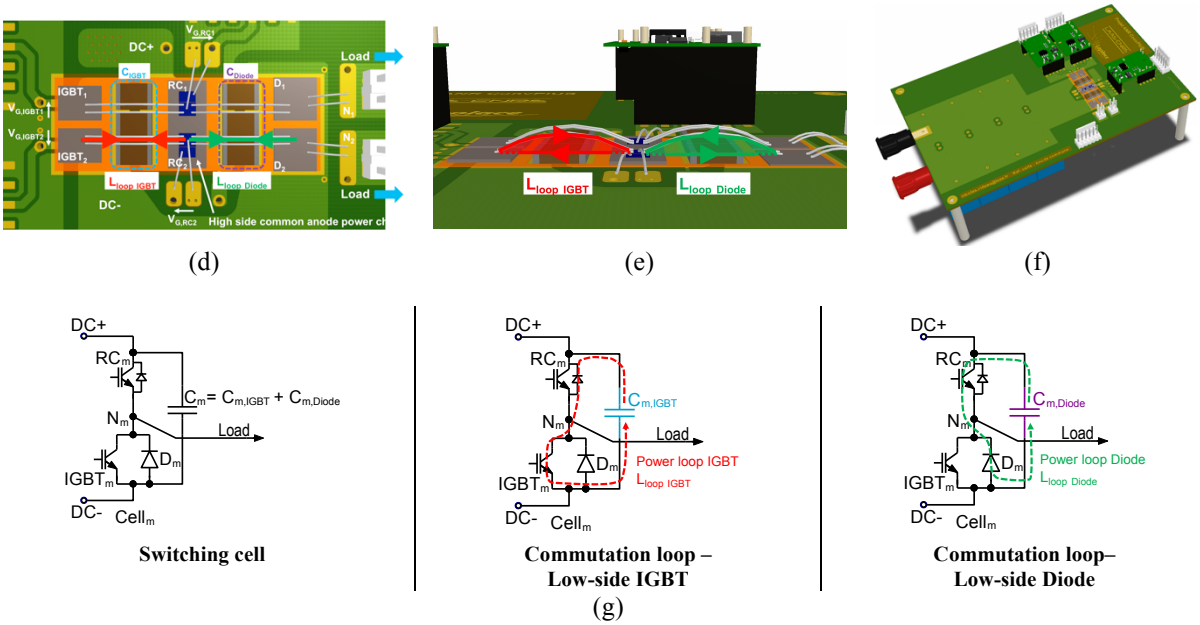
For the purpose of comparing and validating our optimization approach, two layouts of power converters were envisaged. The two converter versions are generic and can host power chips of different sizes and of different technologies (Si, SiC).
The first layout corresponds to the conventional converter, while the second layout corresponds to the proposed "3-chip" concept. Both converters were designed so that they can be realized in a power module. However, for validating this study, we realized/transposed our converters on a one-layer PCB substrate. The thermal aspect is not taken into account in this study. If one wants to design the converters only on a PCB substrate, he could preferably use a two-layer in order to obtain better commutation cells.

The conventional converter that uses four RC-IGBTs is given in figure 6a. A general view of the PCB with the control environment is given in figure 6c. With this conventional approach, the commutation loops are of equal length and coplanar with the PCB (Fig. 6b). The surface of the commutation loop is 130 mm².

For validating the 3-chip concept, a converter obtained by assembling a common anode chip, two IGBT chips and two PiN diode chips (see § III) is designed as shown in figure 6d. Within one "commutation leg", this approach decouples the functions of the diode and the IGBT. Therefore, the commutation loop of a single "leg" is divided into two loops. One loop « L_{Loop} IGBT » and one loop « L_{Loop} diode », of equal lengths and distributed on both sides of the central common anode chip (Fig. 6d). The decoupling capacitor C_m of the same leg is equally divided between the decoupling capacitance associated with the IGBT $C_{m,IGBT}$, and the decoupling capacitance associated with the diode $C_{m,diode}$ (Fig. 6g). The commutation loops are orthogonal to the PCB (Fig. 6e) and are greatly lower than the conventional layout [17]. A general view of the printed circuit board is given in figure 6f. The new assembly based on the three-chip approach permits to reduce the surface and hence the length of the commutation loop. This leads to a reduction in the stray inductance of the commutation loop. Indeed, the areas of the loops « L_{Loop} IGBT » and « L_{Loop} diode » are almost five times shorter than the conventional « L_{Loop} » (area L_{loop} IGBT = area L_{loop} Diode = 26 mm²). Stray inductance reduction permits to reduce losses during switching as well as voltage overshoot across power switches.



(a) (b) (c)



(d) (e) (f)

(g)

Fig. 6: (a) Top view of the conventional H-bridge and (b) coplanar power commutation loops, (c) design of the classical H-bridge in PCB version. (d) Top view of the three-chip based H-bride and (e) orthogonal power commutation loops, (f) design of the three-chip based H-bridge in PCB version, (g) switching cell decomposed into two commutation loops.

(a) (b)

Fig. 7: (a) Power module version of the conventional H-bridge, (b) power module version of the three-chip based H-bridge.

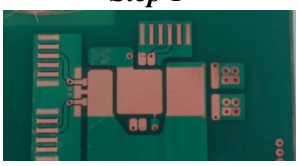
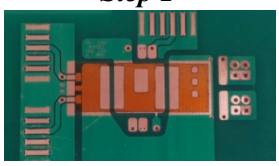
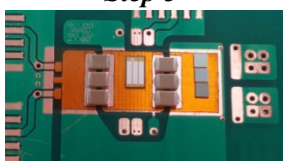
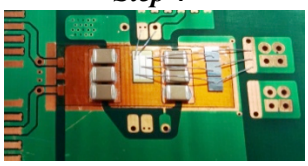
Assembly

This section describes the followed procedure for the realisation of the different converters. To that end, we consider the 3-chip converter that makes use of SiC chips. The assembling steps are the same for each of the other converters. The Kapton polyimide film is cut and windows, realized in the film, wider than the decoupling capacitor allow mounting this latter on the PCB, but smaller than the power chips for positioning the chips and to have access to the contacts (flipped chips and non flipped). The kapton film behaves as a passivation for flipped chips. The kapton film is first cut using laser and the following steps are summarized in table II for the case of a converter that uses SiC power chips. It should be noted that the procedure is generalizable.

The advantages of this solution are:

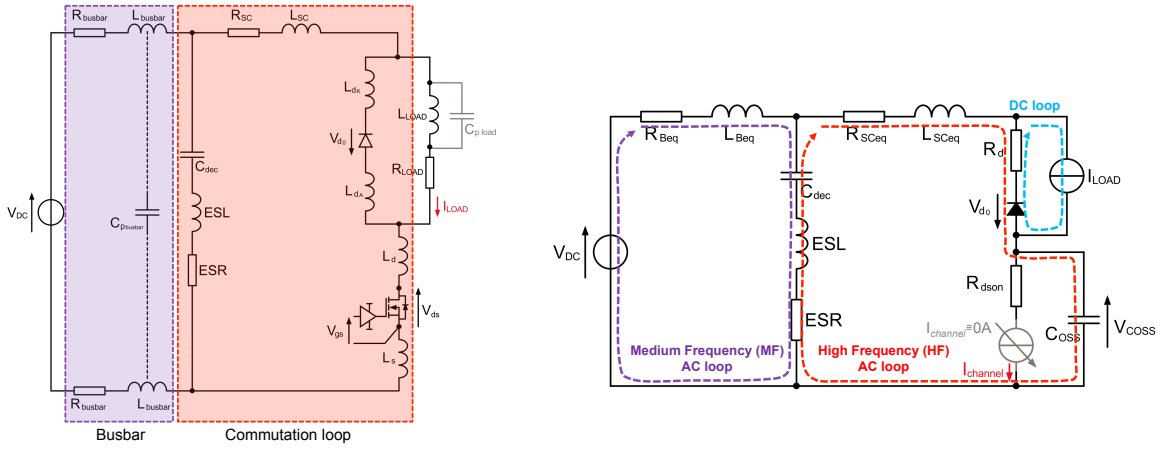
- Easy to implement, robust, and industrializable,
- Placement of the chips (in x/y),
- Height control,
- Flip-chip of the chips.

Table II. Description of the steps for assembly

Step 1	*Step 2*	*Step 3*	*Step 4*
			
Kapton film cut using laser (Laser CO_2 FineMarkerHybrid Trotec). Used insulation film: Kapton double-sided acrylic (Kapton 75µm ARclad 7876 Adhesives Research).	Kapton positioning on the PCB.	Conductive epoxy (EpoTek H20E) and positioning of power chips and capacitors. Placed in an air-oven (80-90°C/2h30-3h).	Wire bonding: 25 µm (Gate) and 250 µm (Drain-Source).

Modeling of an elementary commutation loop at turn-off

We consider the case of a fast and hard switching to turn-off, obtained using a very small external gate resistance (or close to zero) that gives birth to a negligible Miller effect in time duration (disappearance of Miller plateau) [16]. In these conditions, the driver output voltage is quasi-directly applied to the gate MOSFET (remains only the polysilicon gate resistance and the driver's output resistance). Therefore, the MOS channel current decreases to zero before the voltage starts to rise significantly across the MOSFET (i.e sequence of dV_{ds}/dt) and the equivalent parasitic capacitance seen between the drain and the source is given by $C_{oss} = C_{ds} + C_{gs}$. The free wheeling diode starts to conduct as soon as C_{oss} is fully charged. Therefore, the commutation loop at turn-off of the controlled switch can be modelled by the following schematics:



(a) (b)

Fig. 8: (a) Modeling of the switching cell with parasitic components and (b) its equivalent diagram at turn-off.

Therefore, the total maximum overshoot voltage across the switch can be obtained by summing up the terms of overvoltage that appear in Fig. 8b):

$$\delta Vc_{ossMAX} = I_{load}\sqrt{\frac{L_{Beq}}{C_{dec}}} + KI_{load}\sqrt{\frac{L_{SCeq}+ESL}{C_{oss}}} + V_{diode} + \left(L_{SCeq}+ESL\right)\frac{di_{channel}}{dt} \qquad (1)$$

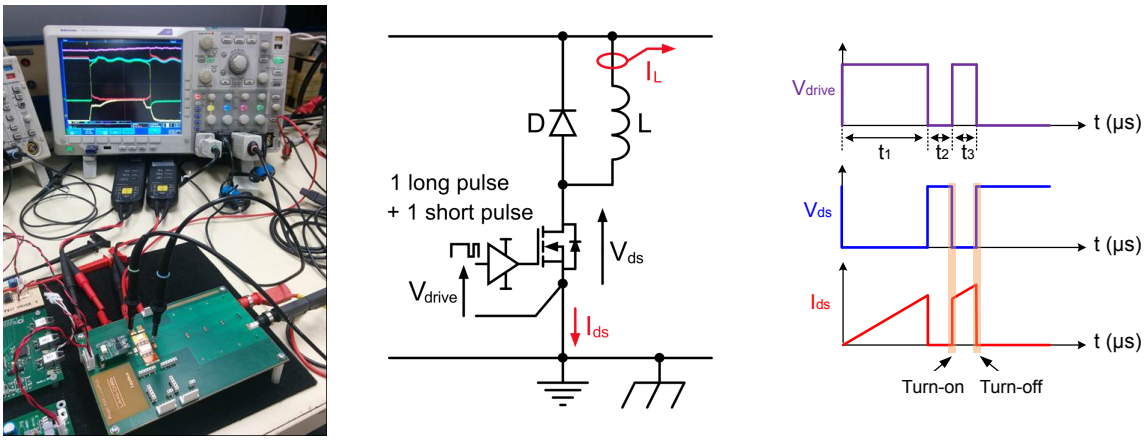
a) *b)* *c)* *d)*

According to this equation, we can see the different terms associated to the commutation loop. Terms a) and b) deals with the effect of the storage energy in the stray inductance of the busbar and the stray inductance of the switching cell on the overvoltage across C_{dec} and C_{oss}. The first one is low and at

medium frequency (<5MHz) while the second is predominant more and more with WBG chips that exhibit low capacitance.cm² values compared to Si devices and so a high frequency oscillation (>50MHz). In term b), K represents the factor of current sharing between C_{oss} and C_{Tdiode}. Term c) describes the dynamic forward recovery at the turn-on of the diode, especially for Si PIN diode. Finally, term d) represents the effect of a residual channel current through the switching loop if a significant Miller effect is realized. In summary, for integrated and fast converter, the ratio ESL_X/C_X must be minimised in order to reduce oscillations. A reduction in C_X must be accompanied by a reduction of ESL_X in the same proportion.

Method for the characterization in time domain of the commutation cell at turn-off

A frequency domain modeling approach based on the decomposition into constitutive elements (set of wire bonds, decoupling capacitor and filtering, busbar, PCB…) was realised by means of an Agilent 4294A impedance analyzer associated to a coaxial compensated probe 42941A dedicated for measurements on a PCB. The results will not be presented in detail in this paper. Only the measurement values will be provided for comparison purposes with the temporal analysis approach (which is described in this section).
In order to highlight the oscillations at power device turn-off, we tested the converters (conventional as well as proposed) using the classical double pulse method. This circuit is generally used for the characterisation of overvoltage phenomena at turn-off. The principle consists in controlling the phase leg with two pulses. The first pulse allows current installation, the second one, which is smaller and closer to an ideal impulse, permits the excitation of the commutation cell in order to obtain the oscillations.



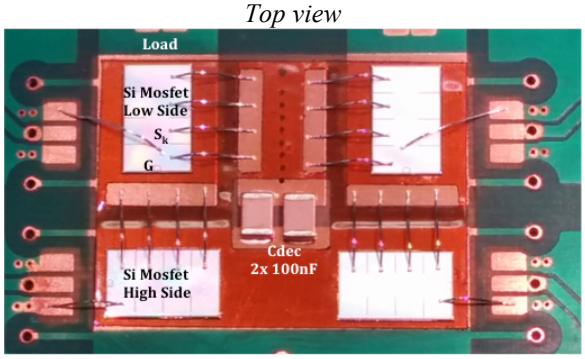
(a) (b) (c)

Fig. 9: (a) Test bench for devices switching characterization, (b) test circuit in Buck-Type topology, (c) control signals of the "double-short pulse" method (Oscilloscope TEK DPO4104B 1GHz/5GSamp.s^{-1} + Passive voltage probes TPP1000 1GHz Deskew mode + Hi/Average x4 mode).

In this paper, the characterization of the commutation loops of the previously presented assemblies (see Fig. 6) focus on the analysis of the voltage waveform across one of the transistors (between drain-kelvin and source-kelvin) at turn-off. The lower side transistor is preferred because it allows eliminating measurements perturbation by the effect of the involved common mode voltage. The analysis of the components constituting the amplitude and frequency of the voltage waveform enable us to extract the physical parameters characterising the quality of the commutation cell. According to equation 1, two main temporal components are involved: the first one is called HF allows to characterize the couple (L_{SCeq}, C_{oss}), the second one called MF allows to characterize the couple (L_{Beq}, C_{dec}).
This methodology will be applied to two groups of converter boards. One group corresponds to an assembly called "conventional" and uses two chips mounted on the backside and wired using two sets of wire bonds (cf. Table III): case 1.1) (silicon version) and case 1.2) (full-SiC version). A second group corresponds to an assembly equivalent to the thee-chip approach detailed in § II of this paper. In this "proposed" assembly, one of the two chips of the commutation cell is mounted using flip-chip

technique and wired using a single set of wire bonds (cf. Table IV): case 2.1) (silicon version) and case 2.2) (full-SiC version). One of the main objectives of these measurements is to compare the assembly types and mainly the interconnection of the chips.

Table III. Characterization of "conventional" Si and SiC power converters

<table>
<tr><th colspan="2">Conventional converter: the two chips are mounted on backside and interconnected by two sets of wire bonds</th></tr>
<tr><td>Case 1.1) Silicon chips</td><td>Case 1.2) SiC chips</td></tr>
<tr><td><u>Half-bridge</u>: 2x Mosfet Si SIPC69N60C3 (CoolMos FET 600V/47A@25°C- 6.59 x 10.52 mm²)</td><td><u>Buck-Type</u>: 1x Mosfet SiC CPM2-1200-0025B (4.04 x 6.44 mm²) + 3 SBD SiC // CPW4-1200-S015B (2.70 x 2.70 mm²)</td></tr>
<tr><td>Top view
 
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 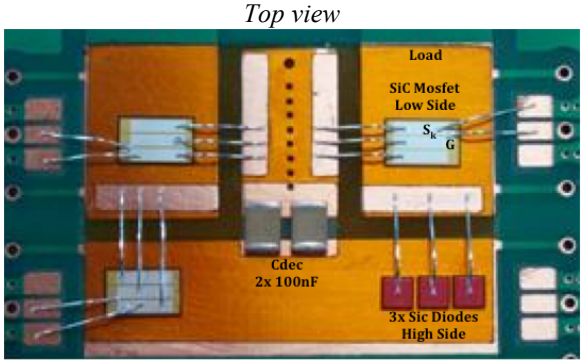
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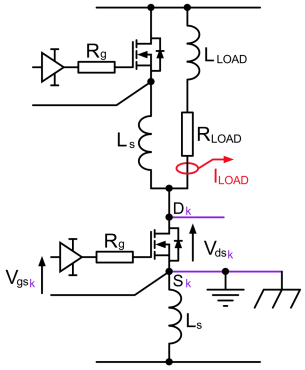
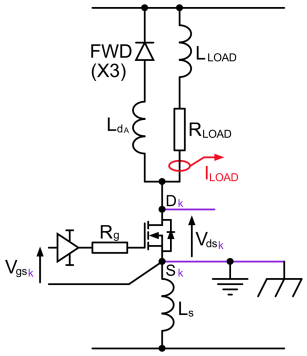
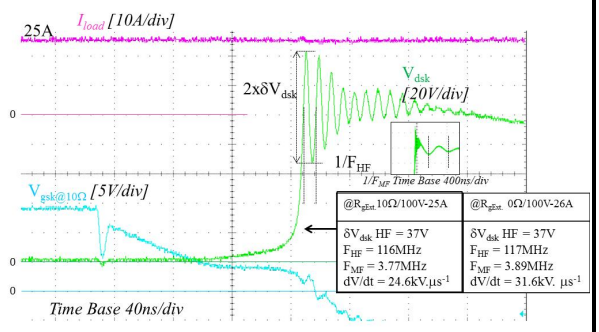
 

Vdrive = +18V/-18V, RgExt. ∈ [0Ω, 10Ω]</td><td>Electrical schematic
 

Vdrive = +19V/-2.5V, RgExt. ∈ [0Ω, 10Ω]</td></tr>
<tr><td>Turn-off waveforms
 
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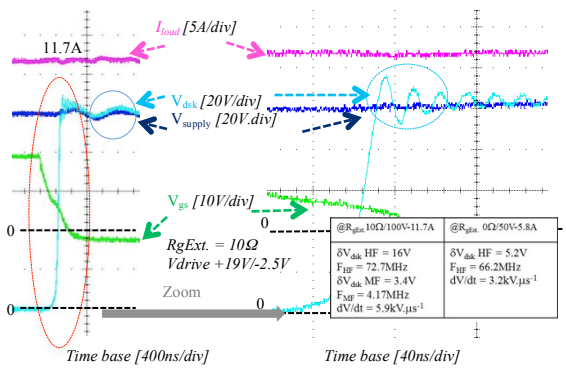
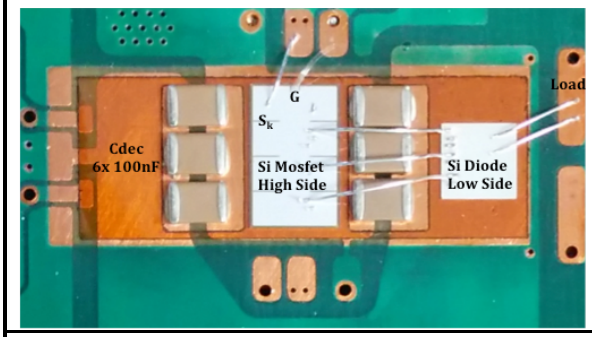
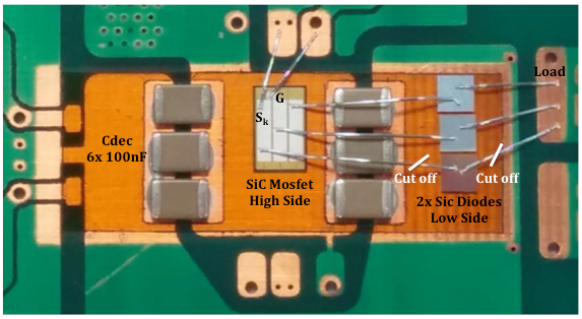
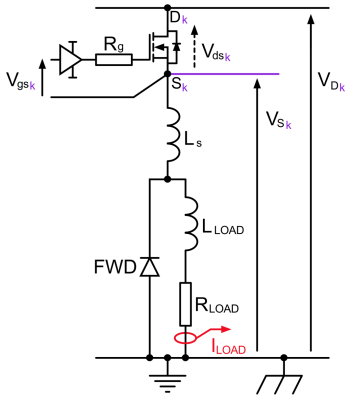
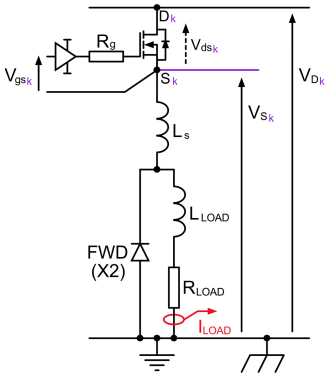
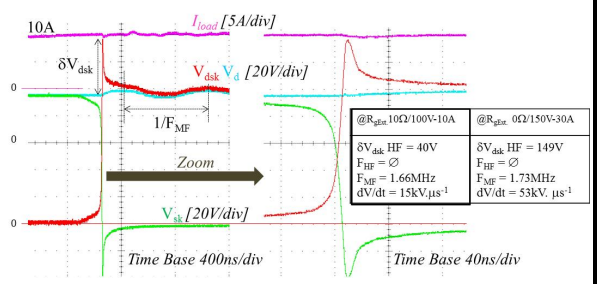
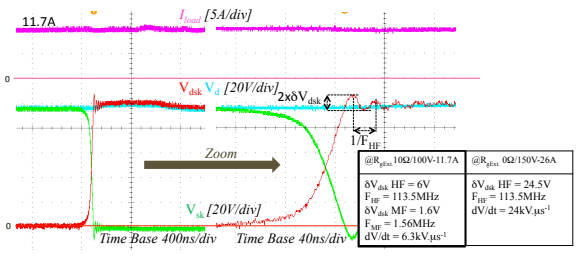
 
</td></tr>
</table>

Table IV. Characterization of "proposed" Si and SiC power converters

<table>
<tr><th colspan="2">Proposed converter: one of the two chips is mounted in flip-chip and interconnected by a single set of wire bonds</th></tr>
<tr><th>Case 2.1) Silicon chips</th><th>Case 2.2) SiC chips</th></tr>
<tr><td>Buck-Type: 1x Mosfet Si SIPC69N60C3 (CoolMos FET 600V/47A@25°C - 6.59 x 10.52 mm²) + 1 diode SIDC30D120H8 (5.5 x 5.5 mm²)</td><td>Buck-Type: 1x Mosfet SiC CPM2-1200-0025B (4.04 x 6.44 mm²) + 2 SBD SiC // CPW4-1200-S015B (2.70 x 2.70 mm²)</td></tr>
<tr><td>Top view
 
</td><td>Top view
 
</td></tr>
<tr><td>Electrical schematic
 

Vdrive = +18V/-18V, RgExt. ∈ [0Ω, 10Ω]</td><td>Electrical schematic
 

Vdrive = +19V/-2.5V, RgExt. ∈ [0Ω, 10Ω]</td></tr>
<tr><td>Turn-off waveforms
 
</td><td>Turn-off waveforms
 
</td></tr>
</table>

Frequency analysis with impedance analyzer and probe has allowed realizing distinct and reproducible measurements on the commutation loops. These results are considered as reference results (Table V).
The results show that the optimized commutation loop is at least twice less inductive than the classic loop. This gain allows to increase the safety margin (SOA) and the reliability level, and to reduce the overshoot across the power devices, the turn-off losses and EMI emission. Integration of both decoupling and filtering capacitors with chips allow to reduce strongly stray inductances values, compared to a power module (type IPM internal stray > 20nH). The optimized commutation loop can be further improved with a better thermal substrate combined to a volumic passivation, allowing to minimize the distance between the chips and so the length of interconnections.
Two methods of extraction of the stray inductance values have been proposed: the first a) based on the peak value of the first HF voltage oscillation, the second b), based on a) and combining the dV_{coss}/dt

expression, finally c) based on the time period of the oscillation. For now, the damping factor is not considered. So, one can demonstrate that method a) gives lower bound values whereas method c) gives upper bound values. Method c) is more easy and accurate to implement, and gives more coherent results as compared to the impedance analyser measurements.

Table V. Stray inductance value: comparison between measured and analytic estimated values

<table>
<tr><th rowspan="2">Equivalent loop inductances on busbar stage and switching cell stage</th><th colspan="3">Medium-frequency busbar-loop characterization
(equivalent localized physical quantities: L_{beq}, C_{dec})</th><th colspan="3">High-frequency switching-cell loop characterization
(equivalent localized physical quantities: L_{sceq}, ESL_{dec}, C_{oss})</th></tr>
<tr><th>Measured values</th><th colspan="2">Analytic estimated values</th><th>Measured values</th><th colspan="2">Analytic estimated values</th></tr>
<tr><td></td><td>1) Frequential 100MHz Impedance Analyzer Agilent 4294A + dedicated PCB Probe 42941A

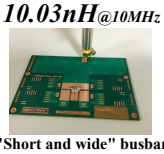
2) Capacimeter Agilent B1505a

3) Temporal analysis oscilloscope TEK DPO4104B 1GHz/5GSamp.s^{-1} + Passive voltage probes TPP1000 1GHz (Deskew mode + Hi/Average x4 mode)</td><td colspan="2">a) From the voltage ripple
(damping neglected → giving a lower bound value):
$L_{beqMIN} = C_{dec}\left(\frac{\delta V_{Cdec}}{I_{load}}\right)^2$

b) From the oscillation period
(damping neglected → giving a upper bound value) :
$L_{beqMAX} = \frac{1}{C_{dec}.(2\pi.F_{MF})^2}$</td><td>1) Frequential 100MHz Impedance Analyzer Agilent 4294A + dedicated PCB Probe 42941A

2) Capacimeter Agilent B1505a

3) Temporal analysis oscilloscope TEK DPO4104B 1GHz/5GSamp.s^{-1} + Passive voltage probes TPP1000 1GHz (Deskew mode + Hi/Average x4 mode)</td><td colspan="2">a) From the voltage ripple
(damping neglected → giving a lower bound value):
$L_{sceqMIN} = C_{oss}\left(\frac{\delta V_{Coss}}{K.I_{load}}\right)^2 - ESL_{eq}$
Buck-Type: $K = \frac{C_{oss}}{C_{oss}+C_{Tdiode}}$ | Half-Bridge: $K = \frac{1}{2}$
b) From the voltage ripple "a)" and dV_{max}/dt
$\frac{dV_{max}}{dt} = \frac{K.I_{load}}{C_{oss}}$
$L_{sceqMIN} = \frac{(\delta V_{Coss})^2}{K.I_{load}.dV_{max}/dt} - ESL_{eq}$
c) From the oscillation period
(damping neglected→ giving a upper bound value):
$L_{sceqMAX} = \frac{1}{C_{oss}.(2\pi.F_{HF})^2}$</td></tr>
<tr><td>1.1) Classic Si (Half-Bridge)
2x Mosfet Si SIPC69N60C3 (data & measures)
C_{oss}@100V = 300pF
C_{oss}@150V = 220pF
→ K = 0.5</td><td rowspan="2">Cdec : 2xKEMET-X7R - 500V Ref.C1812V104 (measures)
2x60nF@100V
2x45nF@150V
ESL = 0.8nH
ESL_{eq} = 0.4nH
$C_{filter\ (fp)}$: EPCOS B32654A4335/2x3.3uF/ 400V/ESL_{eqMAX}=9nH

$L_{bateq\ MEASURE}$ = 10.03nH@10MHz
 
"Short and wide" busbar</td><td>a) 25A/100V/ RgExt. 10Ω/ δV_{Cdec} = 8.4V

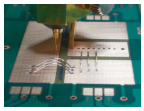
$L_{beq\ MIN}$ = 13.5nH</td><td>b) 25A/100V/ RgExt. 10Ω/3.8MHz

$L_{beq\ MAX}$ = 14.6nH</td><td>9.5nH
(Extrapolated value)
@10MHz
(4W in 2x series)</td><td>a) 26A/100V/ RgExt.0Ω/δV_{Coss} = 37V-b) 25A/100V/RgExt.10Ω/31.6kV.µs^{-1}

$L_{sceq\ MIN}$ = 2.4nH-4.4nH</td><td>c) 26A/100V/ 117MHz/RgExt.0Ω-28A/150V/133MHz/ RgExt.0Ω

$L_{sceq\ MAX}$ = 6.1nH-6.5nH</td></tr>
<tr><td>1.2) Classic SiC (Buck-Type)
1x Mosfet SiC CPM2-1200-0025B + 3x SBD SiC // CPW4-1200-S015B (data sheet)
C_{oss}@100V = 470pF
C_{Tdiode}@100V = 3x170pF
→ K_{100} = 0.48</td><td>a) 11.7A/100V/ RgExt. 10Ω/δV_{Cdec} = 3.4V

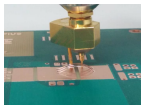
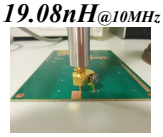
$L_{beq\ MIN}$ = 10.2nH</td><td>b) 11.7A/100V/ RgExt. 10Ω/4.2MHz

$L_{beq\ MAX}$ = 11.9nH</td><td>10.7nH
@10MHz
(3W in 2x series)
  </td><td>a) 11.7A/100V/ RgExt.10Ω/δV_{Coss} = 16V -b) 11.7A/100V/ RgExt.10Ω/5.9kV.µs^{-1}

$L_{sceq\ MIN}$ = 3.8nH-7.7nH</td><td>c) 11.7A/100V/ 72.7MHz/RgExt.10Ω

$L_{sceq\ MAX}$ = 10.2nH</td></tr>
<tr><td>2.1) Proposed Si (Buck-Type)
1x Mosfet Si SIPC69N60C3 + 1x diode SIDC30D120H8 (data & measures)
C_{oss}@100V = 300pF
C_{Tdiode}@100V = 65pF
→ K_{100} = 0.82</td><td>a) 10A/100V/ RgExt. 10Ω/δV_{Cdec} = 2V

$L_{beq\ MIN}$ = 14.4nH</td><td>b) 10A/100V/ RgExt.10Ω/1.7MHz

$L_{beq\ MAX}$ = 24.3nH</td><td>4.5nH
@10MHz
(3W in 1x series)
  </td><td colspan="2">∅
(no resonance, only dynamic forward recovery of the diode)</td></tr>
<tr><td>2.2) Proposed SiC (Buck-Type)
1x Mosfet SiC CPM2-1200-0025B + 2x SBD SiC // CPW4-1200-S015B (data sheet)
C_{oss}@100V = 470pF
C_{oss}@150V = 400pF
C_{Tdiode}@100V = 2x170pF
C_{Tdiode}@150V = 2x140pF
→ K_{100} = 0.58
→ K_{150} = 0.59</td><td>$L_{beq\ MEASURE}$ = 19.08nH@10MHz
 
"Long and narrow" busbar</td><td>a) 24.5A/100V/ RgExt. 10Ω/δV_{Cdec} = 5V

$L_{beq\ MIN}$ = 15.0nH</td><td>b) 11.7A/100V/ RgExt. 10Ω/1.6MHz

L_{beqMAX} = 27.5nH</td><td>5.3nH
@10MHz
(2W in 1x series)</td><td>a) 26A/150V/ RgExt.0Ω/δV_{Coss} ≅ 24.5V-b) 26A/150V/ RgExt.0Ω/24kV.µs^{-1}

$L_{sceq\ MIN}$ = 1.02nH-1.63nH</td><td>c) 11.7A/100V/ RgExt.10Ω/113.5MHz

$L_{sceq\ MAX}$ = 4.2nH</td></tr>
</table>

Conclusion

The aim of this work was to present a novel approach for integration of multi-phase converters, that combines both monolithic integration and hybrid assembly of Si-chip. This converter integration approach makes use of three multi-pole power chips to realize any generic multi-phase power converter. The operating modes of each power chip were validated independently and in a complete H-bridge inverter, using mixed mode Sentaurus™ simulations. In order to characterize the commutation loop of the 3-chip approach, two power modules with different technologies (Si and SiC dies) have been realized on PCB substrates and the stray inductances were measured using a precision impedance analyzer. Double-pulse characterizations were also performed to illustrate the effect of stray inductance reduction at the turn-off. For comparison purposes, two classical power converters have been also realized and analyzed. According the results, the proposed layout allows reducing the stray inductance by at least a ratio of two as compared to the classical layout. To further improve the performances, a Direct Lead Bonding (DLB) version for the proposed packaging is envisaged.

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