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# Bandgap Failure Study Due To Parasitic Bipolar Substrate Coupling In Smart Power Mixed ICs

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**Abstract**— In order to merge low power and high voltage devices on the same chip at competitive cost, Smart Power integrated circuits (ICs) are extensively used. The presence of low power and high voltage devices in Smart Power ICs cause parasitic substrate interaction between switched power stages and sensitive analog blocks. Nowadays this is the major cause of failure of Smart Power ICs, inducing costly circuit redesign. Modern CAD tools cannot accurately simulate this type of interaction expressed as an injection of minority carriers in the substrate and their propagation in the substrate. In order to create a link between circuit design, modelling and implementation in innovative CAD tools there is a need to validate these models by measuring the high voltage perturbations that activate parasitic structures in the substrate directly on the chip. This paper presents a study of bandgap failure issues due to the substrate coupling induced by high power parts of the circuit which can activate parasitic bipolar structures inside the substrate of Smart Power ICs.

**Keywords** — *Bandgap; Smart Power IC; substrate noise coupling; electromagnetic compatibility; substrate parasitic bipolar structures;*

## I. INTRODUCTION

Nowadays, many segments of microelectronics move towards monolithic system integration merging on the same IC (Smart power ICs) low voltage analog and/or digital parts with high voltage parts using power transistors.

Substrate coupling in Smart power ICs occurs when parasitic bipolar structures (with unpredictable size and location) are activated after an injection of current into the substrate due to internal switching activity or external noise coupling. When low power analog and digital applications are integrated with high voltage (HV) devices on the same IC, these side effects become very important and hurtful to the circuit operation. In turn, designers have to rely on empirical basis for the design strategy, which is expensive and time consuming. Today, when simulating circuits with HV-MOSFETS devices, their specific SPICE models are used in every CAD tool but these models do not address generation of these parasitic substrate currents of minority and majority carriers.

AUTOMICS project [1] aims at providing SPICE models that, once implemented in CAD tools, will allow optimizing

high voltage and high current capability, EMI-EMC performance with respect to substrate parasitic robustness.

Moreover, AUTOMICS should considerably improve the design methodology by developing efficient CAD models of parasitic structures activated by HV functions integrated in automotive Smart Power ICs [1]. In order to detect parasitic bipolar structures activation and the induced substrate coupling effect, some well-defined experiments can demonstrate this harmful phenomenon for the circuit and thereby validate the proposed Spice models of the parasitic bipolar junction. These measurements will be performed with a source-meter, on a test vehicle designed using the AMS H35, High Power 0.35 $\mu$ m technological process.

This paper aims at presenting, in real application conditions, an analysis of bandgap failures issues due to the activated parasitic bipolar structures inside the substrate of Smart Power ICs when high power parts of the circuit injects a critical amount of current into the substrate. This analysis aims to propose a substrate coupling scenario and then compare it to SPICE based simulations with the measurements done with a specially designed test vehicle. Section II briefly presents substrate-coupling issues in Smart Power ICs. Section III introduces the principles of work and failure issues of the analyzed bandgap device architecture. Section IV presents experimental measurements of substrate coupling effects and demonstrate the activation of bipolar parasitic structures in Smart Power IC.

## II. SUBSTRATE COUPLING ISSUES IN SMART POWER ICs

In Smart Power ICs, the sources of substrate coupling are parasitic NPN and PNP bipolar transistors (Fig. 1) activated by 'below-ground' or 'above-supply' working conditions of High Voltage-MOSFETS at the circuit output [2], [3]. These parasitic bipolar transistors can be activated during normal circuit operation by the switching on/off of inductive loads. They can be also activated during usual automotive chip testing (EMI-EMC and ESD tests), by external electromagnetic perturbations or electrostatic discharges.

Two physical mechanisms are behind this type of coupling as seen in Fig.1 and Fig.2. The first one is the injection of electrons (minority carriers) into the p substrate when the drain of the power NMOS, at the power output of the circuit,

is below the ground potential and thus activates a parasitic NPN transistor (Fig.1). These minority carriers injected into the substrate can be collected by every surrounding nwell and causing a voltage fluctuation of the nwell of a surrounding sensitive blocks and cause its dysfunction. The second physical mechanism is the injection of holes (majority carriers) into the p substrate (Fig.2). This happens when the drain of the power PMOS (i.e. the power output of the circuit), exceeds the power supply voltage VDD, activating a parasitic PNP transistor. This in turn leads to a local voltage shift of the substrate potential in the neighbor sensitive electronic blocks.

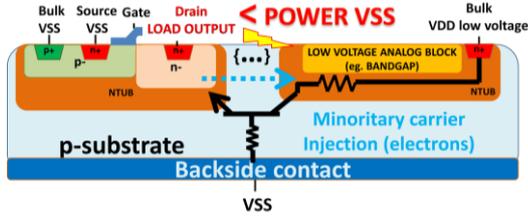


Fig.1 The activation of parasitic bipolar NPN transistor between a power NMOS and a low power device

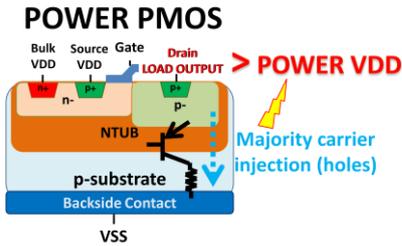


Fig.2 The activation of parasitic bipolar PMOS transistor inside the substrate

### III. BANDGAP : WORK PRINCIPLE & FAILURE ISSUES

#### A. A general architecture description

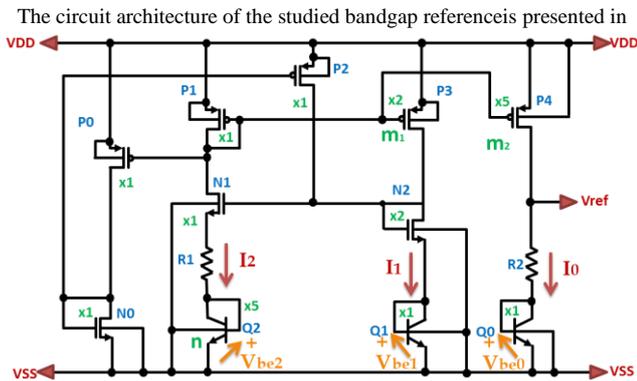


Fig.3 below. It's a classical design of a bandgap reference circuit with voltage-mode output, which provides a reference voltage of 1.23 volts [4], [5]. The main feature of this type of circuit is to have a complementary-to-absolute temperature (CTAT) voltage combined with a proportional-to-absolute temperature (PTAT) voltage in order to have, by summing them, an ideally zero temperature coefficient output reference voltage  $V_{ref}$ . The circuit uses the properties of the

combination of a forward-biased PN junction voltage and a voltage proportional to the thermal voltage  $V_t = kT/q$ , the CTAT and the PTAT voltage respectively. In the presented design, the CTAT voltage is represented by the diode junction voltage  $V_{be}$  of the bipolar transistors Q2, Q1 and Q0. The circuit has one start up circuit (MOS transistors P2, P0 and N0), one current source with current  $I_2$  (MOS transistors P1 and N1) and its two mirrored currents  $I_1$  and  $I_0$  (MOS transistors P3, N2 and P4, N3). The polysilicon resistors  $R_2$  and  $R_1$  are used to fine adjust the output voltage  $V_{ref}$  by the ratio  $R_2/R_1$ .

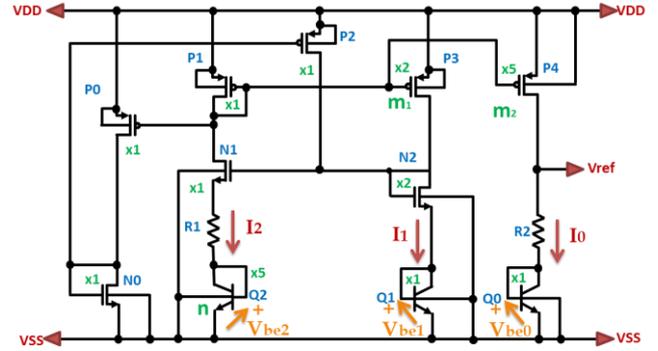


Fig.3 : The architecture of the bandgap under study

The output voltage  $V_{ref}$  is defined by the following equations:

$$m_1 = 2 ; m_2 = 5 ; n = 5 ; I_0 = m_2 I_2 ; I_1 = m_1 I_2 \quad (1)$$

$$V_{ref} = R_2 I_0 + V_{be0} \quad (2)$$

$$V_{ref} = \frac{R_2 I_0}{R_1 I_2} V_t \left( \ln(n) + \ln\left(\frac{I_1}{I_2}\right) \right) + V_{be0} \quad (3)$$

$$V_{ref} = \frac{R_2}{R_1} 5V_t (\ln(5) + \ln(2)) + V_{be0} = 1.23 V \quad (4)$$

#### B. Bandgap failure issues

In the bandgap design presented here a failure is defined when its output reference voltage  $V_{ref}$  differs from its nominal voltage (around 1.23 V). A current substrate coupling can lead to this type of failure causing a current injection in each leg of the circuit and thus the currents  $I_2$ ,  $I_1$  and  $I_0$  will be altered, as seen on the Fig.4.

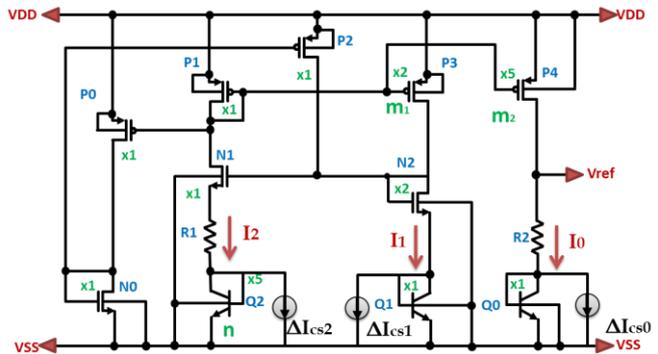


Fig.4 The bandgap failure scenario: substrate current collected with the bipolar transistors collectors Q2, Q1 and Q0

Fig.4 describes the hypothetical scenario of substrate current collected by the collectors of the bandgap bipolar

transistors  $Q_2$ ,  $Q_1$  and  $Q_0$ . Here, the currents sources  $\Delta I_{cs2}$ ,  $\Delta I_{cs1}$  and  $\Delta I_{cs0}$  model these substrate currents caused by the injection of the minority carrier on these collectors nwells by the activation of an parasitic bipolar transistor inside the substrate of the Smart Power circuit as described on last chapter and seen on Fig.1. Depending on the amount and the sign of these injected currents the output reference voltage may vary. Thus the equation (3) becomes:

$$V_{ref(\Delta I_{cs012})} = \frac{R_2}{R_1} \frac{I_0}{I_2 \pm \Delta I_{cs2}} V_t \left( \ln(n) + \ln \left( \frac{I_1 \pm \Delta I_{cs1}}{I_2 - \Delta I_{cs2}} \right) \right) + V_t \ln \left( \frac{I_0 \pm \Delta I_{cs0}}{I_s} \right) \quad (5)$$

Here, in this circuit, the most sensitive devices to minority carrier injection are the bipolar NPN transistors  $Q_2$ ,  $Q_1$  and  $Q_0$ . As their collectors are designed in an nwell layer, they can collect the substrate currents and thus decrease the currents  $I_2$ ,  $I_1$  and  $I_0$ . Taking account the circuit architecture and the size ratio of bipolar transistors  $Q_2$ ,  $Q_1$  and  $Q_0$  we can predict that the collector of the transistor  $Q_2$  will collect 5 times more substrate current. Thus the last equation (5) gives us the equation (6):

$$V_{ref(\Delta I_{cs012})} = \frac{R_2}{R_1} \frac{I_0}{I_2 - 5 * \Delta I_{cs2}} V_t \left( \ln(n) + \ln \left( \frac{I_1 - \Delta I_{cs1}}{I_2 - 5 * \Delta I_{cs2}} \right) \right) + V_t \ln \left( \frac{I_0 - \Delta I_{cs0}}{I_s} \right) \quad (6)$$

Deeper analysis of the last equation (6) shows that the output voltage  $V_{ref}$  will increase according to the injected current (up to slightly less its power supply voltage VDD).

#### IV. STUDY OF BANDGAP SUBSTRATE COUPLING ISSUES IN SMART POWER CIRCUITS

The bandgap device with a high power device has been implemented in a Smart Power IC in order to study the substrate coupling effect caused by the activation of parasitic bipolar transistors. The tested structures have been designed in 0.35 $\mu$ m AMS High Voltage CMOS technology using the H35 20V design kit with 3 metal layers. In this technology, low voltage transistors are isolated from high voltage part of the circuit by a buried N-WELL. The bandgap is entirely designed with 5V MOS transistors for the startup circuit and for the current source and mirrors, except for the  $V_t$  voltage reference where low power bipolar transistors are used. The test circuit includes also one DC-DC converter designed with high voltage 20V MOS driver on its output. The DC-DC converter and the bandgap are isolated by means of a high voltage guard rings surrounding each structure in order to collect the substrate current as much as possible. The circuit is mounted in a 32 QFN package, and soldered on a four-layer EMC test board with all surrounding electronics and I/O connections.

Two case studies are intended in this work. The first one is done during nominal bandgap circuit operation and consists in observing the coupling effects due to an external injection of a DC current on the output of a power device (DC-DC converter). I(V) characterization of the substrate parasitic bipolar structures activated by the current injected into the substrate are done. In parallel, SPICE simulations of the bandgap under study are performed in order to compare results with measured ones. The second case study aims at observing also the coupling effects to the bandgap nominal operation but

with an injection of a pulsed DC current on the output of the same power device. The results will be presented on the final version of the paper.

#### A. Experimental I(V) characterization of the parasitic bipolar NPN transistor

This experiment aims at activating the parasitic bipolar structures and characterizes them using a four quadrants source meter. In order to obtain characteristic I(V) curves of these parasitic bipolar transistors, the source meter is used to inject the current into the substrate of the test circuit: by controlling both current and voltage at the output of the DC-DC converter (pin TX\_LX) and at the power supply pin of the bandgap (pin BG\_VDD), the effects of an inductive charge can be simulated for instance. In this case study the activation of the parasitic NPN transistor is analysed, as seen in Fig.5.

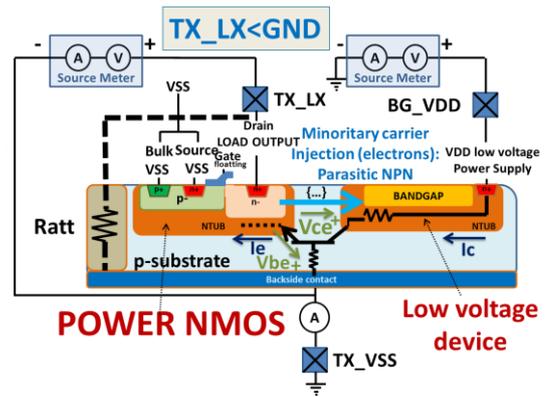
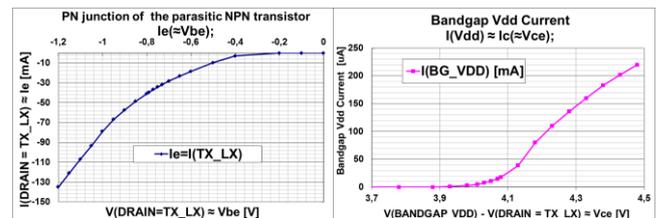
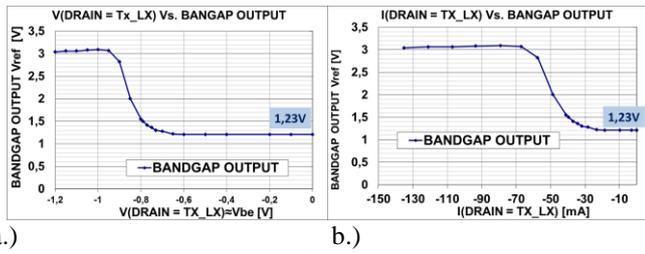


Fig.5 Experimental I(V) characterization of the parasitic bipolar NPN transistor

In this experience the DC-DC converter was disabled in order to have both PMOS and NMOS output transistors in tristate mode and avoid their damaging, even their destruction. Here, the  $R_{att}$  resistance stands for the equivalent resistance of the rest of the circuit. The next step consists in analysing the activation of the parasitic NPN transistor by biasing the drain (TX\_LX output pin) of the power NMOS transistor below the ground voltage. The threshold voltage of the forward biased diode formed by the n well of the NMOS drain and the p well of the p-substrate is measured at  $V_{be} = -0.4$  V, as shown in Fig 6.a. The effects of the working conditions of the bandgap are observed in **Erreur ! Source du renvoi introuvable.** and Fig.7.



a.) b.) Fig.6 Parasitic NPN characteristic transfer curves: a)  $I_e(V_{be})$  and b)  $I_c(V_{ce})$



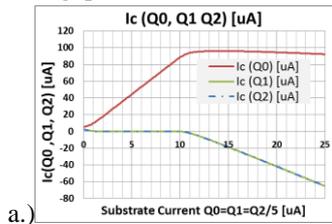
a.)  
b.)  
Fig.7 Parasitic NPN activation influence on the bandgap output voltage:  
a.) vs. NMOS drain voltage  
b.) vs. NMOS drain current

The Fig.6a.) shows the activation of the PN junction (between n region of the drain of NMOS, the TX\_LX pin, and the p region of the substrate) due to the minority carrier injection. This in turn activates the parasitic bipolar NPN transistor within the substrate. The minority carrier current collected on the bandgap power supply Vdd and bandgap guard ring rises with the  $V_{ce}$  voltage, as shown in Fig.6b.. But the main consequence of the activation of the parasitic bipolar NPN transistor, is that the bandgap output increases from its nominal 1.23V to slightly less its supply voltage of 3.3V progressively, leading to its dysfunction as seen on Fig.7. As explained in part III.B, this is essentially due to the increasing of the current inside the current mirrors present in the bandgap circuit architecture, which in turn is transferred to its output due to the deviation of the reference current.

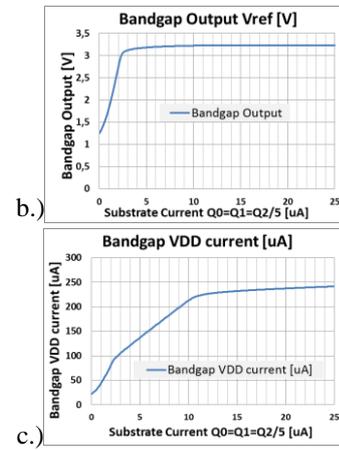
### B. SPICE simulations of the bandgap failure scenario

The influence of the parasitic bipolar NPN transistor activation to the bandgap structure is now modelled by three current sources  $\Delta I_{cs_0}$ ,  $\Delta I_{cs_1}$  and  $\Delta I_{cs_2}$ . Defining a more complex and accurate model of this substrate current coupling is outside of the topic of this paper which is more oriented to the analysis of the failure mechanisms of the low voltage blocks due to the activity of high voltage blocks in Smart Power circuits. These three current sources simply model the substrate current due to an injection of minority carriers into the substrate from the drain of the power NMOS, and doesn't take into account of all bipolar parasitic elements within the substrate between the different parts of the circuit. Moreover, these minority carriers are collected with a certain amount, which depends of the size of the collecting device, its distance from the injection source and the amount of current injected. Thus this substrate current is modelled as flowing from the collector nodes of the bandgap bipolar transistors  $Q_2$ ,  $Q_1$  and  $Q_0$  to the substrate, as seen in Fig.4.

On the next figures in Fig.1, are presented simulation results of the proposed bandgap failure scenario:



a.)



c.)

Fig.8 Simulation of substrate current injection to the bandgap:  
a.) Bandgap collector  $Q_2$ ,  $Q_1$  and  $Q_0$  currents; b.) Bandgap output voltage  $V_{ref}$   
c.) Bandgap power consumption increase due to the substrate coupling;

They confirm the hypothesis exposed in the last chapter: the bandgap output voltage reference  $V_{ref}$  grows up if both conditions are satisfied:

- a substrate current injection occurs, producing an injection of majority carriers into the substrate, from the high voltage devices
- if these majority carriers are collected by collector nodes of bandgap bipolar transistors.

If these conditions are satisfied, the currents circulating in each of three legs with transistors  $Q_2$ ,  $Q_1$  and  $Q_0$  will decrease by the amount of by currents  $\Delta I_{cs_2}$ ,  $\Delta I_{cs_1}$  and  $\Delta I_{cs_0}$  respectively. This in turn leads to an increase of  $V_{ref}$  as seen in equation (6).

The experimental I(V) characterization of parasitic bipolar structures are compared to the SPICE simulation results in order to validate the hypothesis that the substrate current is collected by the collectors of the bandgap bipolar transistors.

### C. Comparison of the experimental I(V) characterization of the parasitic NPN transistor vs. SPICE simulations of the bandgap failure scenario

**Erreur ! Source du renvoi introuvable.** presents the comparison between experimental results and simulations of the bandgap output reference voltage  $V_{ref}$  and its power consumption current when current is injected into the substrate. Simulated and measured curves are quite similar, confirming the bandgap disturbance scenario.

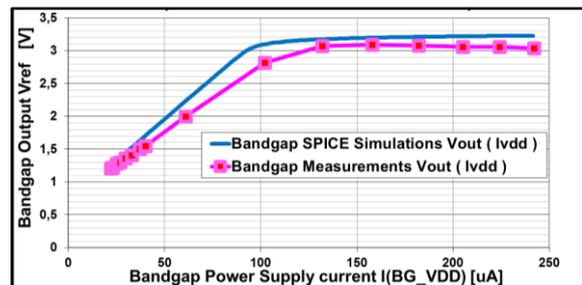


Fig.9 Bandgap output voltage  $V_{ref}$  vs. Bandgap VDD current: Measurements vs Simulation

This result clearly shows the impact of the substrate coupling due to the activation of parasitic bipolar structures caused by the minority carrier injection into the substrate and collected by the bandgap bipolar transitions collectors.

## V. CONCLUSIONS

This paper presents an analysis of bandgap failures issues due to the activation of parasitic bipolar structures inside the substrate of Smart Power ICs in real application conditions. This is the main cause of circuit failure which occurs when high power parts of the circuit inject a critical amount of current into the substrate.

Bandgap bipolar transistors collectors collect the minority carriers injected in the substrate by the high voltage part and an analytical approach of this type of failure was performed. This phenomenon is modelled by the equivalent current sources flowing down from the bandgap bipolar transistors collectors to the substrate. In this simple model not all substrate parasitic elements were included but for a first sight this model gives enough guidance for understanding this phenomenon. A deeper analysis with more precise modelling of this parasitic substrate coupling is currently achieved within the European project AUTOMICS. SPICE simulations results, of the hypothetical model of substrate coupling through the bandgap collectors of its bipolar transitions were then verified experimentally.

To do this, one experimental Smart Power IC test vehicle was developed. The effect of substrate coupling mechanism was demonstrated by an experimental I(V) characterisation of the parasitic bipolar NPN transistor. A proposed scenario of the bandgap failure was confirmed by a comparison of this measured NPN I(V) characteristic to the SPICE simulation. It

was shown also that the most critical parts of the bandgap circuit were its bipolar transistors.

The amount of the coupling via the substrate depends strongly of the circuit layout and thus this coupling needs to be well modelled and integrated within the CAD tools in order to help designers to predict this kind of events once the layout of the circuit was routed. This is the main objective of the project AUTOMICS.

A further work, which is currently performed, will also include transient coupling effects. The further analysis will be performed using the same test vehicle when a pulse injection occurs on the critical nodes. Thus it will complete the analysis of the parasitic bipolar substrate coupling between high power and low power parts in a Smart Power IC.

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