A New Synthesis Methodology for Reliable RF front-end Design

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***Abstract*—A low power and low cost WLAN/WiMAX RF front-end requires more advanced CMOS technologies whose transistor parameters degradation is becoming worse. Few published works has presented the reliability results for RF circuits. In order to fill this gap, we develop a new synthesis methodology for reliable RF front-end design using the design example of a reliable BLIXER. The first steps of our synthesis methodology is a transistor ageing simulation. Then, we calculate an estimation of the circuit performance and ageing using the circuit design equations and the total derivatives. Thus, we can find the required bias and sizing improving the circuit reliability.**

The simulation results of the typical circuit are coherent with the WLAN/WiMAX RF front-end specifications. Despite the integrated process variability and mismatch, we observe that 96.4 % of the simulation runs have Gain > 10.0 dB, and 92.1% of the simulation runs have NF_{max}< 5.0 dB. Moreover, the BLIXER ageing degradation is negligible according to the fitted Poisson distribution of the power consumption for 99.9% of confidence. Going further, we can say that the synthesis methodology proposed and developed for a RF front-end design can be exploited in different AMS/RF circuits and also generalized for a single bottom-up reliable-system design approach.

I. Introduction

A low power and low cost WLAN/WiMAX RF front-end requires more advanced CMOS technologies for electronic circuit integration. Transistor parameters degradation is becoming worse in these technologies, while application fields like military, medical and aerospace demand less variability and more reliability. The first block of a RF front-end is the low-noise amplifier, and design a robust amplifier is one of the most important challenges for a robust RF front-end. Few published works has presented the reliability results for RF power amplifiers [1][2], and for RF oscillators [3]. In order to fill this gap, we develop a new synthesis methodology for reliable RF front-end design using the design example of a reliable BLIXER [4], which aggregates a balun, a wide-band low noise amplifier (WBLNA), and a mixer.

The state-of-the-art of analog synthesis methodologies have two main assignments: topology selection and sizing. Between those two assignments, we can also distinguish: circuit-level synthesis and system-level synthesis. In this work, we will suppose that a circuit-level synthesis shall be done according to a given set of typical performance specification [5]. However, the circuit design is connected with the integrated process variability and ageing. Thus, a new design criterion should be take into account on a synthesis methodology: the variation of the circuit performance. The variation of the circuit performance in short time is often estimated by a variability analysis. Such analysis can be based on meta-modeling techniques [6] or Monte Carlo simulations. The variation of the circuit performance in long lifetime can be estimated by ageing models according to a physical phenomena degradation [7].

The physical phenomena mostly responsible for the ageing degradation in active devices are: *Hot Carrier Injection (HCI)* [8], *Negative Bias Temperature Instability (NBTI)* [2], *Time Dependent Dielectric Breakdown (TDDB)* [9]; and passive devices have ageing degradation caused by *Electromigration (EM)* [10]. From all phenomena, the transistors of the reliable BLIXER design example are only degraded by HCI. HCI is the phenomenon that charges gain sufficient energy to overcome a potential barrier and then migrate to a different area of the device. Such phenomenon occurs at the end of the drain junction of a transistor in saturation, creating many interface traps, which increase the substrate leakage current and cause drain current to decrease. The HCI takes effect when the V_{GD} is greater than or equal to zero and the V_{GS} is very high [8]. Therefore, this phenomenon could be avoided if we reduce the time in which the transistors are in strong inversion, by controlling V_{GD} and V_{GS}.

In this work, we propose a reliable circuit-level synthesis methodology using the circuit design equations to obtain an early estimation of the circuit performance ageing. The circuit variability is not considered as a criterion of the synthesis methodology in this work. Thus, the CMOS 65 nm integrated process ageing shall be characterized, and the sensible circuit bias conditions can be identified. Using the circuit design equations, we can early estimate and reduce the impact of ageing on circuit performance. In Section II, we describe the basis of the proposed synthesis methodology. Then, we characterize the CMOS 65 nm integrated process ageing degradation in Section III. In Section IV, we present the BLIXER design example using the proposed synthesis methodology. In Section V, the circuit simulation results are shown for typical performance, variability and ageing degradations. Finally, we present our conclusions.

II. Synthesis Methodology

In the near future, ageing estimation tools will be available as the variability estimation tools already are, and both will be part of the design process. The ageing must be placed in early stages and must be connected in a single methodology in order to design a reliable circuit.

The operational frequency, bandwidth, power consumption, noise, linearity and gain are the most important RF front-

end performances. However, variability and ageing may change them leading to drop out the RF standard specifications. Mostly designers include margins when specifying such performances and it may lead to an overdesigned circuit. In order to improve the circuit design, it is needed some design experiments which are not often possible to attend the time-to-market with advanced semiconductor technologies. Thus, we propose to use the circuit design equations to also estimate these margins. So that, we can avoid the overdesign without large design experiments at early design steps.

The circuit performances can be defined as

$$\Phi_{min} = \Phi_{typ} - \Delta\Phi, \tag{1}$$

where Φ_{typ} is typical performance and $\Delta\Phi$ is calculated in Equation (1) by the minimum performance (Φ_{min}). The margins $\Delta\Phi$ also is the total derivative of the function $\Phi(\Phi_1,...,\Phi_n)$ of the n transistor parameters. And so,

$$\Delta\Phi \approx \frac{\partial\Phi}{\partial\Phi_1}\Delta\Phi_1 + ... + \frac{\partial\Phi}{\partial\Phi_n}\Delta\Phi_n, \tag{2}$$

where $\Delta\Phi_1,...,\Delta\Phi_n$ are the estimation of the transistor parameters variations by variability and ageing.

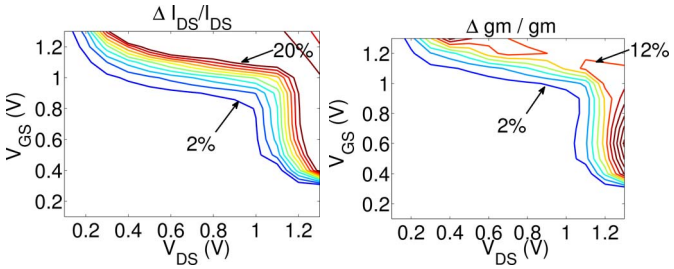
Subsequently, the transistor parameters (Φ_i) and its variation ($\Delta\Phi_i$) shall be characterized for a target integrated process. By choosing the stress time and the environment conditions, the designer has enough information to design the circuit for a determined Φ and also specify the circuit lifetime by the $\Delta\Phi$. Thus, the proposed synthesis methodology can evaluate ageing degradation with the circuit design equations, their total derivatives, and the transistor ageing simulation. However, Equation (2) is not a valid approximation to estimate $\Delta\Phi$ if the transistor parameters Φ_i are treated by a statistical distribution as the case of the integrated process variability. Thus, the proposed synthesis methodology is characterized by a nominal reliability estimation and simulation. The integrated process variability is considered after the sizing and bias are determined. Moreover, most of the transistor parameters are statistically dependent which increase the complexity of $\Delta\Phi$ estimation and prevents the hand analysis advantage of this synthesis methodology. In order to simplify the design equations leading a hand analysis, we choose the transistor drain current and the transistor transconductance to be focus on the ageing simulation and we exclude the variability as a design criterion.

III. CMOS 65 nm Ageing Simulation

We will characterize the transistor ageing by the drain current (I_{DS}) degradation and by the transconductance (gm) degradation to a normalized NMOS (W = 1 μm and L = 60 nm). The target stress time is 30 years of lifetime and the environment conditions are: bias stress up to $1.1V_{DD}$ and 27 ^{o}C of temperature. The percentage of degradation of the transistor parameter is defined as

$$\frac{\Delta\Phi_i}{\Phi_i} = \frac{\Phi_{i_{AGED}} - \Phi_{i_{FRESH}}}{\Phi_{i_{FRESH}}}. \tag{3}$$

In Figures 1(a) and 1(b), we show the percentage of degradation of I_{DS} and gm respectively. In order to design a reliable circuit, we shall choose the transistor bias limiting the parameters degradation to a maximum allowed degradation. Thus, the circuit reliability will be assured for 30 years of lifetime and under the stress conditions of the ageing simulation. Then, such percentage of degradation shall be used to estimate the total performance degradation by its total derivative (as Equation 2). In the other hand, the performance degradation could be specified and the maximum percentage of ageing degradation could be calculated, estimating the circuit reliability.



(a) (b)

Figure 1. Ageing of the I_{DS} (a) and the gm (b) of the normalized NMOS (W = 1 μm and L = 60 nm).

IV. BLIXER Design Example

In this section, we will present the BLIXER design example using the proposed synthesis methodology. The chosen topology is presented in Figure 2 and its specifications in Table I. For the circuit design, we did a I_{DS} and gm versus bias simulation for a fresh normalized NMOS (W = 1 μm and L = 60 nm) [11] (not present in this work) and the CMOS 65 nm integrated process ageing simulation proposed in Section III.

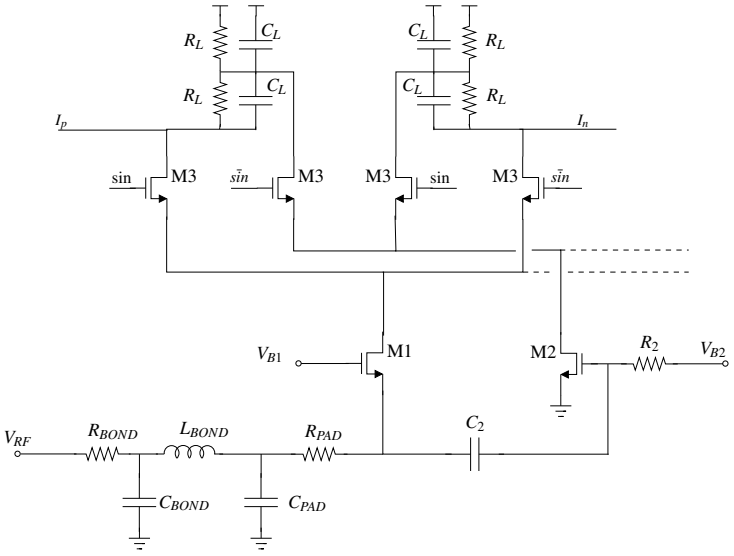


Figure 2. The BLIXER topology composed by a balun, a wide-band low noise amplifier (WBLNA), and a mixer connected: illustration of the I path (the Q path is not present as it is similar to the I path) [4].

The first and most important performance to evaluate is the power consumption, as in equation

$$\mathrm{P} = V_{DD}\,(I_{D1} + I_{D2})\,. \tag{4}$$

Table I
THE BLIXER SPECIFICATIONS FOR WLAN/WIMAX APPLICATIONS.

Operational Frequency	1 GHz - 5 GHz
Bandwidth	> 100 MHz
Gain	> 10 dB
NF	< 5.0 dB
IP3	> 1 dBm
S11	< -10 dB

Then, we found the total derivative of such performance as

$$\Delta \mathrm{P} \approx V_{DD}\left(\Delta I_{D1} + \Delta I_{D2}\right), \tag{5}$$

which leads to a decreasing power consumption with the I_{DS} ageing degradation. Thus, the circuit degradation does not degrade this performance. Moreover, the power consumption is an easy way to evaluate the circuit ageing degradation.

Subsequently, the circuit gain is

$$\mathrm{G} = \frac{2gm_1R_L + gm_2R_L}{2}, \tag{6}$$

and its total derivative is

$$\Delta \mathrm{G} \approx \frac{2\Delta gm_1R_L + \Delta gm_2R_L}{2}. \tag{7}$$

So that, the gain degradation shall be estimated by the *gm* ageing degradation, shown in Figure 1(b). The circuit bandwidth is not controlled by transistor parameter as it is

$$\mathrm{BW} = \frac{1}{2\pi R_L C_L}, \tag{8}$$

and it does not degrade with transistor ageing. The input impedance matching is

$$\mathrm{S11} = \frac{1 - gm_1R_s}{1 + gm_1R_s}, \tag{9}$$

where R_s is the source resistance and the total derivative is

$$\Delta \mathrm{S11} \approx \frac{-2\Delta gm_1R_s}{\left(1 + gm_1R_s\right)^2}. \tag{10}$$

Thus, it is a performance with a large sensitivity to the ageing degradation of the *gm* of the M1 transistor.

Finally, the noise factor is

$$\mathrm{F} = 1 + \frac{\frac{\left((2gm_1R_{L1})^2 - (gm_2R_{L2})^2\right)}{gm_1R_s+1}\overline{e_{n1}^2} + (gm_2R_{L2})^2\overline{e_{n2}^2} + \overline{e_{nL1}^2} + \overline{e_{nL2}^2}}{\frac{\left((2gm_1R_{L1})^2 + (gm_2R_{L2})^2\right)}{gm_1R_s+1}\overline{e_{nS}^2}}, \tag{11}$$

where $\overline{e_{ni}^2}$ is the noise voltage of the component *i*. This equation was obtained by the BLIXER noise analysis of the noise model presented in Figure 3. The total derivative of the noise factor is

$$\Delta \mathrm{F} \approx \frac{\partial \mathrm{F}}{\partial gm_1}\Delta gm_1 + \frac{\partial \mathrm{F}}{\partial gm_2}\Delta gm_2, \tag{12}$$

and the equation expansion was not presented here to save space.

Considering only the typical circuit performance, a classical synthesis methodology consist in optimizing the circuit sizing. After that the designer should simulate the circuit variability and ageing. Using a given specification of maximum ageing degradation of the transistor parameters and the performance total derivatives (Equations (7), (12) and (10)), we propose

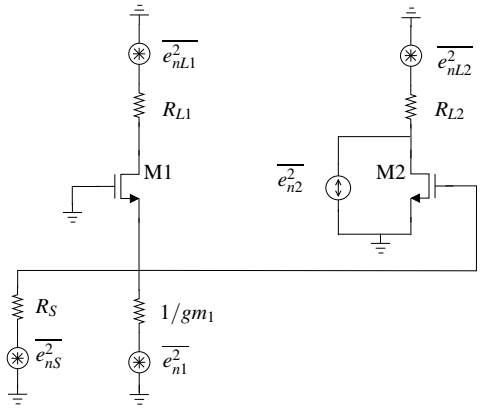


Figure 3. The BLIXER noise model: illustration.

to early estimate the circuit performance ageing. Assuming the case of 10 % degradation of the transistor parameters, we found the estimated performance degradation as: $\Delta \mathrm{P}/\mathrm{P} = 20$ %, $\Delta \mathrm{G}/\mathrm{G} = 20$ %, $\Delta \mathrm{S11}/\mathrm{S11} = 18.63$ %, and $\Delta \mathrm{F}/\mathrm{F} =$ -25.71 %. Such information shall be used on the synthesis methodology to improve the circuit against ageing. Moreover, it leads to how much sensible the chosen circuit schematics and technology are to ageing degradation.

V. BLIXER SIMULATION RESULTS

In order to increase the circuit reliability and also to achieve the desired performance, the required circuit bias is $V_{DS} = 0.4$ V and $V_{GS} = 0.44$ V for both M1 and M2 transistors. Thus, the optimized sizes are: $W_1 = 64.0$ μm, $W_2 = W_3 = 200.0$ μm, $L =$ 60 nm, $R_L = 150$ Ω, and $C_L = 3$ pF. The components of the bond wire and pad modeling are $R_{BOND} = 0.5$ Ω, $C_{BOND} =$ 200 fF, $L_{BOND} = 1$ nH, $R_{PAD} = 0.2$ Ω, $C_{PAD} = 200$ fF, $R_2 =$ 12.0 kΩ, and $C_2 = 30$ pF.

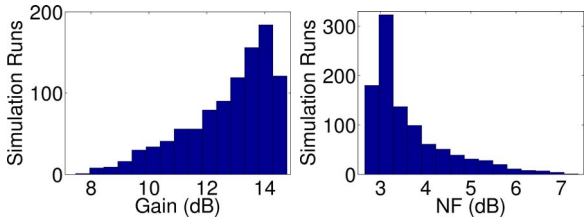
First, the BLIXER design example was simulated obtaining the typical performance for different RF-input-signal frequencies: 1.0 GHz, 2.4 GHz, and 5.0 GHz. The simulation results of the typical circuit are summarized in Table II and they are coherent with the WLAN/WiMAX RF front-end specification.

Table II
THE BLIXER SIMULATION RESULTS: TYPICAL PERFORMANCE.

Frequency (GHz)	1.0	2.4	5.0
Power (mW) Consumption	5.55	5.56	5.59
Gain (dB)	13.5	13.5	14.3
NF_{max} (dB)	4.0	4.5	5.3
IP3 (dBm)	4.4	3.4	-0.73
S11 (dB)	-17.6	-15.4	- 13.3

Subsequently, the BLIXER design example was simulated obtaining the variability of the Gain (Figure 4(a)) and NF_{max} (Figure 4(b)) performances. We present in Figure 4 the results of a 1000 points of Monte Carlo simulation of the fresh BLIXER for the 1.0 GHz of input-signal frequency. The simulated result shows that 96.4 % of the simulation runs have Gain > 10.0 dB, and 92.1% of the simulation runs have NF_{max}< 5.0 dB. Therefore, both performances did not lead the BLIXER to drop

out of the specifications despite the integrated process variation and mismatch.



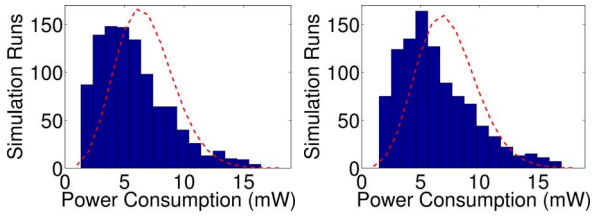
(a) (b)

Figure 4. A 1000 points Monte Carlo simulation of the fresh BLIXER (a) for the Gain and (b) for the NF_{max} performances at 1.0 GHz of input-signal frequency.

In order to characterize the BLIXER ageing degradation, the power consumption (P) will be evaluated. We propose to evaluate the power consumption by 1000 points of Monte Carlo simulation of the fresh BLIXER and the 30 years old stressed BLIXER. Firstly, we obtained the model library for the 30 years aged BLIXER using the typical integrated process parameters. Next, we did a 1000 points Monte Carlo simulation of the (presented in Figure 5(a)) and of the 30 years aged BLIXER using the aged model library (presented in Figure 5(b)). The mode of the fresh BLIXER histogram is 4.2 mW. The mode of the 30 years aged BLIXER histogram is 4.4 mW. Then, we fitted a Poisson distribution for 99.9% of confidence, described by the probability density function

$$f(P;\lambda) = \frac{\lambda^P e^{-\lambda}}{P!}, \tag{13}$$

and we found $\lambda_{fresh} = 5.8$ mW and $\lambda_{aged} = 6.3$ mW. As expected, the bias voltages chosen will lead to an ageing degradation much lesser than 2 % checking the Figures 1(a) and 1(b). Therefore, the performance ageing degradation of the BLIXER is negligible.



(a) (b)

Figure 5. A 1000 points Monte Carlo simulation (a) of the fresh BLIXER and (b) of the 30 years aged BLIXER power consumption using the obtained model library.

VI. Conclusions

In this work, we proposed a reliable synthesis methodology using the circuit design equations to obtain an early estimation of the circuit performance ageing. Thus, the CMOS 65 nm transistor ageing was characterized, and the sensible circuit bias conditions identified. The HCI can be avoided reducing the time in which the transistors are in strong inversion, controlling the V_{GD} and the V_{GS}. In order to increase the circuit reliability and also to achieve the desired performance, the required circuit bias is $V_{DS} = 0.4$ V and $V_{GS} = 0.44$ V.

The simulation results of the typical circuit are coherent with the WLAN/WiMAX RF front-end specification. Despite the integrated process variability and mismatch, we observed that 96.4 % of the simulation runs have Gain > 10.0 dB, and 92.1% of the simulation runs have NF_{max}< 5.0 dB, and they did not lead the BLIXER to drop out of the specifications. Moreover, the BLIXER ageing degradation is negligible according to the fitted Poisson distribution of the power consumption for 99.9% of confidence.

Therefore, simple circuit design equations can help the designer in order to early estimate and reduce the performance ageing, identifying the required reliable circuit bias and sizing. Going further, we can say that the synthesis methodology proposed and developed for a RF front-end design can be exploited in different AMS/RF circuits and also generalized for a single bottom-up reliable-system design approach.

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