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1.4 V and 300 nA UHF Passive RFID Voltage Regulator

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Abstract—UHF passive RFID tags have become a natural option for long distance identification (few meters) as warehouse monitoring and vehicles control access. However, ultra-high frequency and long distance identification implies in very low received power. In order to achieve low power and reliability, a 1.4 V and 300 nA UHF passive RFID voltage regulator was designed in 130 nm CMOS. According to electric simulations of TT corner, we found a voltage regulation settling time smaller than 1 ms for a temperature coefficient of 220 ppm/°C. The voltage reference variability is $\mu = 712$ mV and $\sigma = 45$ mV, estimated by a 1k points MC electric simulation. Finally, we found a PSRR smaller than -30 dB at 100 Hz, 27°C.

I. INTRODUCTION

Radio-frequency identification (RFID) has become widely used for close by applications as: electronic keys, supply-chains management, monitoring, and security. However, UHF RFID tag working in frequencies between 860 MHz to 960 MHz, and 2.4 GHz is more suitable for long distance identification (few meters). Long distance identification is important for example in warehouse monitoring, and vehicle control access applications. Most of RFID tags are battery-less circuitry, due to its low cost and small chip area. Passive RFID tags convert electromagnetic radiation into power supply, usually via a power management front-end (rectifier, regulator and power-on reset circuit - POR), an RF front-end (demodulator and retromodulator), and a digital circuitry (clock generator, baseband processor and memory) [1].

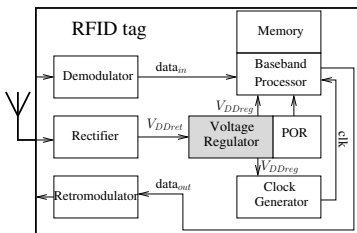


Figure 1. UHF RFID passive tag block diagram: illustration.

According to Friis formula [2]

$$P_R = P_T G_R G_T \left(\frac{c}{4\pi f d} \right)^2, \quad (1)$$

the received power (P_R) available for the power management front-end is shrunk in UHF RFID high frequency (f) and long distance (d) applications. Such a small power (few micro-Watts)

[3] is due to limitations on transmitted power (P_T), receiver and transmitter antenna gains (G_R and G_T). Therefore, the available load current to drive RF front-end and digital circuitry operating with $V_{DD} \approx 1.4$ V shall be only few micro amps. The main design challenge is designing high-efficiency power management front-end and achieving nano-power consumption (nano-amperes of quiescent current). Moreover, the regulator should provide a stable supply voltage, and not being affected by temperature and process variations.

A 1.4 V and 300 nA voltage regulator designed in 130 nm CMOS technology is proposed in this work. To aim low power and high reliability, the voltage regulator design considerations are highlighted according to a system analysis. We present a complete transistor sizing methodology in order to achieve power consumption and reliability specifications. Further, the voltage regulator performance is verified with electric simulations.

This paper is organized as follows. Section II presents UHF passive RFID voltage regulator analysis in power consumption (detailed in Subsection II-A), and reliability (detailed in Subsection II-B) points of view. Section III highlights the design considerations and the transistor sizing methodology to achieve power consumption and reliability specifications. Section IV shows the electric simulation results verifying the power consumption and reliability objectives. The conclusions are presented in Section V.

II. VOLTAGE REGULATOR ANALYSIS

A temperature-compensated regulated voltage ($V_{DDreg} \approx 1.4$ V) is generated by the linear series regulator, represented in the Figure 2. Such a circuit should regulate a rectified voltage (V_{DDret}) using a PMOS switch (M_S) controlled by the difference between a temperature-compensated reference voltage (V_{ref}) and a half V_{DDreg} using error amplifier. The voltage $V_{DDreg}/2$ is obtained by a high-impedance DC voltage divisor. According to CMOS 130 nm reliability guidelines, a limiter circuit guarantee $V_{DDret} < 3$ V.

A. Power Consumption Analysis

The main challenge for a voltage regulator design is achieve a low power consumption, which means a negligible quiescent current in comparison to the load current. Considering P_R equals to the minimum wake-up power and having a maximum load impedance an UHF RFID passive tag represented in Figure 1, we obtain a load current of 8 μ A for $V_{DDret} > 1.6$ V [4] and a communication range from 6 m to 8 m [3]. A negligible

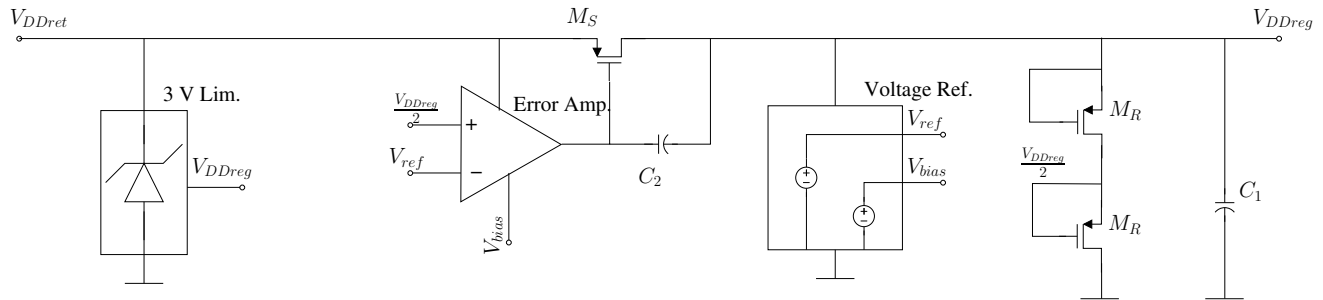


Figure 2. Voltage regulator circuit: illustration.

quiescent current shall be at least ten times smaller than the load current. Thus, the voltage regulator quiescent current have to be less than 800 nA at the worst case of temperature- and process-variation. A worst case of temperature- and process-variation is at FF process corner and 80 °C, hence we assume a quiescent current of 300 nA at TT process corner and 27 °C.

In order to share the power consumption budget, we have determined a strategy to give more current budget to the passive DC voltage divisor. Such a circuit is limited by the maximum resistance feasible using biased MOS transistors. For a $V_{DDreg} \approx 1.4$ V, the quiescent current should be 200 nA guaranteeing a high-impedance DC voltage divisor. The second power hungry circuit is the 3 V limiter. In order to avoid the more than 100 nA leakage current in the limiter, we decided to shut off the limiter while the UHF RFID passive tag is consuming the load current under V_{DDreg} . With the implementation of the shut off switch (see Subsection III-D), we are able to set a 40 nA quiescent current.

An important quiescent current is required for the voltage reference due to the temperature compensation. The error amplifier required for the voltage regulation (see Figure 2) and the temperature compensation (see Figure 3) should have moderate DC gain and low frequency operation constraints. Therefore, we optimized the error amplifier quiescent current in 10 nA to be enough for proper operation. Taking into account the error amplifier quiescent current in the voltage reference budget, we set a 50 nA quiescent current to such a circuit. The total quiescent current is 300 nA.

Such a low quiescent current will be only achievable if the transistors are biased in subthreshold region. This bias region is characterized by a very low charge density in the transistor channel. The 130 nm CMOS technology has 1.5 V as standard supply voltage. Thus, such a very low charges density is only feasible if the transistor length is increased and the V_{GS} is reduced. Hence, we will design the voltage regulator assuming the start point: $L = 20 \mu\text{m}$ and $V_{GS} \approx 300$ mV.

B. Reliability Analysis

The second major issue on voltage regulator design is guaranteeing the required performance despite reliability degradation. The voltage regulator characteristics will be most degraded by temperature variation. Thus, an UHF RFID passive tag should be temperature compensated from -20 °C to 80 °C range. The voltage reference have to provide such temperature compensation (explained in Subsection III-A).

The process variation cannot be compensated for the voltage regulator topology chosen. Such a circuit has no process variation compensation because it may increase the quiescent current over the specification stabilished on power consumption analysis. The voltage reference has the highest sensitivity to process variation caused by the temperature compensation solution (see Equation (3)). For a UHF RFID passive tag, few millivolts of V_{DDref} variation are negligible and such a variation should be verified by voltage reference Monte Carlo (MC) simulations.

The physical phenomena mostly responsible for the ageing degradation in active devices are: Hot Carrier Injection (HCI), Bias Temperature Instability (BTI), and Time Dependent Dielectric Breakdown (TDDB). Both HCI and BTI degradations are increased by high bias stress, however the hypothesis of $V_{GS} \approx 300$ mV leads to a small enough bias, reducing the stress. BTI degradation is also increased by high temperature, but the maximum 80 °C stress implies in not significant temperature stress. Thus, HCI and BTI ageing can be neglected for the voltage regulator if is guaranteed the low bias and moderate temperature [5].

Otherwise, TDDB degradation is more significant while the M_S transistor (see Figure 2) is delivering a small current due to high electric fields between its terminals. To assure a reliable M_S , we should choose a high voltage transistor and design it big enough reducing the electric field. Such an option, guarantee a low TDDB probability on steady state operation, but transient spurs may still breakdown the transistor oxide. Thus, we decided to design a 3 V limiter securing the voltage regulator during transient phase. Moreover, the limiter is shut off when $V_{DDreg} \approx 1.4$ V as explained in Subsection II-A.

III. VOLTAGE REGULATOR DESIGN

The voltage regulator (presented in Figure 2) is designed to achieve $V_{DDreg} \approx 1.4$ V with a quiescent current of 300 nA at TT process corner and 27 °C. Due to reliability constraints, we designed M_S transistor using high-voltage option and sizing of $W/L = 20 \mu\text{m}/2 \mu\text{m}$. The design considerations for its building blocks' design are presented in the following subsections. The final optimized transistors' sizes are shown on Table I.

A. Voltage reference

Figure 3 presents the voltage reference circuit [6]. Designed for -20 °C to 80 °C temperature range, the V_{ref} temperature compensation is obtained while biasing the active load (M_{5-7}) with a controlled current. Such a current is obtained from

a current mirror feedback (M_{1-5}) and the error amplifier, presented in Subsection III-B.

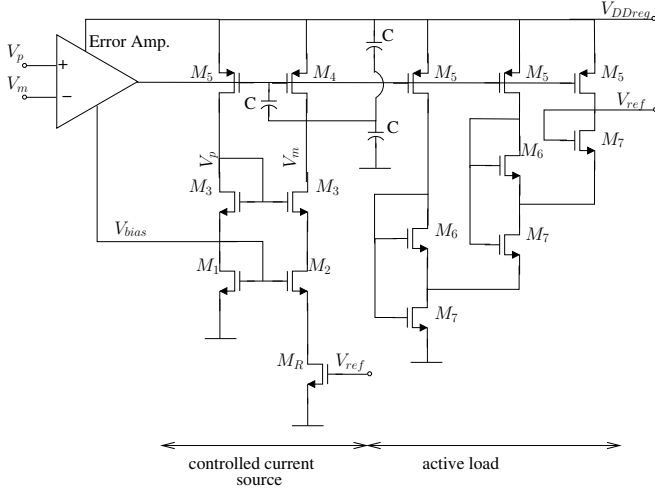


Figure 3. Voltage reference circuit (start-up circuit not shown): illustration.

The active load (M_{5-7}) provides a reference voltage given by

$$V_{ref} = 3V_{GS7} - 2V_{GS6}. \quad (2)$$

Biased in sub-threshold region, such transistors have temperature dependence on threshold (V_{th}) and thermal (V_T) voltage with opposite signs. K. Ueno et al. [6] have shown that the V_{ref} temperature compensation is obtained when

$$V_{ref} = V_{th} \text{ at } T = 0 \text{ K}. \quad (3)$$

Moreover, Equation (3) is satisfied when $W_6 \gg W_7$ for M_{6-7} biased in sub-threshold region [6].

The temperature compensated V_{ref} was obtained estimating V_{th} at $T = 0 \text{ K}$ for standard 130 nm NMOS transistors. Simulating NMOS transistors with width between $1 \mu\text{m}$ and $3 \mu\text{m}$, we are able to evaluate the V_{th} temperature dependency by a linear regression

$$V_{th} = A_1 T + A_2, \quad (4)$$

where $A_1 = -0.96404 \text{ mV/K}$ and $A_2 = 664 \text{ mV}$ with an estimation error of 5 mV for 3σ . We assumed $V_{th} = 664 \text{ mV}$ and M_{1-2} scale equals to five as a start design point. The final optimized transistors' sizes are shown on Table I for an estimated quiescent current lesser than 50 nA , and $V_{th} = 707 \text{ mV}$ at $T = 27^\circ \text{C}$ and TT corner. The capacitor ($C = 8.5 \text{ pF}$) is designed to achieve a stable V_{ref} with at least -30 dB of power supply rejection ration (PSRR) and also guarantee a settling time smaller than 1 ms . The start-up circuit (not presented here) was designed with minimal transistor sizing [6].

B. Error amplifier

The error amplifier is a simple NMOS differential pair (M_1) and a PMOS active load (M_2). The voltage regulator control require at least 50 dB of DC gain and a quiescent current budget lesser than 10 nA . For simplicity, the amplifier current source (M_3) was designed using bias voltage available from the reference voltage circuit (V_{bias}) estimated on 300 mV . The

optimized transistors' sizing is presented in Table I for the required compensation capacitance of $C_2 = 6.5 \text{ pF}$.

C. High-impedance DC voltage divisor

The high-impedance DC voltage divisor (presented in Figure 2) was designed to feedback $V_{DDreg}/2$ with a 200 nA quiescent current for $V_{DDreg} \approx 1.4 \text{ V}$. Thus, the equivalent resistance required is $6 \text{ M}\Omega$. In order to filter V_{DDreg} , we have chosen a cut-off frequency about 50 kHz , which leads to a capacitance of 0.6 pF . For the required resistance, the PMOS transistor sizing ($W_R/L_R = 0.5 \mu\text{m}/20 \mu\text{m}$) is obtained using a simulation optimized design.

D. 3 V Limiter

Figure 4 shows the 3 V limiter designed to be able to drain the load current ($8 \mu\text{A}$) while the voltage regulator is during transient stabilization phase and before a power-on-reset pulse (see Figure 1) which enable the charge circuit. In order to limit V_{DDret} , M_3 transistor should have a large enough width. Increasing M_3 width also increases the leakage current which might turn the quiescent current over the specification. To reduce the quiescent current, we decided to implement M_6 shutting off the M_{1-2} current mirror when the voltage regulator achieve the V_{DDreg} steady state and the current is delivered to the load. The optimized transistors' sizing is presented in Table I

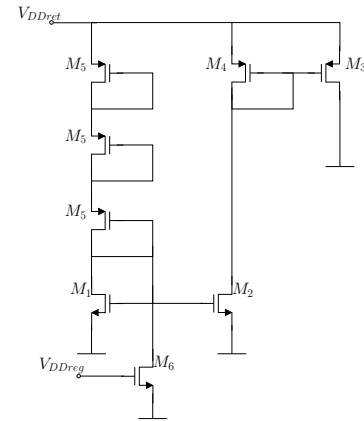


Figure 4. 3 V Limiter circuit: illustration.

Table I
VOLTAGE REGULATOR DESIGN: TRANSISTORS' SIZING.

| Voltage Reference | M_1 | M_2 | M_3 |
|---------------------|-----------|-----------|-----------|
| $W/L (\mu\text{m})$ | 1/20 | 5/20 | 20/20 |
| | M_4 | M_5 | M_6 |
| | 5/20 | 1/20 | 30/20 |
| | M_7 | M_R | |
| | 0.4/20 | 15/20 | |
| Error Amplifier | M_1 | M_2 | M_3 |
| $W/L (\mu\text{m})$ | 3/20 | 0.5/20 | 0.5/20 |
| 3 V Limiter | M_1 | M_2 | M_3 |
| $W/L (\mu\text{m})$ | 0.15/0.13 | 0.15/0.13 | 6/0.13 |
| | M_4 | M_5 | M_6 |
| | 0.15/0.13 | 0.15/0.13 | 0.15/0.13 |

IV. SIMULATION RESULTS

We have designed a voltage regulator circuit, using 2-poly, 4-metal, and optional high-voltage transistor 130 nm CMOS process, and BSIM3 (V3.2) electric simulation model. Figure 5 shows the voltage regulator transient electric simulation at 27°C and TT corner. We found a settling time smaller than 1 ms and a quiescent current smaller than 300 nA for $V_{ref} = 707$ mV and $V_{DDreg} = 1.38$ V. Such power consumption optimization reveals promising results with a quiescent current a half smaller than previous works, but it is also expected a worse output voltage precision as a trade-off [1].

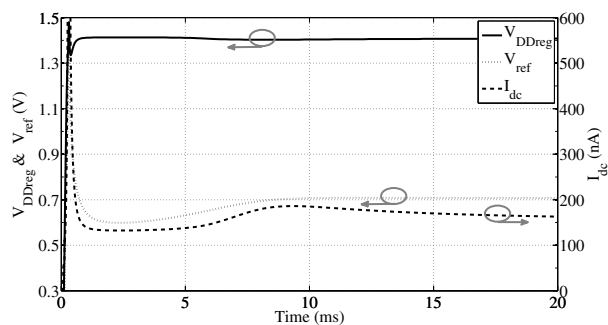


Figure 5. Voltage regulator electric simulation for 27°C and TT corner.

The circuit temperature compensation is electric simulated (presented in Figure 6) for -20 °C to 80 °C temperature variation and different process corners variation (TT - no mark, FF - o mark, SS - > mark). We found a V_{DDreg} temperature coefficient of 220 ppm/°C, 270 ppm/°C, 30 ppm/°C; and a V_{ref} temperature coefficient of 148 ppm/°C, 137 ppm/°C, 195 ppm/°C for TT, FF, and SS corners respectively. The maximum quiescent current is 268 nA, 746 nA, and 127 nA for TT, FF, and SS corners respectively. Such results validate the temperature compensation worsening as a trade-off to have a negligible quiescent current and the design hardship of Equation (3) for 130 nm CMOS technology.

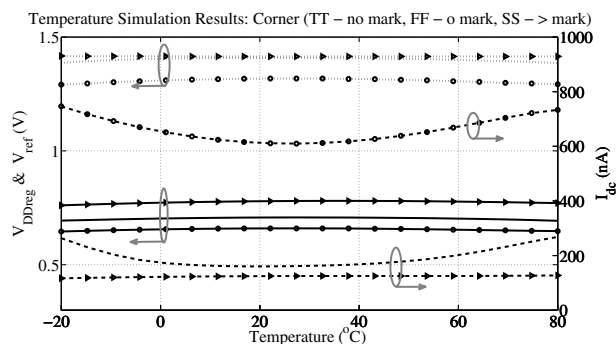


Figure 6. Voltage regulator electric simulation under temperature variation (TT - no mark, FF - o mark, SS - > mark).

The process variation is responsible for V_{ref} variability observed during corners simulation. To characterize such variability, we evaluated a 1k points MC electric simulation of the voltage reference circuit. We found $\mu = 712$ mV and

$\sigma = 45$ mV for a normal distribution with 99 % of confidence. Such variability is negligible for a UHF passive RFID application.

Figure 7 presents the voltage regulator PSRR electric simulation for different process corners (TT - no mark, FF - o mark, SS - > mark). By different process corner simulations, we found a PSRR smaller than -30 dB at 100 Hz, 27°C, $V_{DDreg} \approx 1.4$ V, and a expected RFID circuit load (200 kΩ and 20 pF). Such PSRR is suitable for a UHF passive RFID application.

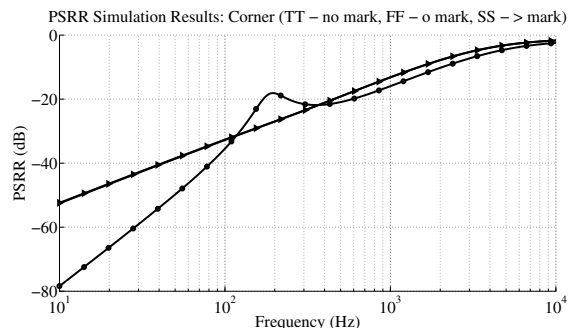


Figure 7. Voltage regulator PSRR electric simulation for different process corners (TT - no mark, FF - o mark, SS - > mark).

V. CONCLUSIONS

A 1.4 V and 300 nA UHF passive RFID voltage regulator was designed in 130 nm CMOS. According to electric simulations at TT corner and 27 °C, we found a voltage regulation settling time smaller than 1 ms for a temperature coefficient of 220 ppm/°C. The voltage reference variability is estimated by a 1k points MC electric simulation achieving $\mu = 712$ mV and $\sigma = 45$ mV. Finally, we found a PSRR smaller than -30 dB at 100 Hz. Such results validate the voltage regulator for a UHF passive RFID application according to the power consumption and reliability specifications. Promising results have been found for power consumption optimization in comparison to previous works, however the temperature compensation worsening is a trade-off of such optimization [1], [6].

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