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### 3. Protecting Mixed-Signal Technologies Against Electrostatic Discharges: Challenges and Protection Strategies from Component to System.

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**Abstract:** Mixed-signal technologies such as smart power technologies are used in demanding applications such as the automotive one. In this application, one of the very stringent requirements concerns the robustness to electrostatic discharges (ESD) that still constitutes one of the major causes of re-design and field returns. In this chapter, we review the challenges that have to be tackled both at chip and system levels. With the help of simple examples, we demonstrate that a global ESD protection strategy approach based on efficient predictive modeling is key to reach the goal of zero ppm failure.

#### ***3.1 Introduction***

In the automotive industry, complex electronic systems are developed to enable advanced remote applications (such as airbag control, antilock braking systems, relay drivers, transmission, cruise controls,...) that require mixed-signal technologies and more particularly, smart power

technologies. In these applications, environment is quite severe in terms of temperature and types of stress (EMC, ESD, load dump...) whereas reliability is critical to ensure the safety of the vehicle with a drastic objective of zero ppm failure. Regarding ESD protection, requirements are much more demanding than in consumer applications with at least 2kV HBM and specific pins required to withstand up to 15 kV contact discharge and 25 kV air discharge. Designing ESD protections in smart power technologies is thus very challenging. In this chapter, we will review these challenges and give some important design guidelines and methodologies for efficient ESD protection both at chip and system levels.

### ***3.2 ESD Qualification Techniques***

Automotive qualification stress tests for integrated circuits are defined in the AEC-Q100 (Automotive Electronics Council) documents [1]. They include ESD test requirements performed at the Integrated Circuit (IC) level. Human Body Model (HBM) [2] and Charged Device Model (CDM) [3] are now the standards currently used for ESD qualification of ICs. Machine Model (MM) standard [4] that was originally created for automotive applications is now abandoned. Each standard defines a specific dynamic current waveform to be injected to the IC pins. For each type of waveform, a dedicated model specifies a capacitor that is preliminarily charged and a discharge network, generally a series resistor [5]. In the case of HBM and MM stress, the equivalent capacitor that is charged is a human or a machine, respectively. In the case of CDM stress, this is the IC itself that is initially charged and then discharged by contact with a conductive surface. The CDM current depends on the equivalent capacitance of the whole die that increases with the size of the package. To this simple model, parasitic elements (RLC) need to be added to correctly represent the actual dynamic behavior of the stress.

Figure 3.1 (a) presents the equivalent electrical circuit that can represent the various waveforms

of HBM, MM or CDM stress by using the related values of the parasitic components [6]. These values are summarized in Table 3.1. Figure 3.1 (b) compares the various waveforms of HBM, MM and CDM stress for the respective standard level required for consumer products.

Model	$C_{ESD}$ (pF)	$R_S$ ( $\Omega$ )	$L_S$ ( $\mu H$ )	$C_S$ (pF)	$C_T$ (pF)
<b>HBM</b>	100	1500	5	< 5	< 30
<b>MM</b>	200	0	0.5/2.5	0	< 30
<b>CDM</b>	10	10	0.01	0	0

Table 3.1: Characteristics of HBM, MM and CDM discharge models.

Pins of the device under test (DUT) are classified in two categories: supply pins, and no supply pins. ESD zap between pins and groups of pins are applied. Combinations depend on the pin category. Typical maximum required HBM stress levels are 1kV to 2kV. Common requirements for CDM are 250V and it can be up to 500 V for all pins and 750V for corner pins.

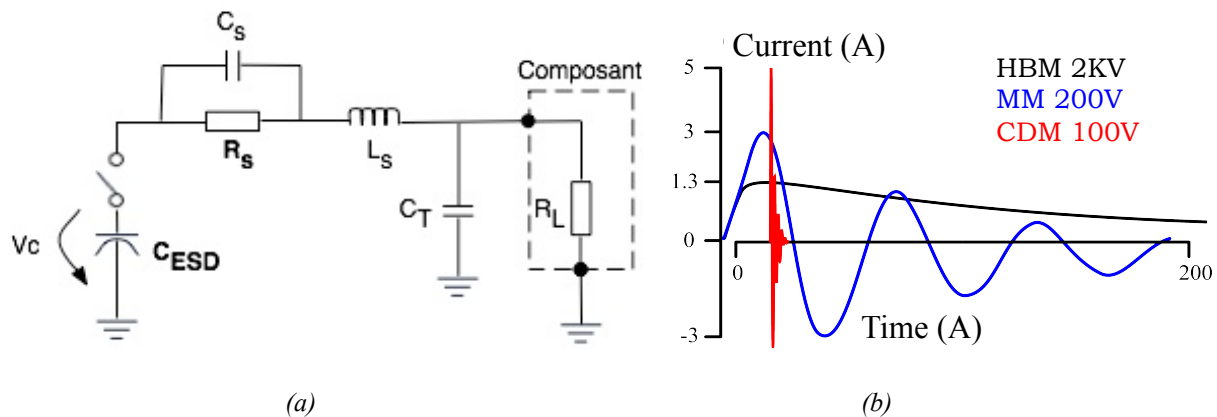


Figure 3.1: Equivalent RLC electrical schematic (a) and resulting waveforms (b) for HBM, MM, CDM models.

Other standards are defined at system level (vehicle) such as IEC61000-4-2 [7], and the ISO10605 [8] that is more dedicated to automotive systems. In this case, an ESD zap is applied at the system level, for example at a connector, with an ESD generator (Gun), and the current is diverted through the different elements of the printed circuit board (PCB). A residual current of this stress can reach the ICs and generates permanent damage. There are multiple test setups, powered, unpowered conditions, contact discharge, air discharge, with several types of ground connections. For these standards, the same equivalent electrical circuit as in Figure 3.1 applies. For IEC61000-4-2 standard, the discharge is realized with a gun RC module of 150pF and 330 ohms. For the automotive ISO10605 one, all combinations of 150pF and 330pF capacitors with

330 ohms and 2 kilo-ohms resistors are possible. This greatly impacts the dynamic behavior of the stress waveforms as reported in Figure 3.2.

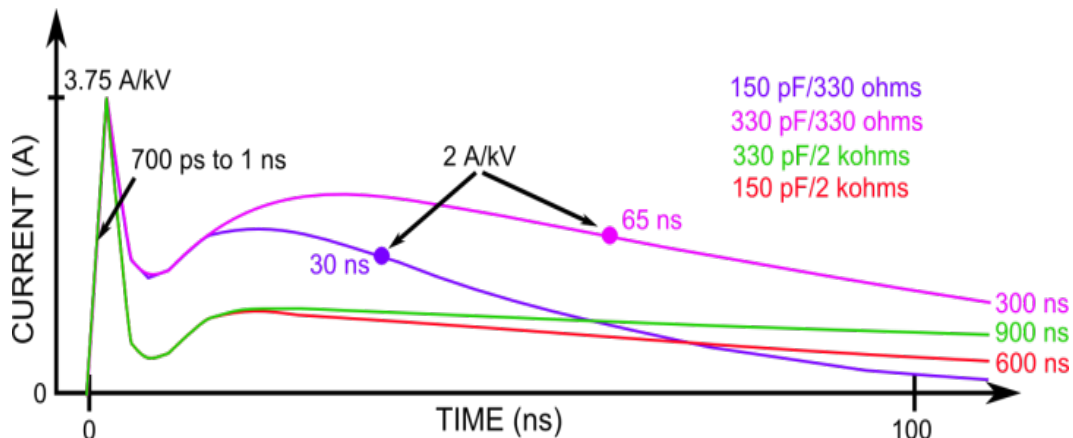


Figure 3.2: Comparison of various waveforms required by ISO10605 standard.

For a system, different levels of functionality are required after or during the ESD. For the most severe requirements all functions should operate normally during and after the ESD stress.

### 3.3 Investigation Methodologies

#### 3.3.1 Electrical Characterization

Standard ESD tests at IC level such as HBM, MM or CDM are not suitable to help IC designer optimize its ESD protection strategy. Indeed these tests characterize the ESD robustness level of a given protection but do not provide crucial data such as threshold voltage  $V_{T1}$ , holding voltage  $V_H$  if a snapback occurs, or on-resistance during ESD stress. The maximum current capability  $I_{T2}$  of the protection can be extracted from its HBM robustness but the relation between these two values is not always verified.

All these parameters are necessary to check if the protection is compliant with the ESD design window. Today, the integration of these parameters is not standardized yet. But an approach is ongoing to incorporate ESD parameters in standard models like IBIS models already used in the Electro-Magnetic Compatibility (EMC) field.



To characterize the behavior of the device regarding faster ESD event like CDM, an extension of TLP setup have been proposed [10]. Very-Fast TLP (VF-TLP) is based on the same architecture as TLP, but the generated pulse is shorter (1 to 5 ns) using a smaller transmission line. The current and voltage measurement is more difficult because the incident and reflected pulses are totally separated in the time domain. Post-processing is needed to recalculate the current/voltage value. Also, some hardware solutions exist to merge the pulses using delay line and a combiner. VF-TLP characterizations at wafer level require high bandwidth probes with special care for the ground path. Ground/Signal 50 $\Omega$  probes can be used for the best results but involve a special design of the pad access. Generally VF-TLP allows characterizing ESD protections at higher current level since the pulse is shorter, the power dissipated by the device is smaller. But the state of the device could be different i.e. in TLP the device is in quasi-static mode while during VF-TLP it could be in transient situation.

#### (ii) Overshoot Issues: Gate Monitoring and Transient TLP

Even if the ESD protection exhibits low impedance when turned on, during its triggering an overvoltage can occur due to capacitive effects. Typically this critical phase is a few hundred picoseconds after the beginning of the ESD event. This overvoltage can induce the destruction of the IC. As a result, ESD protection designer should be aware of this phenomenon and take it into account.

One method to check the protection efficiency is to implement a gate monitor [11]. The gate and the source of an nMOS transistor are coupled in parallel with the ESD protection. The drain of the MOS transistor is open but connected to an external pad for functional test. The intrinsic TLP curves of each component are already known. Then a TLP characterization of this association is performed until failure. If the ESD protection is firstly destroyed, there is no overvoltage issue. If

the MOS transistor fails, for a quasi-static voltage higher than its  $V_{T2}$  value, there is no overvoltage issue but this means that the on-resistance of the ESD protection is too high. If the failure quasi-static voltage is lower than the MOS  $V_{T2}$ , we are facing a destructive overvoltage but without knowing its value.

Transient TLP method has been developed to evaluate this over-voltage value [12]. It uses a simplified VF-TLP setup combined to a post-processing technique in order to increase time accuracy. Firstly, RF scattering parameters (DC to 4GHz) of each part of the VF-TLP setup are characterized using a vector network analyzer; this is the calibration step. During transient characterization, the waveform of the incident and reflected pulses are digitized with a high bandwidth oscilloscope. A Fast Fourier Transform (FFT) is then applied in order to convert signals from time domain to frequency domain. The data coming from the vector network analyzer characterization are then used to correct the signals with a complex algorithm. And finally an inverted FFT is processed in order to come back in time domain. With this technique, measurement limitation is coming from the oscilloscope bandwidth (6GHz) and the time resolution is about 60ps, which is enough to estimate the transient overvoltage [13].

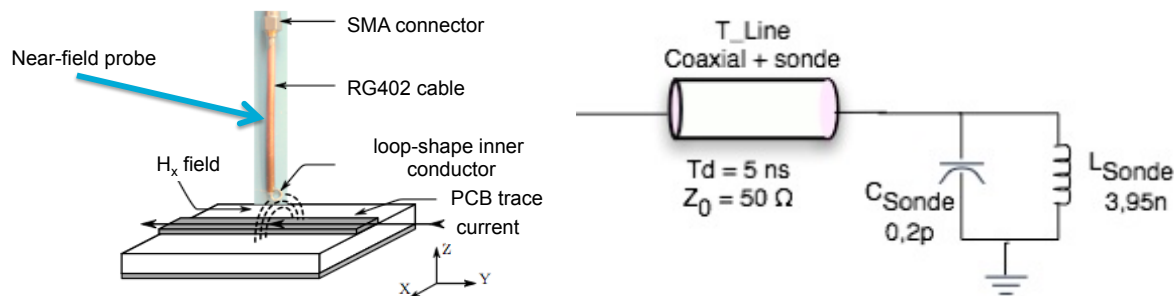
### (iii) Near-Field Scan

One of the main issues when designing ESD protection strategies at system level is to identify the propagation path of an ESD stress within the system and to extract the precise resulting waveform and its impact on the embedded ICs. Near-field scanning is a non-invasive measurement technique based on the use of a magnetic field probe [14]. It allows current monitoring at printed circuit board (PCB) level or even at IC level if the probe is miniaturized.

The same probe as the one used in the EMC standard [15] allows capturing the magnetic field emission while the current propagates. It is made up from a semi-rigid copper coaxial cable



(Figure 3.4). The inner conductor of the coaxial cable is twisted and shorted to the outer shield, thus creating a current loop. Such a probe can be modeled using an inductor and a capacitor to represent the loop and a transmission line to take into account the RG402 high frequency coaxial cable. In terms of transmitted power, it exhibits a pure magnetic coupling effect up to 1 GHz that is mainly inductive. This injection model was already validated in previous works [16].



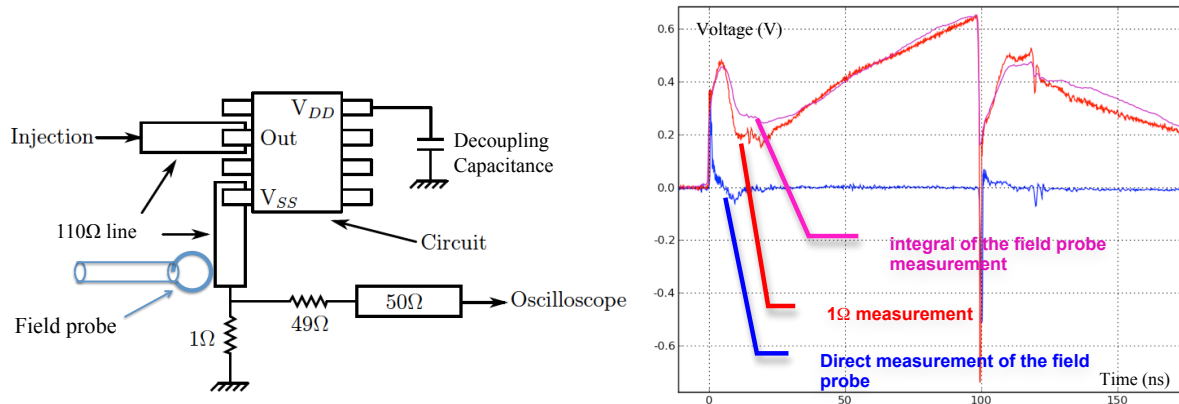
**Figure 3.4: (Left) Homemade magnetic field probe. (Right) Equivalent model of the probe.**

Based on the purely inductive behavior of the probe up to 1GHz, we directly reconstruct the current waveform flowing through the PCB line by integrating the measured magnetic field.

With regard to system level ESD stresses, it turns out that a 1 GHz probe bandwidth is sufficient for low discharge levels (2kV), and integral reconstruction waveform can be used. For high levels (8kV), it is more appropriate to work in the frequency domain by performing a FFT of the probe dynamic measurement, correcting it with the probe frequency response and finally getting the current waveform using an  $\text{FFT}^{-1}$ .

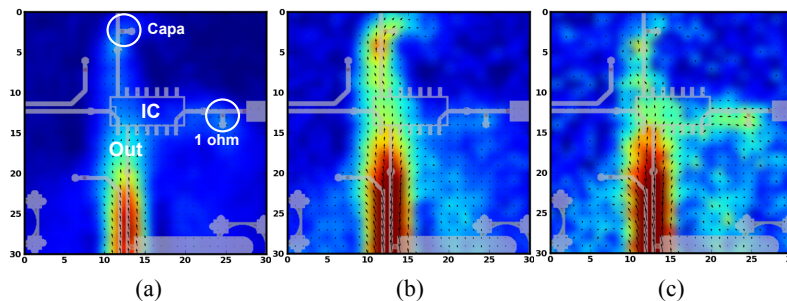
As a validation of this method, we present a measurement comparison with the  $1\Omega$ -resistor method on a simple commercial inverter submitted to the injection of a square current pulse (1A, 100ns) using a VF-TLP tester. The injection is applied to one output pin and current is measured at the ground pin. As shown in Figure 3.5, there is a good agreement between the current measurement obtained by the field probe and the  $1\Omega$ -resistor one. It has to be noticed that the external decoupling capacitance on VDD pin dramatically changes the waveform of the injected

square pulse. Such waveform could not be predicted by the ESD protection strategy of the chip.



**Figure 3.5: Schematic diagram of the test setup for a commercial inverter using 1Ω-resistor and magnetic field probe. Current measurement comparison for a VF-TLP pulse (1A, 100ns) injected into Vout pin.**

To understand how the current of an ESD stress propagates within a system at board level, we developed a near-field scanning system where the field probe is mounted on a 3-axes table with a maximum spatial resolution of 100μm. The TLP generator synchronizes the measurement test bench. Each time a stress is injected into the connector of the PCB,  $H_x$  and  $H_y$  magnetic fields are captured using a 12GHz oscilloscope. By repeating this operation step by step, the scan of the PCB is performed. From the registered data, a movie can be built showing the evolution of the emitted field during an electrical fast transient.



**Figure 3.6: Pictures from the movie of the current propagation into the board: current injection (a), decoupling capacitor absorption (b) and current split between capacitor and 1Ω-resistor (c).**

Figure 3.6 reports three pictures showing the current propagation into the system of Figure 3.5 at

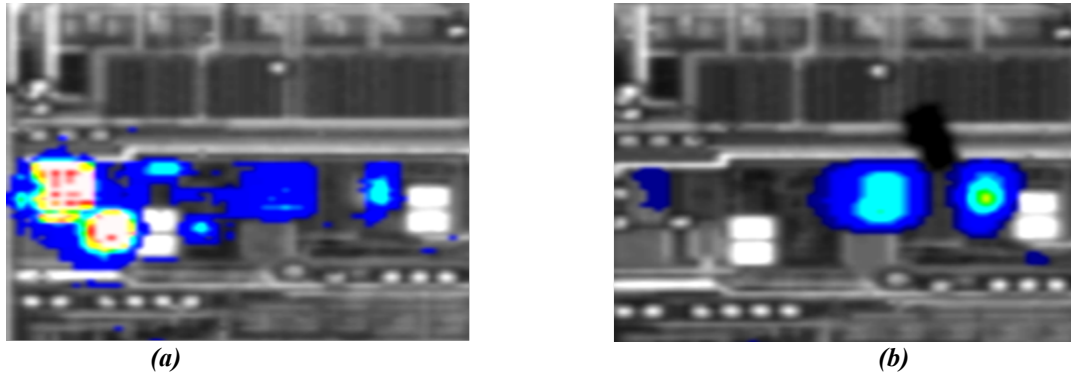
different times and in particular, the impact of the decoupling capacitor. The near-field scanning system is a powerful tool for system level ESD investigation and for understanding the system behavior under different types of stresses.

### *3.3.2 Debug and Investigation Methods*

The simulation of functional failures during ESD events remains very challenging for integrated circuits due to the frequency domain and to the high current injection mechanisms. Hence, the root cause of a functionality loss after an ESD event can be very difficult to understand.

Combining TLP and Emission microscopy (EMMI) can provide good results (Figure 3.7). EMMI is an optical analysis technique used to detect and localize integrated circuit defects. It is non-invasive and phenomena can be observed in real time, integrating the photoemission generated by the IC. Photons are generated during gate oxide defects, polysilicon filaments, substrate damage, junction avalanche, active bipolar transistors, saturated MOS device, ...

Combined TLP + EMMI technique consists in taking a reference picture of the photon emission while the IC is submitted to TLP zap at a level just before a failure occurs. Then, at a higher TLP zap level another picture is taken once a malfunction is detected. Both pictures are compared to identify where the photon activity has changed at blocks or elements levels. Figure 3.7 shows an example with the emission activity of an internal 5V regulator when a TLP pulse is applied on a global pin. Figure 3.7 (a) shows a normal activity of the block whereas Figure 3.7 (b) exhibits the emission change after a “reset” generation.



**Figure 3.7:** *Coupling TLP and EMMI for debugging, InGaAs sensor 20x, 30s integration: (a) TLP injection level below fault generation threshold and (b) TLP injection level increased until the soft failure occurs.*

The analysis of these pictures allowed understanding that the 5V regulated voltage was decreasing until the undervoltage detection, and then creating a reset. After a thorough investigation into schematics and layout, a parasitic coupling on the current reference circuit was identified as the root cause of the failure. This study is detailed in [17].

### ***3.4 ESD Design In Smart Power Technologies***

#### ***3.4.1 ESD Design Window***

The role of ESD devices is the protection of integrated circuits (ICs) not only against any ESD events during manufacturing and assembly but also during the IC operation. An ESD design window defining a safe operating area of the protection device in the IC was proposed to properly optimize its voltage/current characteristics. Figure 3.8 describes the ESD design window with the lower and upper voltage limits. The lower voltage limit is the maximum pin power supply voltage or the maximum pin voltage rating. In contrast, the upper voltage limit is the lowest breakdown voltage of the IC (oxide or junction breakdown of IC devices). With these elements, any designer can develop an ESD structure with specific voltage characteristics between these voltage limits. By this way, the ESD protection scheme provides protection of the IC while being compatible with the electrical pin constraints.

The ESD design window is generally defined at ambient temperature. However, ICs are also required to handle ESD stresses during their operation and temperature in some applications such as the automotive one can be as high as 125°C or even more. An illustration of the impact of temperature on the efficiency of a protection is the case of a MOS power clamp. MOS devices are very sensitive to temperature. Indeed, a MOS power clamp exhibiting 1.74 A failure current and 4.4 Ω on-resistance at 25°C sees its robustness and on-resistance degraded down to 1.34 A and 7.1 Ω at 200°C, respectively [18]. If this temperature behavior is not taken into account, it could induce detrimental effects such as a lower failure current and even could lead to not providing the expected protection due to the non-compliance with the ESD design window. To compensate this effect, the size of the power clamp protection would have to be increased.

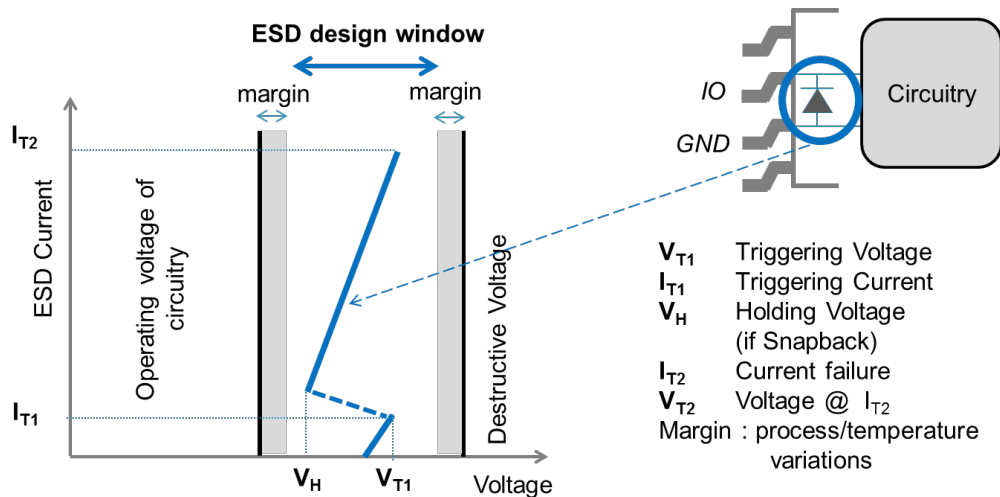
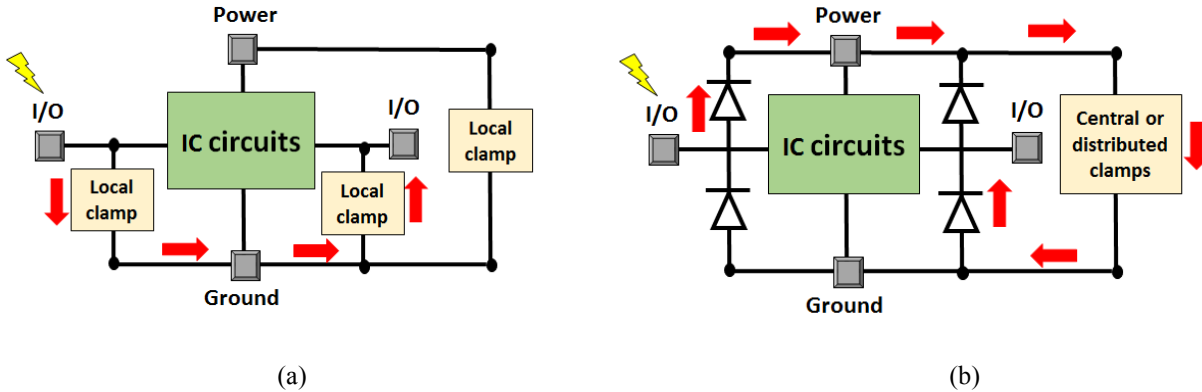


Figure 3.8: ESD design window.

ESD protection strategy placement consists in implementing the appropriate ESD protection structures for a safe ESD discharge current path while providing proper voltage clamping at the I/O pins to be protected. A good protection strategy should provide an efficient current path during any ESD events between I/O and supply pins whereas optimizing ESD protection structures placement to minimize die size.

There are two different ESD protection strategies at any pin: local and distributed. The local ESD protection strategy is the basic technique consisting in placing the ESD protection structure at the pin to be protected. It requires for the protection structure to be bidirectional. This technique presents the advantage to simplify the definition of the ESD architecture placement by using the common metal ground bus around the chip (Figure 3.9 a). It also limits any coupling between the different pins. However, it implies significant design efforts to develop different types of ESD protection structures with multiple I/O or power pins. As a consequence, die size may not be optimized.



**Figure 3.9: ESD protection strategies: local (a) versus distributed (b). In both cases, the arrows indicate the ESD current path for an ESD zap between the two I/Os.**

Conversely, the distributed ESD protection strategy uses diodes to divert any ESD current from any I/O pin to a single or distributed clamps generally placed at the power pins (Figure 3.9 b). Diodes only work in forward mode then conferring a high robustness and requiring small silicon footprint. Design efforts are focused on the clamps at power pins and on the common metal routing for power and ground bus. This strategy has the advantage to reduce the ESD protection development time since design efforts are focused on the power clamp. In addition, since the protection strategy uses active devices from the technology library, it can be easily simulated. However, the use of this technique is limited with the number of voltage levels applied at

different power pins (more than 3). It increases the complexity of bus architecture by increasing additional common metal bus ring connected at different power-pin voltage levels. In addition, this technique cannot be applied for I/O pins isolated from power pins in some cases.

#### *3.4.2 ESD Integrated Protection*

Although in some cases active devices can be self-protected by an appropriate design, this is not generally the case and specific ESD protections have to be implemented even for power devices. A major difficulty of ESD protection design is that it should be done with a small-footprint and free device for a given technology, i.e. it should not involve any extra mask or technology process step. As local protections are placed under the pads, the maximum-targeted surface is equal to the pad one, generally closed to  $100*100 \mu\text{m}^2$ . ESD design specifications involve both high power dissipation and high current density. As a result, snapback ESD clamps are popular bipolar-based protection devices. In addition, since multiple voltage domains could be integrated on the same chip, ESD protections with tunable operating voltage are highly desirable. We will discuss hereafter the main issues for proper ESD device design, their advantages and drawbacks and main use.

##### (iv) Power MOS

The typical ESD protection clamp used from several products is the power MOS transistor. This kind of protection is often self-protected during any transient ESD current event.

This technique uses a high gate resistance between the gate terminal and the source terminal of the N-channel MOS transistor (Figure 3.10). The size of MOS transistor is optimized to get not only a low on-resistance when activated but also to have high capacitive coupling between the drain terminal and the gate terminal for fast activation.

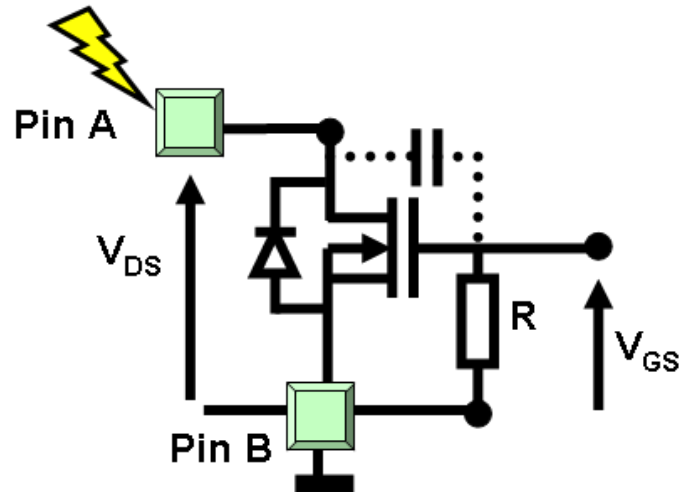


Figure 3.10: ESD clamp – Self protected N-MOS transistor.

The MOS transistor performance protection depends on its area form factor. It was demonstrated that using a specific area configuration of the grounded gate N-MOS transistor provides the best ESD performance [19] [20].

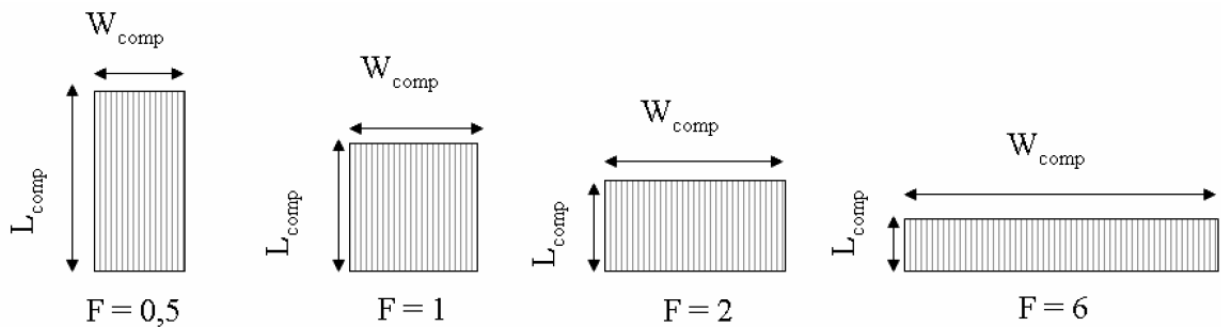


Figure 3.11: Grounded Gate N-MOS transistor.

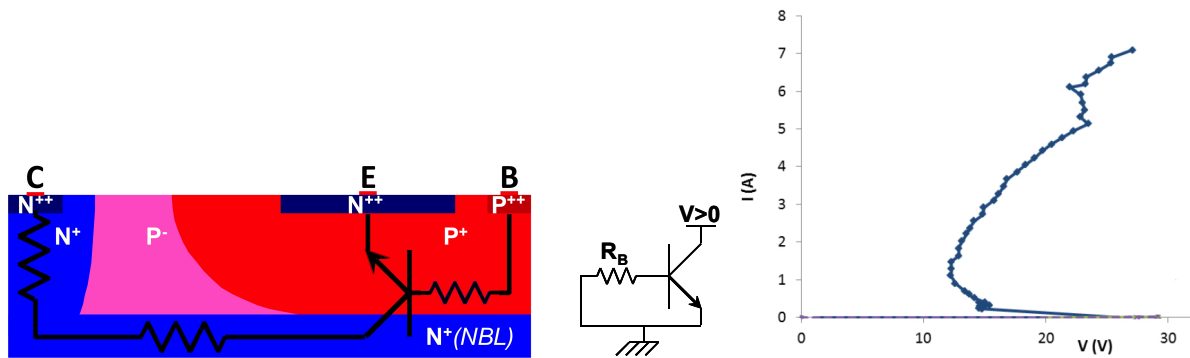
Designing grounded gate N-MOS transistor with  $F=6$  improves by a factor of 3 the HBM ESD performance in comparison with the one designed with  $F=0.5$  (Figure 3.11).

#### (v) NPN-based ESD Protections

The main advantage of snapback bipolar-based devices is related to the conductivity modulation mechanisms [21] that allow drastically reducing their on-resistance and then their silicon footprint. In CMOS technologies, parasitic bipolar transistors intrinsic to MOS structures are used for ESD protection. In the case of smart power technologies, bipolar transistors are part of



the library of active devices. They just need to be adapted for pulsed operation to provide high power dissipation and high current density ( $10^5$ - $10^6$  A.cm<sup>-2</sup>). To this aim, they are generally self-triggered by operating them in conditions of avalanche injection. The resulting high power generation in local regions of the device requires specific design solutions such as proper energy balance inside the device structure and current ballasting implemented via a proper layout using contact diffusion regions and backend metallization.



**Figure 3.12: Grounded-base NPN transistor used as an ESD protection: cross-section (left), electrical schematic (middle) and typical TLP characteristics (right).**

Figure 3.12 shows a typical NPN transistor of a smart power technology that is currently used as a self-biased ESD protection. When the voltage  $V$  on the collector pin increases and reaches the breakdown voltage of the collector-base junction, avalanche current is generated and flows through the intrinsic base resistance ( $R_B$  on schematic). When its value is such that the voltage drop on this resistance is higher than 0.6V, the bipolar transistor turns on and as a result its I-V characteristics undergoes a strong snapback as shown by the TLP curve shown in the same figure. In the case of the protection of high-voltage pins, this strong snapback is an important drawback since it is generally not compliant with the requirement of the ESD design window for a snapback voltage higher than the operation voltage. To cope with this issue, a classical solution is to stack as many NPN structures as necessary in series. This allows increasing the snapback

voltage but concurrently the on-resistance and the silicon footprint. An alternative solution consists in using devices exhibiting a weak snapback or even a no-snapback device.

An avalanche diode could have been an interesting component as a no-snapback protection. A high robustness should be attained given its excellent current uniformity due to a constant breakdown voltage increase with current and temperature. However, the current-induced field modification leads to low  $R_{ON}$  only for structures closed to  $p^+ - i - n^+$  configuration. Otherwise, the  $R_{ON}$  could be extremely high [22] [23].

In bipolar devices, the simplified implicit equation that governs the snapback behavior is the following:

$$\alpha M = 1 + \frac{I_B}{I_E} \quad (1)$$

Where  $\alpha$  is the common base gain (in self-biased configuration), M the multiplication factor,  $I_B$  the current at base contact,  $I_E$  the current at emitter contact.

According to this equation, two methods can be contemplated to increase the holding voltage of a bipolar structure:

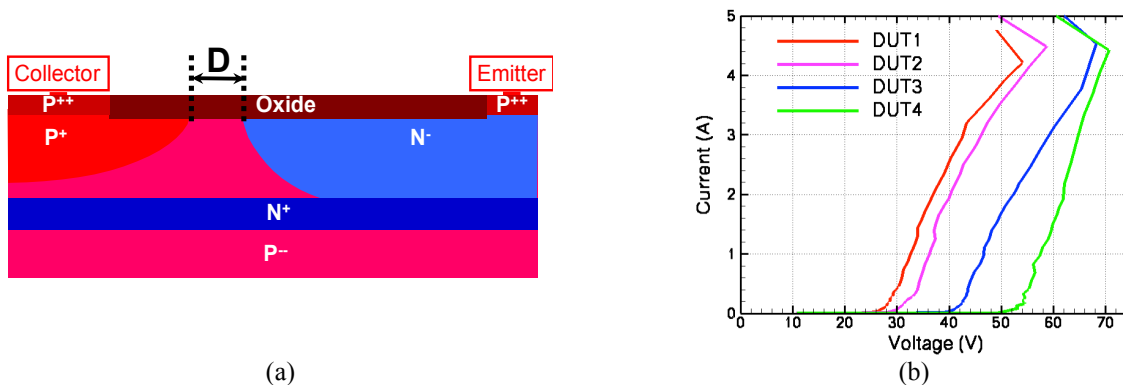
- First, lower the gain  $\alpha$  (in self-biased configuration), to increase the corresponding M value and then the voltage.
- Secondly, use a device with a lower avalanche multiplication factor M.

#### (vi) PNP-based ESD Protections

Using a PNP bipolar transistor instead of a NPN one is an attractive solution. Its gain is generally lower than the NPN one, given the lower holes diffusion coefficient. The multiplication factor is also lower in a PNP than in a NPN, since holes impact ionization coefficient is smaller than the electrons one. The main issue to develop PNP-based ESD protections concerns the reduction of the on-resistance ( $R_{ON}$ ) value, which is intrinsically higher than the NPN one. Two major reasons

explain this difference: firstly, the only available PNP transistor is generally a lateral one then resulting in higher access resistances and secondly, the conductivity modulation mechanisms (beneficial to the  $R_{ON}$ ) are less pronounced in PNP devices. To counterbalance these drawbacks, the following design guidelines can be implemented:

- Use of multifingers interdigitated structures with minimum dimensions for emitter and collector widths without any ballasting.
- Suppression of base contact since PNP devices exhibit a weak snapback or no snapback at all. This allows saving up to 25% silicon area.
- Abrupt collector profile and low base doping to favor high-injection effects.



**Figure 3.13: Optimized PNP-based ESD protection in 0.8 $\mu$ m smart power technology: cross-section (a) and measured TLP characteristics (b). Distance D allows tuning  $V_{t1}$  triggering voltage.**

These design guidelines have been implemented on PNP devices issued from SmartMOS<sup>®</sup> 8 MV smart power technology [24]. Figure 3.13 presents the cross-section a PNP bipolar transistor from the library without base contact and its measured TLP characteristics. For this transistor, distance D allows tuning the triggering voltage of the structure. In the four different cases corresponding to different distances D, the structures do not show any snapback behavior and the triggering voltage value has almost no impact on the failure current, which corresponds to an HBM robustness of about 7kV. Table 3.2 summarizes the main electrical parameters of DUT4

structure. Finally, the leakage current of the PNP without base contact was measured to be lower than one picoAmpere (limit of the measuring set-up) that is compatible with standard leakage specifications.

PNP bipolar transistor (DUT4)					
$V_{d1}$ (V)	$V_{d2}$ (V)	$I_{d2}$ (A)	$R_{ON}$ ( $\Omega$ )	$I_{d2}/S$ (mA. $\mu\text{m}^{-2}$ )	$R_{ON}*S$ (m $\Omega$ .cm $^2$ )
49V	70.7	4.42	4.9	0.28	0.77

Table 3.2: Measured electrical parameters for the PNP-based ESD protection of Figure 3.13. The PNP

bipolar transistor is made up of seventeen 100 $\mu\text{m}$ -long fingers resulting in 15700  $\mu\text{m}^2$  surface.

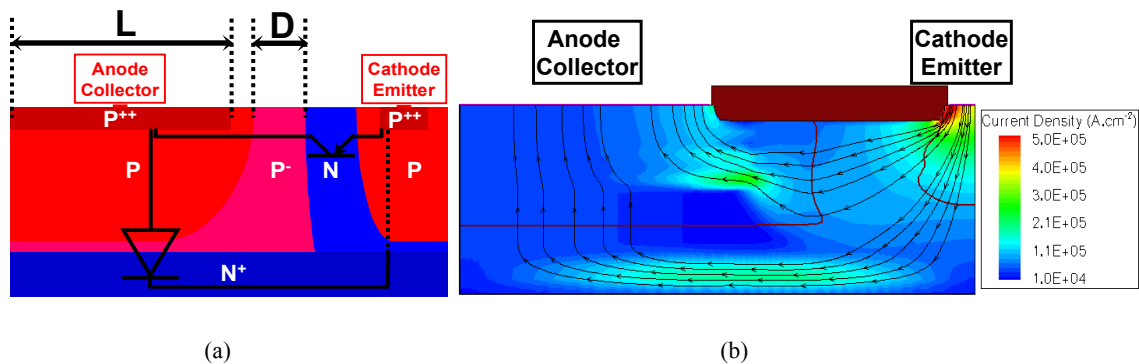


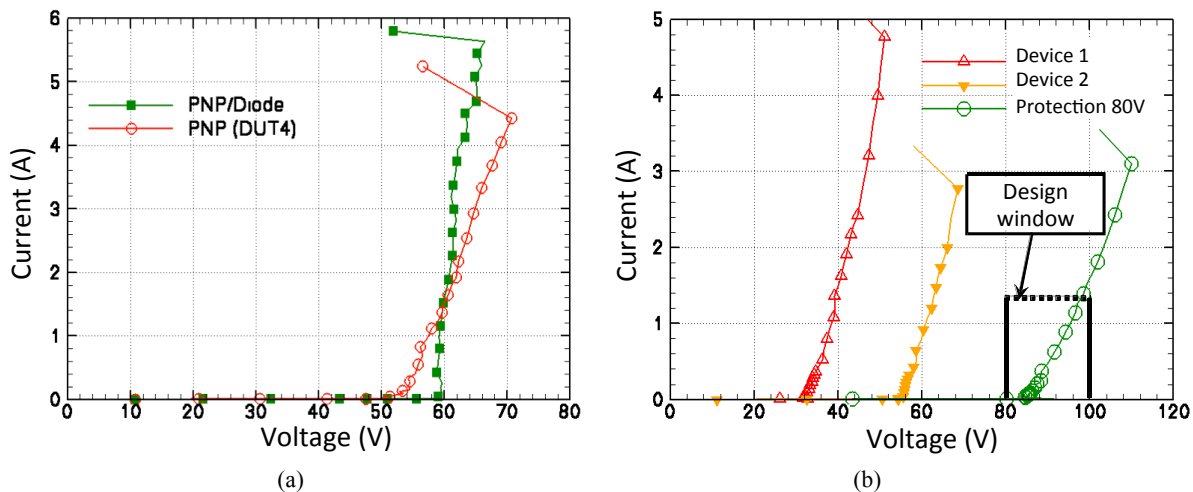
Figure 3.14: Proposed PNP/diode ESD protection: schematic cross-section (a) and TCAD simulation showing the current distribution over the two elements, diode and PNP (b).

To further improve the performance of such PNP-based ESD protection, it is worthy to efficiently couple the intrinsic vertical diode with the lateral PNP bipolar transistor [25]. Figure 3.14 (a) presents the basic principle of the structure. Its optimization requires to first adjusting the voltage triggering of both devices: making them equal provides the best trade-off. As the breakdown voltage of the vertical diode is defined by the doping profile of the different layers, the only way to tune this parameter is to vary the distance  $D$  that defines the collector-emitter PNP breakdown voltage. The second parameter to optimize is the current density flowing in each device: it controls the on-resistance of the global structure. This is achieved by adjusting the width of the anode contact  $L$ . Increasing  $L$  allows significantly decreasing the on-resistance, the optimum being defined by the following factor of merit:

$$F_{RON} = \frac{R_{ON} \cdot S}{V^2} \quad (2)$$

Where  $R_{ON}$  is the on-resistance of the structure,  $S$  its silicon area and  $V$  the clamping voltage. The simulation results of Figure 3.14 (b) show the homogeneous current distribution over both devices in such optimized structure.

Figure 3.15 (a) illustrates the significant improvement obtained with such optimization. The measured PNP/diode having an optimum  $L$  of  $10\mu\text{m}$  and  $10000\mu\text{m}^2$  silicon footprint results in a very low on-resistance of  $1\Omega$  and  $8\text{kV}$  HBM robustness. It was successfully implemented in a commercial circuits to protect an  $80\text{V}$  I/O pin using two stacked PNP/diode devices, one with a  $V_{t1}$  of  $32\text{V}$  and the second with  $V_{t1}=54\text{V}$ . As shown in Figure 3.15 (b), it provided the required robustness of  $2\text{kV}$  HBM ( $\sim 1.3\text{A}$ ) for a silicon footprint of  $21000\mu\text{m}^2$ . This has to be compared with the original implemented protection (NPN stacked with an LDMOS) that required a silicon footprint of  $40000\mu\text{m}^2$  for the same HBM robustness.



**Figure 3.15: PNP/diode experimental results: TLP characteristic comparison with a single PNP for a 5-fingers structure with  $10000\mu\text{m}^2$  footprint (a) and practical implementation for the protection of an  $80\text{V}$  I/O pin of a Power-over-Ethernet commercial circuit (b).**

#### (vii) Silicon Controlled Rectifier (SCR)

Silicon controlled rectifier (SCR) are very attractive devices. Their excellent clamping

capabilities and high ESD robustness allow designing efficient and compact protections [26] [27] [28]. However, their main drawback is that most of SCR-based protections exhibit a low holding voltage  $V_H$  ( $\sim 1.2V$ ), which makes them prone to latch-up and not compliant with the ESD design window. In deep submicron CMOS technologies, the problem is solved since the power supply is below 1V and SCR-based protections are now widely used [29]. In high-voltage technologies, many research studies have been carried out to increase either the holding voltage [30] [31] [32] or the holding current of SCR devices [33] [18]. The holding current of the parasitic SCR is defined by the following parameters and equation [34]:

$$I_H = \frac{\beta_p(\beta_n+1)I_{NW} + \beta_n(\beta_p+1)I_{PW}}{\beta_n\beta_p - 1} \quad (3)$$

Where  $\beta_n$  and  $\beta_p$  are the current gains of the parasitic NPN and PNP bipolar transistors and  $I_{NW}$  and  $I_{PW}$  the currents flowing into the N-well (PNP base) and P-well (NPN base), respectively. In the same way, the holding voltage  $V_H$  is linearly proportional to  $I_H$ .

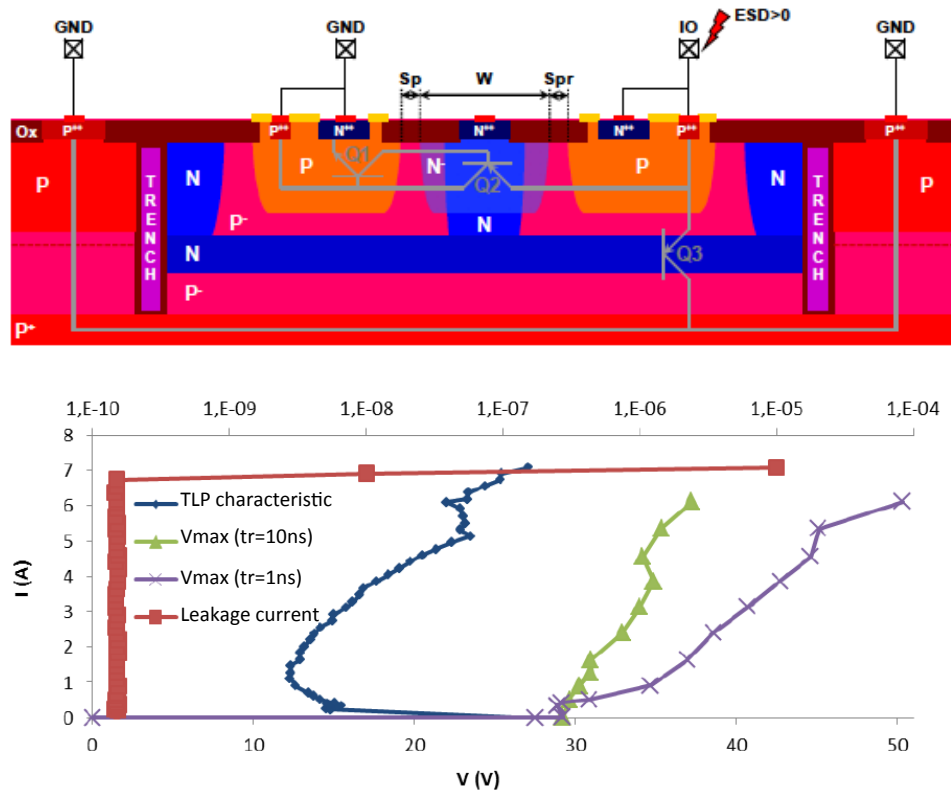
As a result, to increase  $I_H$  or  $V_H$ , two options are available:

- Reduce the current gain of the respective bipolar transistors
- Reduce as much as possible the resistance of the NPN and PNP bases.

The specific design of the bidirectional SCR presented in Figure 3.16 allows achieving a high  $V_H$ : it is made up of two P-wells isolated by a deep  $N^+$  diffusion and an  $N^+$ -buried layer [35] [36]. It is composed of 3 bipolar transistors: a lateral NPN Q1 (P-well as base,  $N^{++}$  as emitter and central deep  $N^+$  as collector), a lateral PNP Q2 whose base is the central deep  $N^+$  and a vertical PNP Q3 (P-well as collector,  $N^+$ -buried layer (NBL) as base and P-substrate as emitter). This protection structure allows the protection against both positive and negative ESD stresses.

Upon a positive ESD stress, this protection is triggered via the self-biasing of the lateral NPN Q1 when the ESD voltage reaches its base-collector breakdown voltage that is defined by the

distance  $S_p$ . Once turned on, both lateral and vertical NPN transistors inject current into the PNP base. As this latter is highly doped, the PNP current gain is very low and as a result induces a high holding voltage (12.5V). In addition, the vertical PNP transistor Q3 provides a secondary current path. Figure 3.16 also presents the TLP characteristics of this device realized in 0.25 $\mu\text{m}$  SmartMOS® technology for a distance  $S_p$  that results in a triggering voltage of 28.9V and a holding voltage of 12.5V. These structures can be stacked to meet different voltage targets.



**Figure 3.16: High holding voltage bidirectional SCR-based ESD protection showing active bipolar transistors under a positive ESD zap (top). Measured TLP characteristics and associated overshoot,  $V_{\text{max}}$ , according to TLP pulse duration (bottom).**

The main issue of a SCR device is the overshoot that can be induced before its triggering. In the graph of Figure 3.16, is also plotted the overshoot under two different TLP pulses with 10ns and 1ns rise time, respectively. This overshoot has to be carefully characterized and taken into account in the ESD design window or reduced by implementing efficient SCR triggering

techniques [37]. Specific characterization methods such as the transient TLP described in section 3.2 are essential to assess this overshoot.

### ***3.5 System Level ESD Protection Strategies***

With the wide dissemination of electronic products and the stringent failure requirements of Original Equipment Manufacturers (OEMs), it is important to estimate what would be the impact of an ESD stress on ICs depending on their implementation in the system. Predicting IC's ESD robustness has becoming a challenge for both IC manufacturers and OEMs. ESD requirements are even more severe on ICs with "global pins" tied to connectors and directly exposed to external aggressions of a system.

As a result, the demand for robustness against system-level, defined by IEC61000-4-2 standard (some other standards like ISO 10605 are also used for automotive applications), is increasingly shifted to the IC component itself [38] [39].

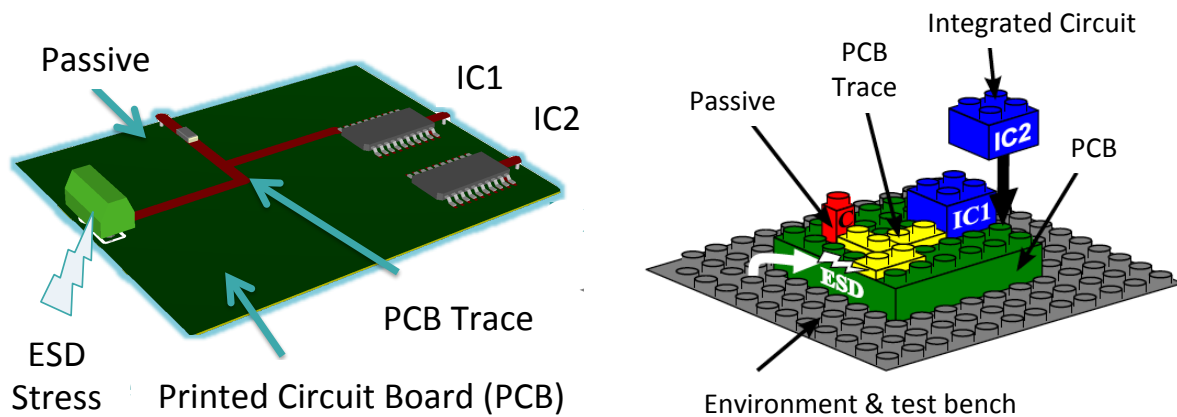
Performing ESD system level reliability prediction remains a very challenging topic. Being able to do so could bring further improvements to existing protection approaches [40], while reducing costs. The ESD stress level required during system qualification is increasing over the years. Therefore, taking into account these disturbances during the system design phase becomes mandatory to improve the system immunity, which tends to decrease with technology nodes, as observed by Camp [41].

Up to now, there is no methodology to anticipate system ESD failures, which results in redesign if the system does not fulfill the standard. To implement such predictive approach, both modeling and characterization methodologies should be developed.

To this aim, a co-design approach mixing IC design and PCB design is necessary to predict ESD current paths and failures at system level.



To ensure that chips can handle system level ESD events, OEMs face the problem of the lack of information concerning the internal ESD strategy of the ICs. The same problem arose years ago concerning signal integrity (SI) issues, and gave birth to IBIS standard [42]. IBIS file contains behavioral data of parasitic elements (of package, inputs and outputs) and description of buffers that are needed for SI simulation. Keeping the concept of IBIS description, we proposed to develop IC models to perform System Efficiency ESD Design (SEED) [43] according to the methodology presented in Figure 3.17. This methodology is intended to model a system composed of ICs, active components and external protection elements mounted on a Printed Circuit Board (PCB). The main principle consists in modeling each system part separately and assembling all parts hierarchically by following the system topology [44]. Each part of the system can be identified as an independent block as reported in Figure 3.17 (“Lego block” system approach).



**Figure 3.17: ESD system level modeling methodology: view of a printed circuit board (left) and its hierarchical representation (right).**

The main element of the system is the IC, and a dedicated attention has to be paid to be sure that the current flow through this element is correctly reproduced. Depending on the internal protections, the current can use different paths. The proposed IC model has to maintain

intellectual property rights of several manufacturers. For this reason, it is based on the existing methodology provided by IBIS model. Some of the information provided by IBIS can be kept, but to perform SEED additional information has to be added.

### *3.5.1 Advantages and Limitations of IBIS Models*

An RLC network (given by IBIS) models the package of the device. The series inductance is the only element that has the most significant impact on the waveforms. Typical values are close to a few nH [45], which is enough to induce a significant voltage spike across its terminals during transient current injection (i.e. TLP) [44].

ESD signals exhibit high  $di/dt$  and as a result, parasitic elements from IBIS are important to estimate the dynamic of the current that flows inside the chip and through the IC protections. Let us show on a simple example the importance of package parasitic elements. The typical inductance value of a surface-mount technology (SMT) package is around 3nH. For 8KV gun stress, the current rises up to 25A in less than 1ns. This means that the overshoot voltage across the inductance is instantaneously around 75V.

IBIS includes I-V data of the diodes between Input/Output and VDD (called Power clamp in IBIS), and to ground. These diodes are static ones and are only modeled from -VDD to  $2*VDD$ , which is a too small range for ESD events. Moreover, IBIS suffers from a lack of information concerning the central power clamp (PC) protection between VDD and VSS, which is crucial for the ESD strategy. An equivalent model of the commercial inverter IC used in [44], extracted from IBIS file, is reported on the schematic of Figure 3.18.

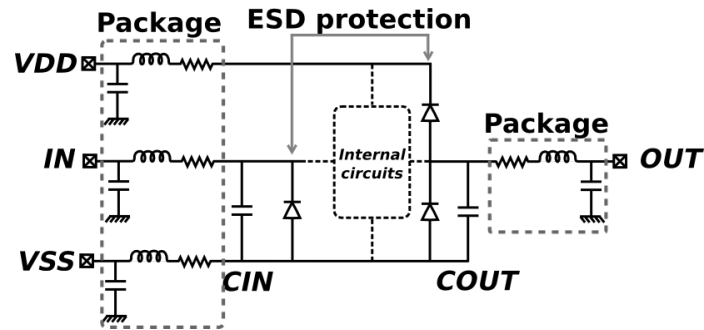


Figure 3.18: Equivalent IC model obtained from IBIS.

IBIS suffers from a lack of information concerning input and output ESD protections. The philosophy of previous work [46] was to extract a behavioral description of ESD protections between two pins from TLP measurements. The new I-V curves will replace the I-V characteristics from IBIS and protections that are not defined will be added and in particular, the Power Clamp (PC) between VDD and VSS. Then, a full behavioral description of the ESD strategy is built. To keep the IBIS concept, no prior knowledge of IC internal structures is needed, which is often the case for system designers at OEM level. Specific measurements are needed to extract information about ESD protections of the chip. Transmission Line Pulse (TLP) testing can be used to extract quasi-static and static characteristics between each pair of IC pins.

### 3.5.2 Behavioral Description of the Protections from TLP Measurement

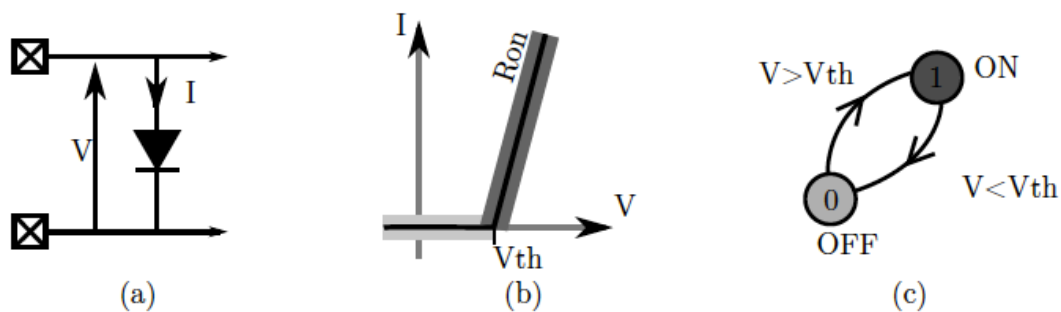
Various types of components can be extracted from TLP measurement, like simple diodes, or more complex structures with snapback, like Silicon Controlled Rectifier (SCR), or structures that clamp with dynamic conditions (triggered MOSFET - PC). Piecewise linear curves provide sufficient information whereas preserving the intellectual property of manufacturers. For example, only two I-V points could describe a simple diode. For improved accuracy and more complex devices, as many points as necessary can be added.

From all these structures, we proposed to use the simplest I-V characteristics as possible. Given the high current level of ESD stresses, small discrepancies are not important regarding the

accuracy. The parasitic elements of the PCB (line and passives) plays a much more important role than a small variation on the ESD protection on-resistance as discussed later on. Moreover, behavioral models do not reveal any proprietary knowledge on the ESD protections and are exchangeable between IC manufacturers and OEMs.

### (i) Diodes

Diodes are good examples to expose the philosophy. Only two parameters can be given like the triggering voltage,  $V_{th}$ , and the on-state resistance,  $R_{on}$ . This defines a very simple two states machine diagram (Figure 3.19). When the voltage across the diode is below  $V_{th}$ , the diode is off (State 0), no current flows into the protection. Otherwise, we are in state 1 with the equation  $V=R_{on}\cdot I$ .



**Figure 3.19: Schematic diagram of a diode (a), ideal I-V curve (b) and state diagram (c).**

### (ii) Snapback Devices

For snapback protection devices, the same philosophy is used and defines 4 states, reported on the measured I-V curves (Figure 3.20 a) and following the state diagram reported in Figure 3.20 b. Six couples of voltages and currents are defined as parameters. These  $(V_x, I_x)$  couples define the inflection points of the SCR and the equivalent equations for states 0, 1, 2 and 3. The model has been used in previous works for simulation of ESD stress injection (TLP and IEC 61000-4-2) [47]. Such model could suffer from convergence issues that are solved by adding in parallel to

the SCR, its equivalent parasitic capacitance (often given into IBIS). It prevents the internal voltage of the SCR from a strong drop.

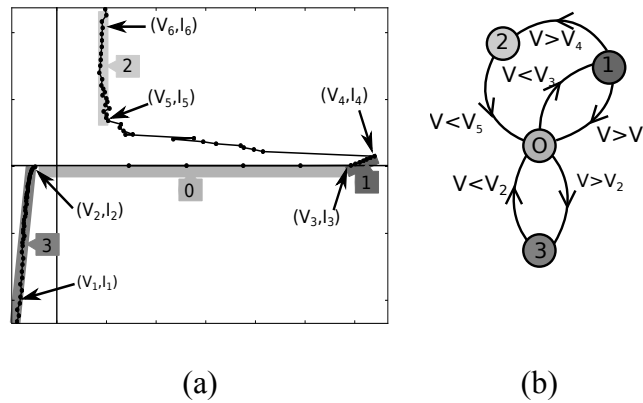


Figure 3.20: TLP measurement (a) and extracted state machine diagram (b).

### (iii) Power Clamp (PC)

PCs are based on MOS transistors with complex triggering conditions. The proposed behavioral model is a two-state machine, defined like diodes, but the triggering condition is set on a  $dV/dt$ . A similar structure has been implemented into the study of paper [46] where the susceptibility of failure is compared with measurement data into Direct Power Injection (DPI) configuration [48]. The PC drives part of the current during the stress, reducing the failure level that could be predicted using only IBIS information.

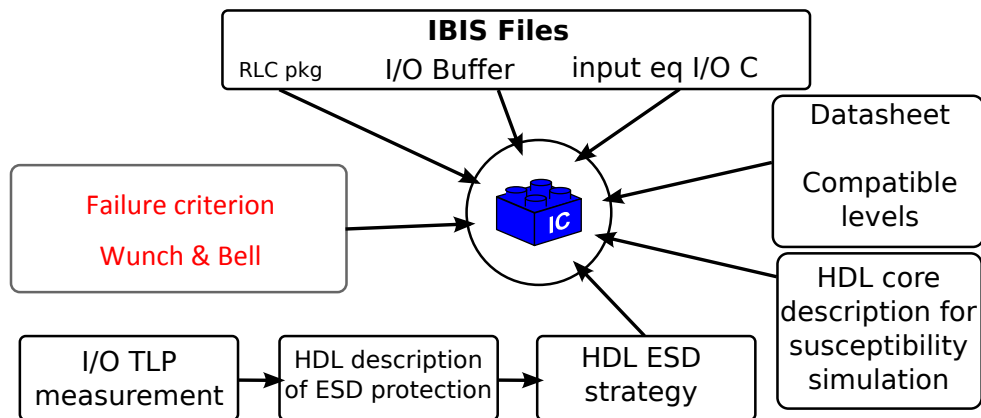


Figure 3.21: IC model elements.

### 3.5.1 Synthesis of IC Model

The combination of the different blocks forms the complete IC model introduced previously. While keeping the philosophy of IBIS files, this approach proposes improved IC model with full behavioral ESD protections description that preserves the intellectual property of semiconductor's manufacturers. Based on state-machine diagram, with a minimum set of parameters like resistances and inflection points, these models allow predicting with good accuracy the ESD current path and its impact on the IC robustness. Figure 3.21 summarizes the proposed methodology and the input needed to build up the IC model. Both system designers and IC suppliers can use such models. This work is under development at the ESDA working group WG14- "System Level ESD". This approach can be used to simulate the injection of an electrical fast transient (TLP, IEC 61000-4-2, etc.) directly on the bare die.

#### (i) Passive Elements and PCB Traces

For ESD pulses with rise-time close to the nanosecond, High-Frequency (HF) effects of passive elements are not negligible. The use of perfect models for passive components (capacitors and inductors) results in unrealistic simulations. Indeed, the impedance measurement of a 47nF decoupling capacitor versus frequency is moving from a capacitive behavior to an inductive one at 10MHz. In this case, only a HF model allows visualizing the actual transient response [49]. In the same way, for the package inductance, the high frequency inductance is non negligible for the ESD stress. Nevertheless, it is not necessary to use an HF model for every single passive element of the circuit. Only decoupling capacitors need to be modeled this way, apparently being the main passive element with a significant impact.

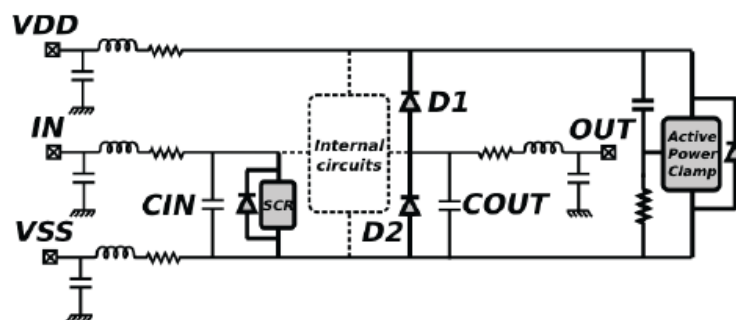
Similarly, it is really important to take into account PCB traces, even short ones (< cm), since they can introduce non-linear overvoltages when a measurement is performed. Depending on

their dimensions, PCB traces have different equivalent impedances, and their equivalent model can be complex [50]. In high current regime, using VF-TLP testing and time domain reflectometry method, we showed that PCB lines can be modeled using basic LC lumped elements, calculated using analytical formulations of [50], to take into account propagation and coupling effects.

PCB traces induce a delay proportional to their length ( $\sim 33$  ps/mm for  $110 \Omega$  PCB lines). Moreover, on the propagation path of an ESD stress, when a PCB line separates a load from a measurement point, a residual voltage peak can be generated on the measurement.

(ii) Validation on a simple circuit

This modeling methodology was applied to the commercial inverter IC whose IBIS model is given in Figure 3.18. Based on static and TLP measurement on each pair combination of pins, we were able to identify the related ESD protections. Three types were identified: diodes, an RC triggered power clamp (PC) and a silicon controlled rectifier (SCR). Each “device-type” model is assembled in a classical protection strategy as shown in Figure 3.22. The conduction of SCR and PC are modeled by a diode for their forward-biased operation.



**Figure 3.22: Full model of the commercial inverter after including into the IBIS model of Figure 3.18 the ESD protections extracted from TLP measurement.**

To validate our simulation methodology, this commercial inverter was implemented on a PCB including a  $1\Omega$  resistor between the ground plane and Vss for current measurement comparison.

Using the previously described methodology, we modeled the whole system by assembling the different blocks: parasitic elements of the package, ESD protection strategy and IC core, PCB lines, cables, measurement test bench and ESD generator [44]. With this behavioral model, we studied the impact of the value of the decoupling capacitor (50 nF, 14 nF and no capacitance) on the ESD current propagation path. Figure 3.23 presents the comparison between measurement and simulation of the resulting current in the  $1\Omega$  resistor when a 1A TLP pulse is applied between the output of the inverter and ground. We can notice the good agreement between measurement and simulation, the error being smaller than 20%. Without the external decoupling capacitance, all the current flows through the ESD protection strategy network as expected. By adding an external decoupling capacitance between VDD and ground of the IC, the current waveform strongly differs depending on the capacitance value, and on the parasitic elements of the system. When the TLP pulse ends, a continuous current is observed over twice longer time. Even if the energy is the same, the resulting thermal effect of this second current pulse could lead to the destruction of the chip since the time to failure is temperature dependent as described by Wunch & Bell [51].

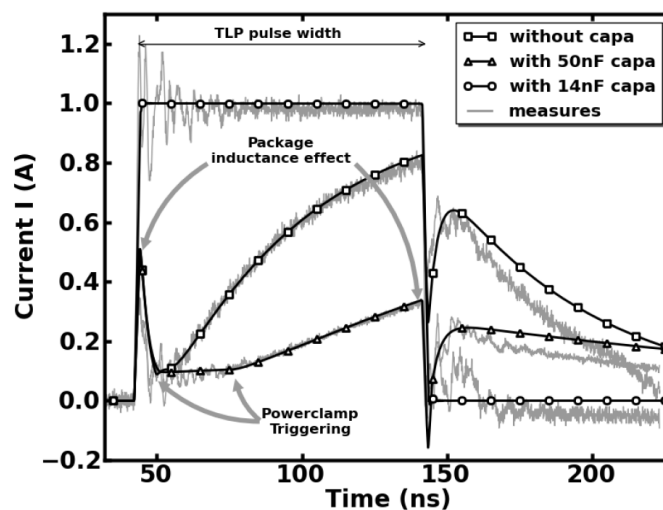


Figure 3.23: Measurement versus simulation comparison of the current in the  $1\Omega$  resistor for 1A TLP pulse injected from output to ground, with 14 nF, 50 nF and without decoupling capacitor.



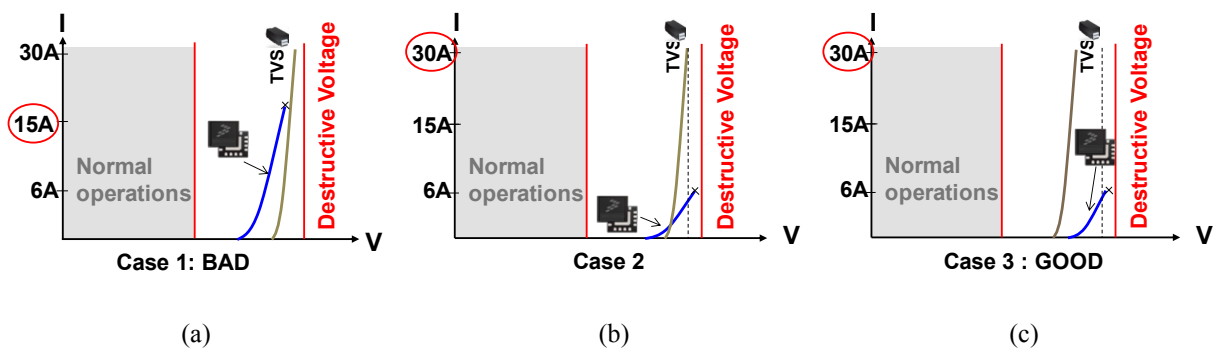
### 3.5.2 Discrete Protection: Compatibility with the Device

To cope with the high current of gun stress applied to ICs, some system engineers propose to add external discrete protections or Transient Voltage Suppressors (TVS) on the PCB. Such discrete protection is designed to clamp high ESD current. The choice of the proper discrete protection is not trivial and depends on the knowledge of the on-chip ESD protection characteristics.

System Efficient ESD Design (SEED) approach proposes the TLP information exchange of the on-chip ESD protection characteristics between system engineer and on-chip design engineer.

Regarding the optimization between discrete protection and on-chip ESD protection structure, there are three possible scenario cases that are described hereafter.

First, or bad scenario case, means that the IC ESD protection will absorb the gun stress current instead of the discrete protection (Figure 3.24 a). Low resistive voltage clamping characteristic of the IC ESD protection prevents the high voltage activation of the discrete protection. Failure will be expected at the on-chip ESD protection structure.



**Figure 3.24: Various scenarios of ESD discrete protection: Bad case (a), Mitigated case (b) and Good case (c).**

With resistive on-chip ESD protection structure characteristics as shown in Figure 3.24 (b), the discrete protection can be activated at high current. By this way, the on-chip ESD protection is only activated at low current level. Experiences from paper [52] show that this kind of protection works for the short time high current of the 150pF/330 $\Omega$  gun model and not for the long time

discharge current of the  $2\text{k}\Omega / 300\text{pF}$  gun model. It was demonstrated that the long time current discharge due to this  $2\text{k}\Omega$  resistor gun model ( $>1\mu\text{s}$ ) at low current level is applied at the on-chip ESD protection structure instead of the discrete one. As a result, the on-chip ESD protection has to absorb the energy provided by the end of this  $2\text{k}\Omega / 330\text{pF}$  gun current pulse. TLP measurement with different pulse widths from  $100\text{ns}$  up to  $1\mu\text{s}$  allows extracting the time to failure curves as mentioned by [51] and can help the system engineer check the robustness of the on-chip ESD protection over longer pulse durations.

Last scenario case (case 3, Figure 3.24 c) implies that low resistive voltage characteristics of discrete protection provide good protection of the IC protection thanks to high triggering voltage of the on-chip ESD protection structure. This case presents the drawback for the system engineer to have additional cost due to the expensive low resistive voltage clamping of discrete protection.

### ***3.6 Conclusion and Perspectives***

ESD protection strategies should be elaborated with a global approach taking into account the final application of the IC. Indeed, this would save on the one hand, silicon footprint dedicated to integrated protections since the ESD robustness of the system is not directly related to the one of the IC and on the second hand, it would avoid costly design iterations at system level. Such a global approach is already used for ElectroMagnetic Compatibility (EMC) qualification and we have shown that the same modeling approach should be implemented for ESD qualification. Regarding ESD, the main focus is on the development of protection strategies against various types of stresses. The drastic growing of embedded electronic systems in a large variety of applications requires a more global approach for their ESD qualification that is basically part of the EMC one. In the EMC field, propagation phenomena are prevailing and a large number of standards already exist whereas this is not the case for system level ESD (except IEC 61000-2-4

or ISO10605). The idea is to directly reuse the experience and methodologies developed in the EMC field to achieve the ESD system level objectives.

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