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3D ICs: An Opportunity for Fully-Integrated, Dense and Efficient Power Supplies

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Abstract— With 3D technologies, the in-package solution allows integrated, efficient and granular power supplies to be designed for multi-core processors. As the converter design obtains few benefits from the scaling, 3DIC allows the best technology to be chosen i.e. one which suits the DC-DC converter design. This paper evaluates the achievable power efficiency between on-die and in-package converters using a combination of active (28 and 65nm CMOS nodes) and passive (poly, MIM, vertical capacitor) layers. Based on the same load power consumption, on-die and in-package switched capacitor converters achieve 65% and 78% efficiency, respectively, in a 1mm² silicon area. An additional high density capacitance layer (100nF/mm²) improves efficiency by more than 20 points in 65nm for the same surface which emphasizes the need for dedicated technology for better power management integration. This paper shows that in-package power management is a key alternative for fully-integrated, dense and efficient power supplies.

Keywords—Fully-integrated power supply, switched capacitor converter, multi-core, on-chip voltage regulator, 3D power management.

I. INTRODUCTION

Fully-integrated dc-dc converters seem to be a power-efficient solution to supply a heterogeneous System on Chip (SoC) on the same package such as multi-core processors (Fig. 1). The advantage is to provide clean, fine, high speed and individual power supply modulation for the various blocks in the SoC without bulky off-chip passive components or numerous power pins [1].

Nonetheless, the recently published on-die power converters integrated in the same process as the digital core, i.e. the most advanced technology, still achieves performance far from the industrial targets in terms of power density, voltage regulation, efficiency versus conversion ratio or direct battery connection compatibility [2], [3], [4].

Due to the difficulty in integrating on-die dense passive components [5] and high voltage-rating transistors in recent CMOS technology, 3D integration is a key opportunity to propose an alternative and efficient way between off- and on-die converters by using a less recent and more compatible technology to integrate active and/or passive components in DC-DC converters [4], [5], [7].

This paper aims to compare the 2D and 3D approaches using one or multiple active and passive layers to improve the achievable efficiency of the integrated power supplies of a multi-core processor. The 65nm bulk (mature, high yield), 28nm FDSOI (dense integration, large DVFS capability [8]) process and a potential TSC technology in a passive layer (high capacitance density [9]) are studied in this paper. This comparison leads to the key question: how much area is needed to integrate power supplies from this combination of three technologies to reach targeted power efficiency?

To answer this key question, the power partitioning, converter structure, main design trade-off and different technology combinations are first introduced. Then, the converter efficiencies are compared using a combination of 28, 65nm and TSC technologies. The analysis leads to a discussion

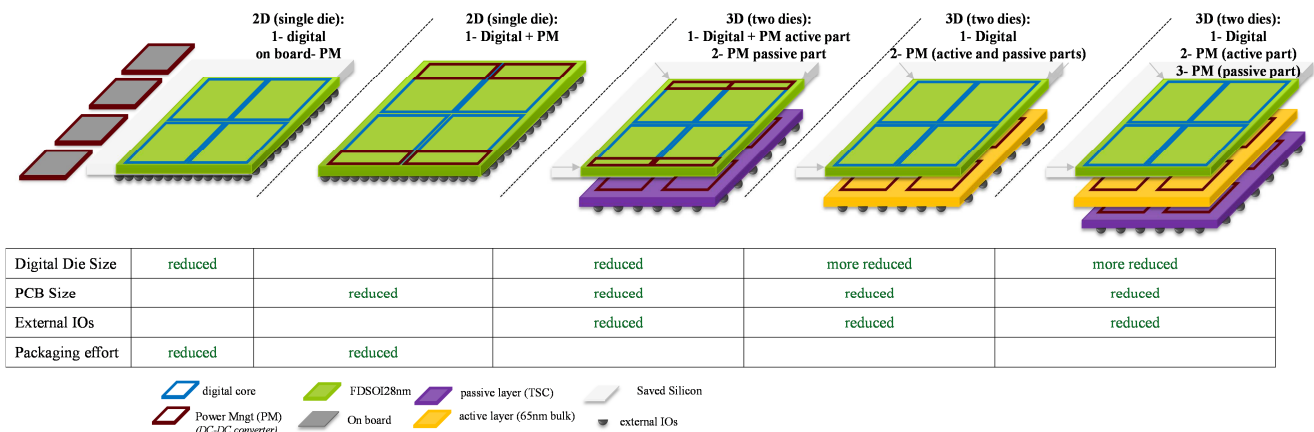


Fig. 1. Possible integration of quad-core processor and its dedicated granular power supplies.

of the opportunities of using 3D technology and the possible trends for more efficient on-chip power management in a single-chip multi-core system.

II. POWER MANAGEMENT DESCRIPTION

A. Power Tree Partitioning

A typical power tree consists of two or three cascaded DC-DC conversion stages as shown in Fig. 2. The first step-down converter provides an intermediate power rail V_{dd} from the primary supply bus V_{in} e.g. from a chemical battery. An inductive-based switching converter is often used mainly to keep high efficiency over a large conversion ratio and at high current. Designing by power electronics community, the first stage is traditionally off-chip converter chosen in currently available buck type regulator. The V_{dd} value is chosen to provide a compatible input voltage rating for the on-chip second stage, typically 1.8V where the greater this power rail value, the less current there is, thus requiring fewer power pins for the packaging.

In the latest N-core processor generation [1], the second stage provides individual DVFS technique for N cores to dramatically reduce the processor consumption. It includes N converters as close as possible to the N cores to provide fast and clean power supplies. These converters could be off-chip, in-package or on-die. Off-chip i.e. an on-board solution (Fig. 1, left scheme) fails to meet the fast power demand of the different supply domains in the multi-core system mainly due to the trace impedance [9]. Moreover, the N off-chip converters around the N-core processor occupy a large area on the PCB and need numerous power pins. Only in-package and on-die seem to be relevant solutions for granular power management (Fig. 1, other schemes). With the prospect of integration, the design of the second stage is mostly handled by the VLSI community.

A third stage could be added to protect against severe transient signals and so reduce the fluctuation of the power supply even if each step includes bypass capacitors and fast-transient feedback to smooth the power rails. For example, the current profile varies with tens of A per ns in real processors [1]. Typically, N small-area linear regulators are implemented on-die i.e. closest to the N cores. As the conversion ratio is close to one, their efficiency can be more than 90% [10].

B. Converter Topology in the Second Stage

Linear voltage regulators are widely used in the second stage thanks to their dense integration [10]. Unfortunately, they suffer from low efficiency when the output voltage is not close to the input voltage. In the second stage, the input voltage is

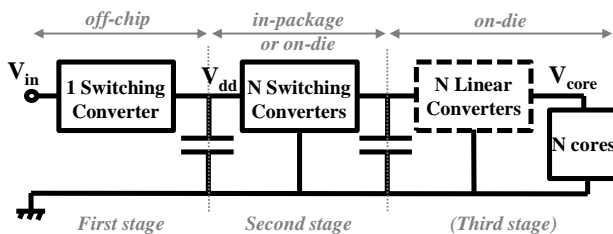


Fig. 2. Third-stage power partitioning

1.8V and the output varies from 0.5 to 1V leading to less than 50% efficiency for a linear regulator. Some published work suggests replacing the linear regulator by the switched converter for power efficiency improvement ([3], [4]). However, the inductive-based switching converter suffers from low on-chip integration as the magnetic-core inductor is not compatible with CMOS process [5]. Therefore, with this topology, it is difficult to compare on-die and in-package solutions. Switched capacitor converters (SCCs) have been well studied to alleviate this problem. This approach offers easier on-chip integration thanks to the high capacitance density in recent CMOS technologies [2], [11]. However, SCCs also have different drawbacks such as efficiency dependence on conversion ratio and large input current pulse i.e. a potential EMC issue.

A non-external SCC component needs silicon area to integrate the capacitor which could be costly if they are integrated on the same die as the digital functions in most recent technology. However, 3D technology stacking of the N converters or their passive components just below the N cores is an alternative. It potentially reduces the overall cost of the chip saving costly silicon die by replacing the last digital technology by thicker or fewer-step processes. The active layer can also integrate other functional blocks such as non-volatile memory or intra-core communication which slightly gain performance from the CMOS scaling.

The 2:1 SCC topology is studied here because of its excellent integration capacity proved in the standard CMOS process [2]. Under ideal conditions, the converter reduces the 1.8V voltage rail generated by the first stage to 0.9V. If other voltages are needed, N:M conversion ratios and voltage regulation of SCC are possible [3].

The SCC mainly consists of a flying capacitor C_{fly} charged and discharged in two phases by four switches as shown in Fig. 3.a. In the first phase, ϕ_1 , T_1 and T_4 are in on-state and the capacitor is charged from the input voltage through the output load. In the second phase, ϕ_2 , the flying capacitor is discharged into the load through T_2 and T_3 . Between the two phases, a dead time is introduced to avoid cross-conduction between the output, input voltage and ground (Fig. 3.b). The T_4 transistor is an N-type to improve its driving capability when the output voltage is lower than $V_{dd}/2$.

In steady-state and under ideal conditions (infinite capacitor and switching frequency values, ideal switches), the output

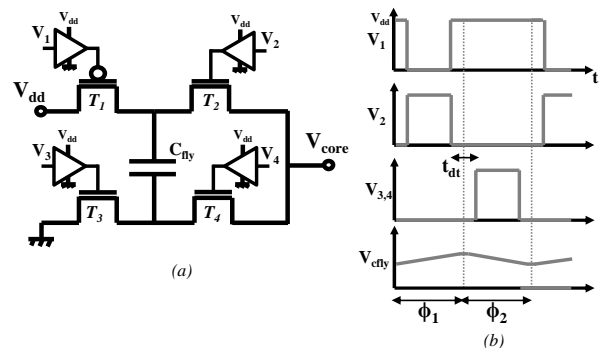


Fig. 3. 2:1 SCC topology

voltage V_{core} is equal to $V_{dd}/2$ and the converter efficiency reaches 100%. In practical conditions, the switches introduce conduction and switching losses. Moreover, the capacitance value is limited by the finite silicon area which induces a charge/discharge loss and output voltage ripple. To predict the efficiency and gain physical insight, small signal models of this structure are given in the literature [2],[12] as shown in Fig. 4.a. The resistances R_c and R_p represent the conduction and switching loss, respectively. In following the switching loss means the loss due to the charge and discharge of the gate capacitance, not the loss induced by the nonzero $V_{ds} \times I_{ds}$ product during the switching. The overall loss can be summarized by the following equation from [16] in SSL or FSL regions [2]:

$$P_{loss} = \underbrace{\lambda_c f_{sw} V_{dd}^2 \sum W_i}_{\text{MOSFET input capacitance}} + \underbrace{\frac{1}{2} I_{core}^2 \lambda_r \sum \frac{1}{W_i}}_{R_{ds(on)}} + \underbrace{\frac{I_{core}^2 R_s}{\text{Flying capacitor ESR}}}_{\text{Flying capacitor ESR}} + \underbrace{\frac{V_{core}^2 k_{bot} C_{fly} F_{sw}}{\text{Bottom plate}}}_{\text{Bottom plate}} + \underbrace{\frac{I_{core}^2}{4 C_{fly} f_{sw}}}_{\text{Switched Capacitor impedance}} \quad (1)$$

where, W_i is the width of each transistor, F_{sw} the switching frequency, λ_c the gate capacitance density (expressed in F/m), λ_r the on-state resistance density ($\Omega \times m$ metric) and k_{bot} the parasitic to flying capacitance ratio.

Assuming the area of the switches is negligible, the flying capacitor is set by the desired surface of the SCC and capacitance density (F/m²) offered by the targeted technology i.e. an area constraint optimization. The variables $\{F_{sw}, W_i\}$ are the only design freedom parameters to maximize the power efficiency under a load profile $\{V_{core}, I_{core}\}$ defined by the digital core. As shown in Fig. 4.b, the maximal efficiency is obtained at an optimal value $\{F_{opt}, W_{opt}\}$ where W_{opt} represents the total width of the switches. The optimal output voltage V_{opt} is below a 2:1 voltage gain due to the finite equivalent output resistor R_c (Fig. 4.a). It is important to notice our optimization maximizes the power efficiency without guarantee on the output voltage.

The SCC provides a sufficiently fast transient response to meet the load transient requirement as proven in [6], [13]. If a small voltage regulation range is required, the switching frequency could be slightly modulated. However, the efficiency is reduced as the SCC acts as a linear regulator outside its optimal 2:1 ratio (Fig. 4.b). As previously mentioned, this is one of the limitations of switched capacitor topology. For large output voltage regulation, reconfigurable SCC [3] or MISO [17] topologies can be used to maintain

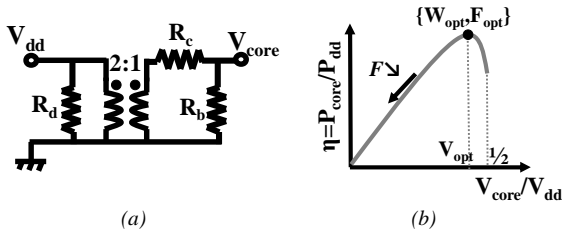


Fig. 4. Small signal model and power efficiency v. voltage gain

higher efficiency.

C. Area constraint of the on-die and in-package converters

The on-die solution requires the area of the core die to be increased as shown in Fig. 5. An additional area of 10% seems to be an acceptable solution for industry. On the other hand, a 3D solution could offer more flexibility in terms of area constraint. For instance, to keep the same chip surface, the surface of the stacked converter could be equal to the size of the digital core. However, the final choice is made according to the cost of the overall chip including the silicon die, 3D assembly and packaging. Unfortunately, the authors have insufficient data to provide a relevant cost analysis. Here, the 65nm and TSC process are expected to be far cheaper than the 28nm allowing more space allocation for an in-package SCC for the same price.

D. Load Profile

The power consumption of an MIPS32 core within the TSAR architecture [14] in FDSOI is used to define the converter's consumption profile $\{V_{core}, I_{core}\}$. The one digital core is modelled by a current source controlled by a voltage source defined as:

$$I_{core} = V_{core}^2 + 0.2V_{core} - 0.1 \quad (2)$$

For example, the power consumption is about 0.9W for a 0.9V core voltage. The die area of one core is approximately 21mm². (This value is the S_{core} in Fig.5 and will be kept in the following analysis.) The power density is then 43mW/mm², which is relatively low compared to current digital dies (about 1W/mm²).

III. COMPARISON OF CONVERTER EFFICIENCY

A. Key Parameters for an Efficient Converter

Equation (1) predicts the SCC efficiency using three technology parameters: λ_r , λ_c and k_{bot} . For example, λ_r and λ_c illustrate the switch capacity to reduce the conduction and switching losses, respectively, i.e. the 2nd and 1st terms in this equation. In this paper, thick oxide 150nm- and 280nm-long channel transistor L_{sw} in 65 and 28nm technologies, respectively, are chosen to allow 1.8V input operation. The figure of merit (FoM) for the switch, well used in the power community, results from the trade-off between conduction and switching capacity and is given by:

$$FoM_s = R_{on} \times Q_g = \lambda_r \times \lambda_c \times V_{drive} \quad (3)$$

where, R_{on} is the on-state resistance, Q_g the total charge

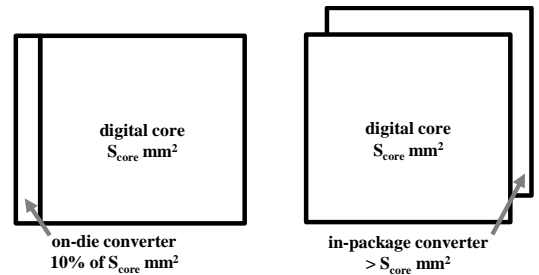


Fig. 5. Small signal model and power efficiency v. voltage gain

needed to switch from OFF to ON states, and V_{drive} the gate voltage swing (here 1.8V).

The capacitance density σ_c is also a key parameter as the flying capacitor value is strongly linked to the achievable efficiency as shown by the 5th term in (1). The two technologies offer poly/nwell and MIM capacitances. The high density poly-type capacitance i.e. thin oxide, is not permitted in the SCC design as the maximal voltage value across the flying capacitor (1.2V max in steady-state, 1.4V in transient) is higher than its maximal voltage rating (1V in 28nm and 1.2V in 65nm). The thick oxide poly-type capacitance was chosen as it offers a higher voltage rating but lower density. It also suffers from a non-negligible bottom plate capacitance which influences the efficiency as shown by the 4th term of equation (1). The k_{bot} parameter is expressed as:

$$k_{bot} = \frac{C_{bot}}{C_{fly}} \quad (4)$$

Moreover, the poly capacitance area cannot be reused to stack the transistors of the digital core as it already uses the polysilicon layer. The MIM-type could be stacked on the poly-type capacitor to gain density but the MIM option adds a slight cost (a few % more). Here, the k_{bot} coefficient for MIM is assumed to be zero as the metal layers for the plates are far from the bulk i.e. typically on the 5th and 6th layers. For all capacitor types, the equivalent series resistor (ESR) is assumed to be negligible (though non-negligible in practice). This paper studies an ideal case which involves a lower SCC efficiency in reality.

B. Technology Capability

To highlight each technology capability, Table 1 gives the most critical parameters which influence the SCC efficiency. The best parameters are highlighted in bold. Concerning the switching capability, the two technologies offer a similar FoM_s . The total stacked capacitance in the same surface is about 50% higher for the 28nm node which potentially allows

TABLE I
PROCESS PARAMETERS INFLUENCING CONVERTER PERFORMANCE

Parameter	65nm bulk	28nm FDSOI	Unit
N-MOSFET channel resistivity λ_c (1)	0.7	0.5	$k\Omega \times \mu m$
Gate capacitance per transistor unit length λ_c (1)	1.6	1.8	fF/ μm
Figure of Merit of the switch FoM_s	1.9	1.8	$k\Omega \times fC$
Integrated poly capacitance density $\sigma_{c,poly}$ (2)	9.6	6.6	fF/ μm^2
Integrated MIM capacitance density $\sigma_{c,mim}$ (3)	5.0	15.9	fF/ μm^2
Total stacked capacitance $\sigma_{c,poly} + \sigma_{c,mim}$	14.6	22.5	fF/ μm^2
Bottom plate poly cap. Coefficient k_{bot} (4)	1.2	8.6	%

Note: in bold, the best benefit value in terms of converter design (1) Thick oxide 150nm- and 200nm-long channel transistors in 28 and 65nm technology, respectively; driving voltage 1.8V; (2) Thick oxide polysilicon capacitors at 1.0V bias with 1.8V maximal voltage rating; (3) additional layers needed for Metal Insulator Metal capacitor option, the bottom plate of the MIM is negligible. In 28nm, the MIM voltage rating is 1.1V (4) included in the DKit model (not post-layout extracted).

the best power density for the SCC i.e. reducing the 5th term in (1). In practice, the capacitance density is less than the given value for both technologies (see Table 1) as some partitioning is needed to reduce the effective ESR. The FDSOI process suffers from a higher bottom plate coefficient k_{bot} thus increasing the 4th term in (1).

Table 1 gives an overview of the main advantages and disadvantages of these technologies but it fails to give an exact figure for the achievable efficiency of an SCC for a given surface. However, section III.D will discuss this.

C. Vertical Capacitor Integration: a Relevant Option

The previously mentioned capacitors (poly and MIM) have planar plates. The surface density σ_c (F/m²) is mainly limited by the thickness of the dielectric e (about 1nm) and is expressed as:

$$\sigma_c = \frac{C}{S} = \epsilon \frac{S}{e} \times \frac{1}{S} = \frac{\epsilon}{e} \quad (5)$$

Where, S is the surface required for the capacitor, and ϵ is the permittivity.

The vertical capacitor is an alternative solution to alleviate this problem. For example, deep-trench capacitance has proven its ability to reach a high density value and efficient SCC on a smaller area [15], [6].

In recent literature from the 3DIC community, the through silicon capacitor (TSC) is introduced [9]. The main advantage is its higher capacitance density compared to planar CMOS capacitance e.g. poly or MIM. As the SCC efficiency strongly depends on the capacitor value, this paper will also explore the TSC option as well as the planar capacitance.

Fig. 6 shows the three possible stacking arrangements in the context of this paper. The first solution consists in integrating the TSC in the 65nm die where through silicon via (TSV) does not take up the total die area). The TSV is not shown in Fig. 6. The second solution is to have an additional layer with specific technology which integrates the passive components i.e. TSC capacitors. The third solution is to integrate the active part of the converter in a 28nm die i.e. the switches and control, and to use a passive layer for TSC capacitance. In all cases, the available on-die capacitor (poly and MIM) could also be used to improve the overall capacitance density.

Based on the literature and the expected evolution of this promising technology, a 100fF/ μm^2 capacitance density with no bottom plate ($k_{bot} = 0$) and no ESR are assumed in the following sections.

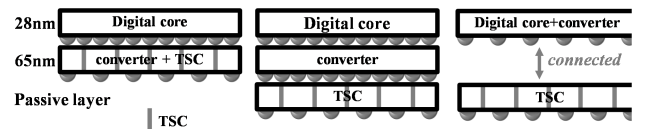


Fig. 6. Stacking configuration to integrate TSC in the power distribution.

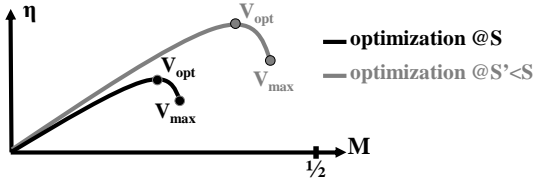


Fig. 7. Maximal efficiency versus maximal output voltage

D. Simulation-based Optimisation and Comparison

The same 2:1 SCC topology (Fig. 3) in both technologies is optimized to reach maximal power efficiency. The conditions are to supply the MIPS32 core defined in II.C with 1.8V input voltage for a given die area. The dead time is set to 500ps and the driver loss is taken into account. Figure 8 shows the achievable power efficiency versus die area of the SCC topology using 28 and 65nm nodes with planar (poly and MIM combination) and vertical (TSC) capacitances. These results come from transistor-level simulations.

Fig. 8 shows the maximal efficiency achievable by SCC occupied a silicon surface from 0.1 to 50mm² for different capacitance options: poly only, poly and MIM stack, and TSC only. As our optimization does not guarantee any output voltage, the two gray lines illustrate the achievable output voltage value. For example, 0.8V and higher output voltage is reached at maximal efficiency in few cases: only surface higher than 10mm² for TSC option and than 25mm² in 28nm with MIM. To clarify the difference between the maximal efficiency at the optimal output voltage (V_{opt}) and the achievable output voltage at a lower efficiency (V_{max}), two optimization cases are traced in Fig. 7 where η is the efficiency and M is the conversion ratio (V_{core}/V_{dd}).

In a poly configuration, the 28nm node is less efficient than 65nm. For example, the power efficiency in 28nm is decreased by 8 points for the same 1mm² surface or the area is multiplied by 6 to keep 73% efficiency compared to 65nm. This is mainly

TABLE II
EFFICIENCY IN 2 AND 3D SOLUTION COMPARISON WITH CAPACITANCE OPTIONS FOR THE PROCESSOR UNDER TEST

Capacitance option available	2D	3D
only poly	65	78
MIM, no TSC	92	87
MIM and TSC	92	96

due to the high parasitic capacitance i.e. the 4th term is predominant.

In the poly and MIM stack configurations, the 28nm process offers the best efficiency over the whole die area range. This is mainly due to better capacitance density as already shown in Table 1. The poly-type capacitance is removed from the stack in 28nm due to a high k_{bot} parameter. The capacitance density $\sigma_{C,MIM}$ is lower but the overall efficiency is better allowing higher switching frequency. Now, 28nm has four points of efficiency more than 65nm at 1mm². To keep the same efficiency, the converter needs to be 50% larger in 65nm than in 28nm. Thus, the surface area saved in the expensive 28nm die could cover the additional cost of a larger 65nm die.

The vertical capacitance improves power efficiency in both technologies. For 1mm² converter area, the efficiency is improved by 23 points in 28nm. The gap between 28nm and 65nm is negligible as the switch characteristics are equivalent (see Table 1). This option confirms the major role of the dense passive layer to propose efficient and dense integrated DC-DC converters. A decrease in surface highlights the benefit of using TSC.

For the processor being studied here, 10% additional area is allocated for its on-die power supply (see section II.C), meaning 2.1mm² of 28nm using poly-type capacitance. From Fig. 8, the power efficiency is equal to 65%. For in-package solution, the 65nm area could be up to 21mm² implying 87% power efficiency. If the MIM could be integrated on the top of the digital core, the surface dedicated to the SCC is S_{core} . In this

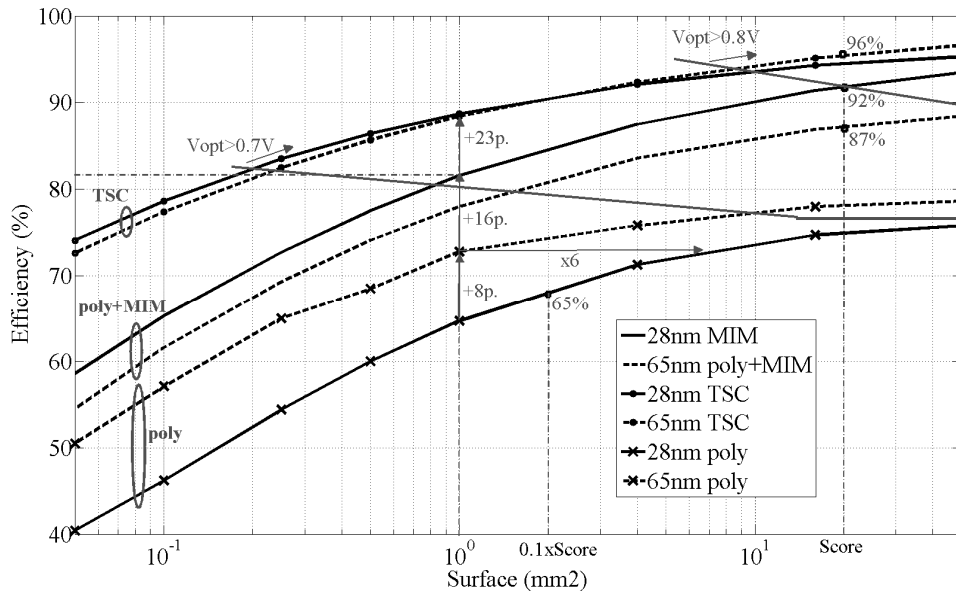


Fig. 8. Power efficiency v. die area in 28 and 65nm nodes from transistor-level simulations.

case, 92% efficiency is possible in 28nm, better than the in-package solution. The TSC option improves the efficiency to 96% in both technologies as S_{core} is used to integrate TSC capacitors (Fig. 6). Table 2 resumes the different options in 2D and 3D contexts.

If the power density of the load increases e.g. 1mm^2 instead of 21mm^2 , the dedicated area in 28nm-poly case is reduced to 0.1mm^2 leading to less than 50% efficiency i.e. lower than a linear regulator. Therefore, we can say that the introduction of TSC increases the efficiency to 90% as the flying capacitor covers the same area than the digital load i.e. 1mm^2 . To conclude, high power density digital load needs special layer such as TSC to reach acceptable efficiency and output voltage.

E. Optimal Switch Width and Switching Frequency

The optimal $\{F_{opt}, W_3\}$ parameters of the four SCCs are given in Fig. 9. The total switch width is given by:

$$W_{opt} = \sum_{i=1}^4 W_i = 3 \times W_3 + 2 \times W_3 + W_3 + 2 \times W_3 \quad (6)$$

A decrease in surface area, increases the switching frequency to compensate the 5th term in (1), but also decreases the total switch width to limit the 1st term in (1). For 1mm^2 , the on-die converter operates at a 100MHz switching frequency with a total transistor width of 10mm for both technologies. These similar results can be explained as the result of a global optimization of all terms in (1).

The TSC option reduces the optimal switching frequency from 100 to 20MHz for 1mm^2 . This lower frequency leaves room to increase the total switch width as all terms in (1) are optimized at the same time. However, it is important to point out that the surface of the switches is far lower than the SCC area confirming the negligible surface of the switches, as:

$$S_{sw} = W_{opt} \times L_{sw} \ll S_{core} \quad (7)$$

F. Losses distribution

Figures 10 and 11 show the loss distribution in 65nm node

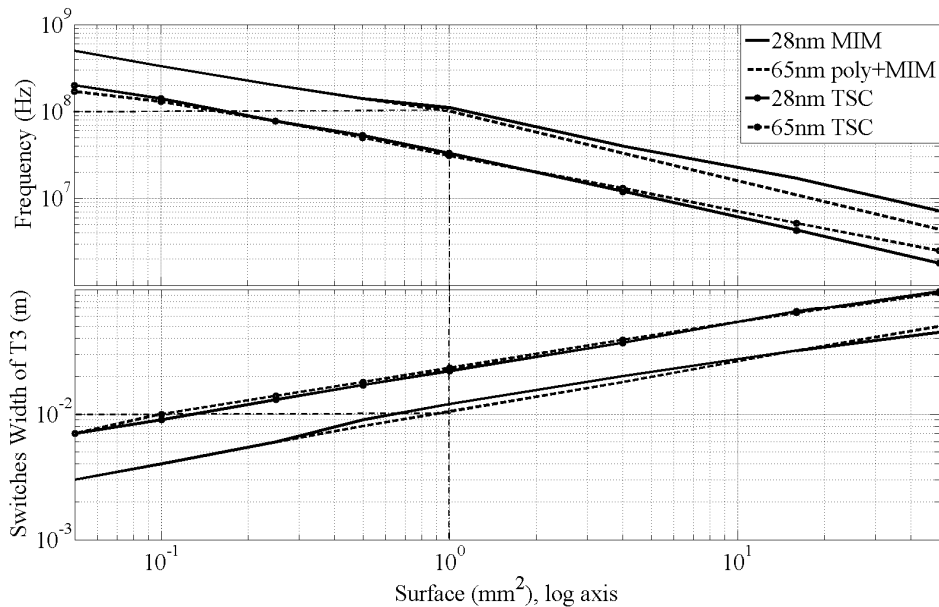


Fig. 9. Power efficiency v. die area in 28 and 65nm nodes from transistor-level simulations.

with poly and MIM stack configuration at 27mm^2 silicon surface (S_{core}) when the frequency or transistor widths vary. The losses are distributed between DC and AC conductions, bottom plate and driver which correspond to 2nd, 4th, 3th and 1st terms in equation (1) respectively. The $\coth(\frac{\beta}{2})$ coefficient places the SCC behavior in the SSL or FSL regions [12]. In Fig. 10 and 11, the optimal point to reach the maximal efficiency is $\{F_{opt}, W_3\} = \{9\text{MHz}, 34\text{mm}\}$ (see Fig. 9). For example, if the switching frequency decreases, the efficiency is reduced due to the AC conduction loss (Fig. 10). In this case, the SCC is in SSL region. In opposite, if the switching frequency increases (FSL region), the power feeds by the gate drivers and the bottom plate charge/discharge phenomena are increased then reducing the SCC efficiency. To conclude, these Figures clearly show the optimal point and losses distribution when the $\{F_{opt}, W_3\}$ couple varies.

Fig. 12 shows the loss distribution at the maximal efficiency when the SCC surface varies from 0.05mm^2 to 50mm^2 . At higher surface i.e. higher flying capacitance value, the bottom plate loss contribution increases. The optimal SCC region is between SSL and FSL as $\coth(\frac{\beta}{2})$ is close to the unity.

G. Towards Reducing the Pin Number

By using higher voltage-rating components, the input voltage can be increased which then reduces the current through the power pins. Therefore, the number of pins is reduced in the final packaging. In the context of this paper, the 65nm process offers a 2.5V voltage rating transistor and 1.8V capacitor and so the 2.5V input voltage rail can divide the current by 0.7 compared to 1.8V case. The IO pins can be reduced by 50% to keep the current constraint. This scaling is more difficult in 28nm as the maximal voltage of the MIM capacitor is limited to 1.4V. Moreover, the switches have to be cascaded reducing the FoM_s defined in (2).

H. Limitations and strengths of this analysis

A comparison has been made using assumptions justified in the previous sections: i) maximal capacitance density, ii) no capacitance ESR, iii) no effect of the interconnection (layer to layer), iv) no power consumption from the feedback, v) only 2:1 ratio analysis, vi) negligible effect of the layout especially on k_{bot} , vii) low density digital core, viii) no static or dynamic FDSOI back biasing, ix) only results from transistor-level simulations, x) no driving swing optimization, xi) no interleave scheme, xii) no thermal analysis, xiii) no output voltage guaranteed in the optimization procedure. However, in practice, the power efficiency will be lower. The inductive-based converter is also not studied even if published work [1] has proven their capacity for a dense and efficient converter with a passive layer.

The above assumptions are chosen to analyze the maximal efficiency achievable by the two technologies under the same constraints. Our aim is to avoid a table comparing previous published work using heterogeneous technologies (MIM, deep trench, SOI) under different constraints (load current profile, input voltage, die area) [11], [1]. On the one hand, the key advantage of these tables is to access the achievable efficiency in practice. On the other hand, the comparison range may be too large to clearly underline the effects of the process and design choices.

IV. DISCUSSION AND TRENDS

This study confirms that 3D technology is a relevant candidate to provide an efficient integrated power supply in a multi-core processor context. As DC-DC converters do not directly benefit from scaling technology, the additional active or passive layers in a 3D context allow a higher voltage rating transistor or higher capacitance density which better suits the converter requirements. This solution saves the expensive die-area of digital cores, improves the silicon yield, increases the acceptable input power supply and therefore reduces the pin number for the external package. The recent improvement for high capacitor and inductor value integration in a process including a small number of steps argues in favor of this.

The authors believe that the future of granular power management is 3D with dedicated layers for power as shown in Intel's choice [1] rather than on-die converters. 3D design also allows multiple layers to integrate N converters in parallel to again improve the power density. However, the best topology between inductive-, capacitive- or resonant-based converters is not clear cut as it strongly depends on the passive performance offered by the emerging 3D technologies.

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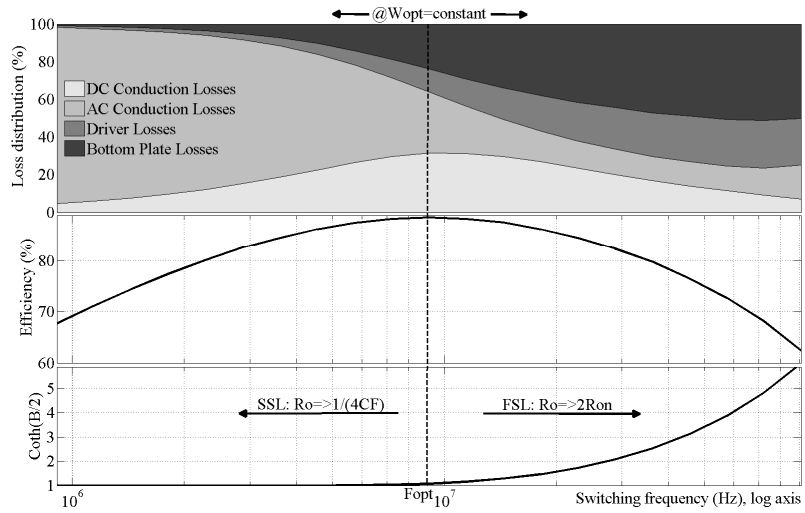


Fig. 10. Loss distribution v. switching frequency at the optimal width for 65nm in poly and MIM stack configuration ($S=27\text{mm}^2$)

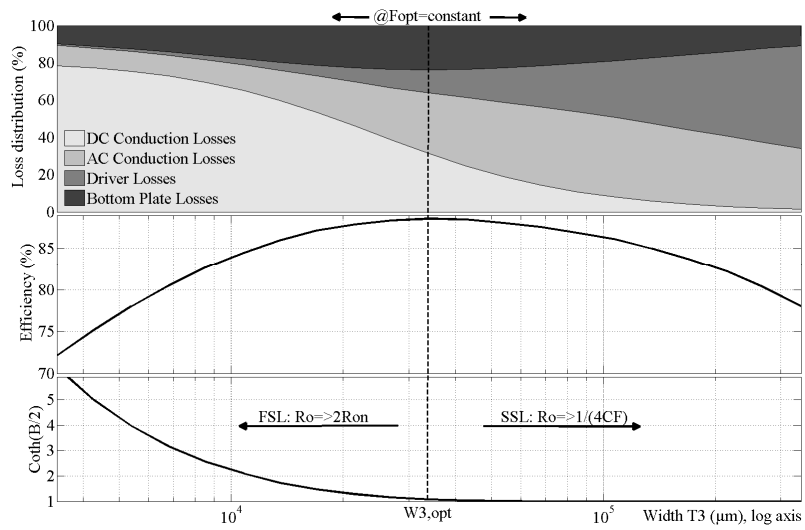


Fig. 11. Loss distribution v. transistor T3 width at the optimal frequency for 65nm in poly and MIM stack configuration ($S=27\text{mm}^2$)

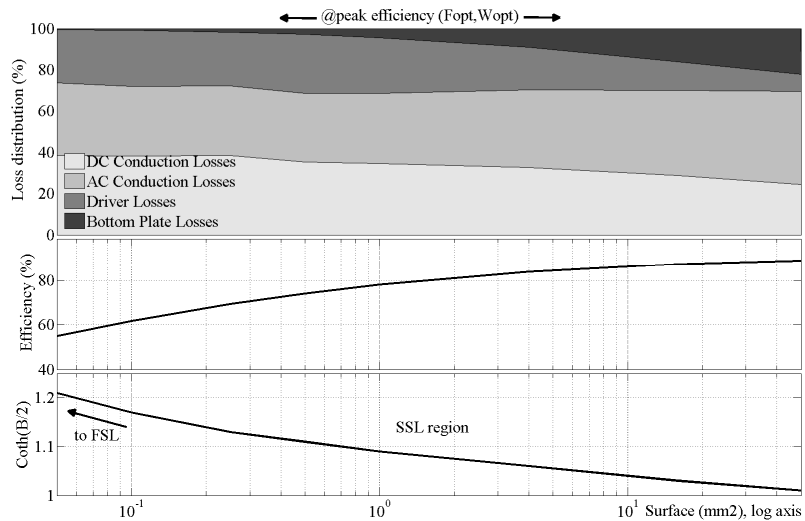


Fig. 12. Loss distribution at optimal switching frequency and transistor width v. CSC surface for 65nm in poly and MIM stack configuration