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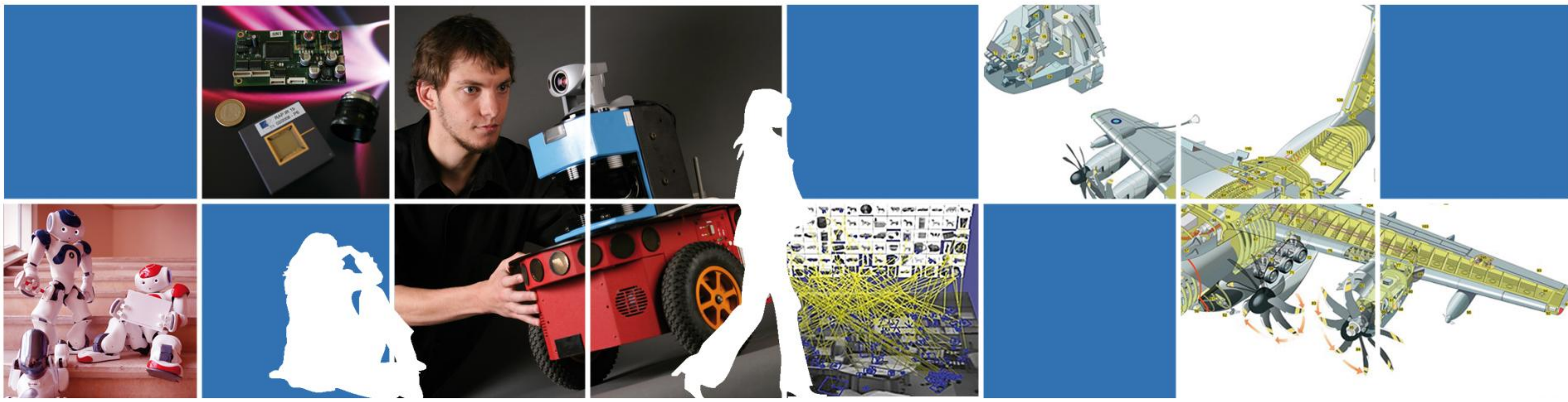
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A WCET estimation workflow based on TWSA model of SystemC designs

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Objectives

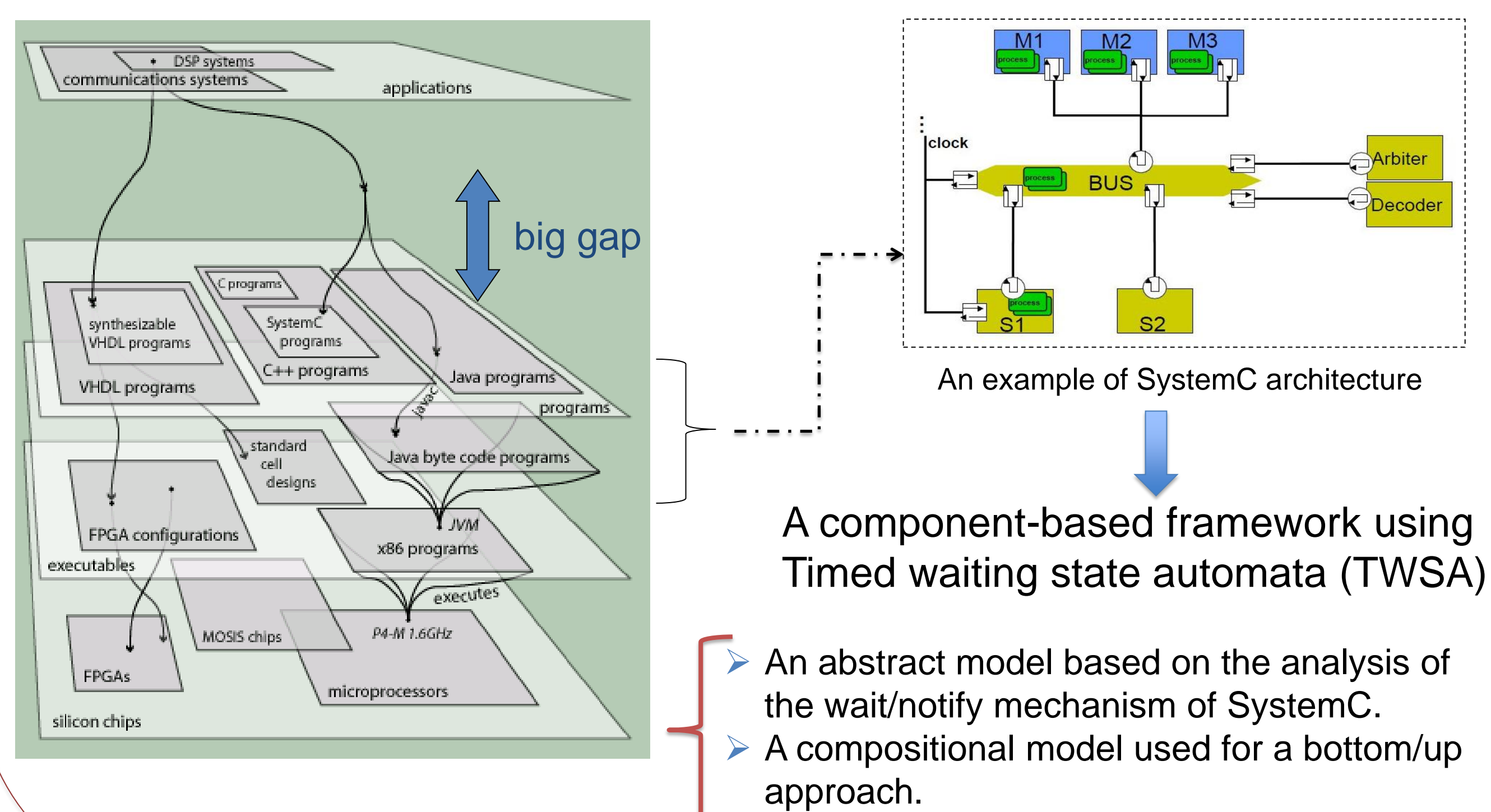
- Validating functional (correctness of system behavior) or non-functional properties (time constraints) of hard real time systems. Using the timed SystemC waiting state automata (TWSA) to model the hardware.
- Timing properties need to be carefully addressed as they are important in performance and safety verification of real time embedded systems.
- Giving an upper bound estimation of the worst case execution time of the code running on the modeled system.

Issues

- Scientific challenges:** verify and validate embedded software
- Industrial challenges:** verify both functional and non-functional properties of a hard real time systems.

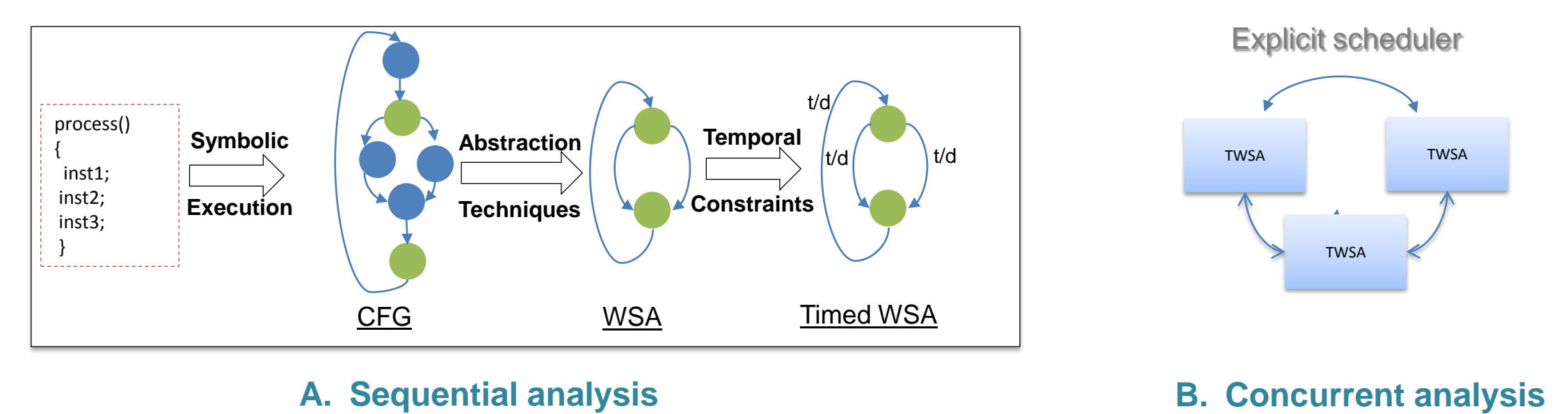
Programming language: SystemC

SystemC is a system level design language for hardware/software modelling, it extends C++ by concurrency, time, hardware data types, reactivity... It has a simulation kernel that executes designs in a discrete-event simulation

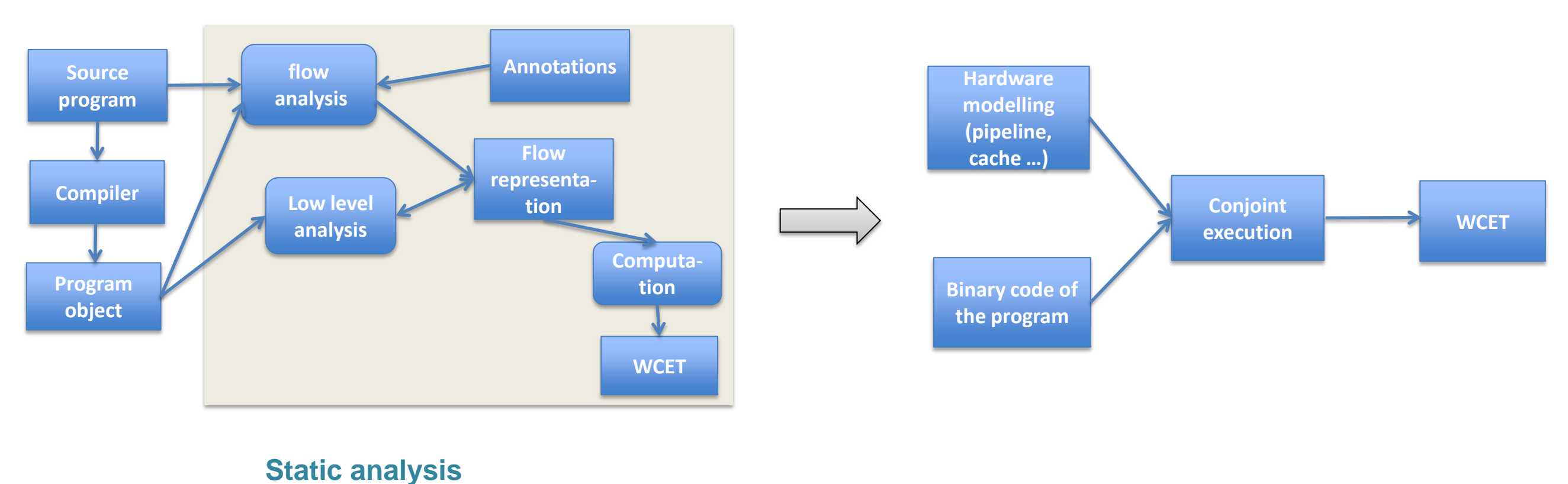


Problem: Building TWSA & WCET estimation

1. Building the abstract model

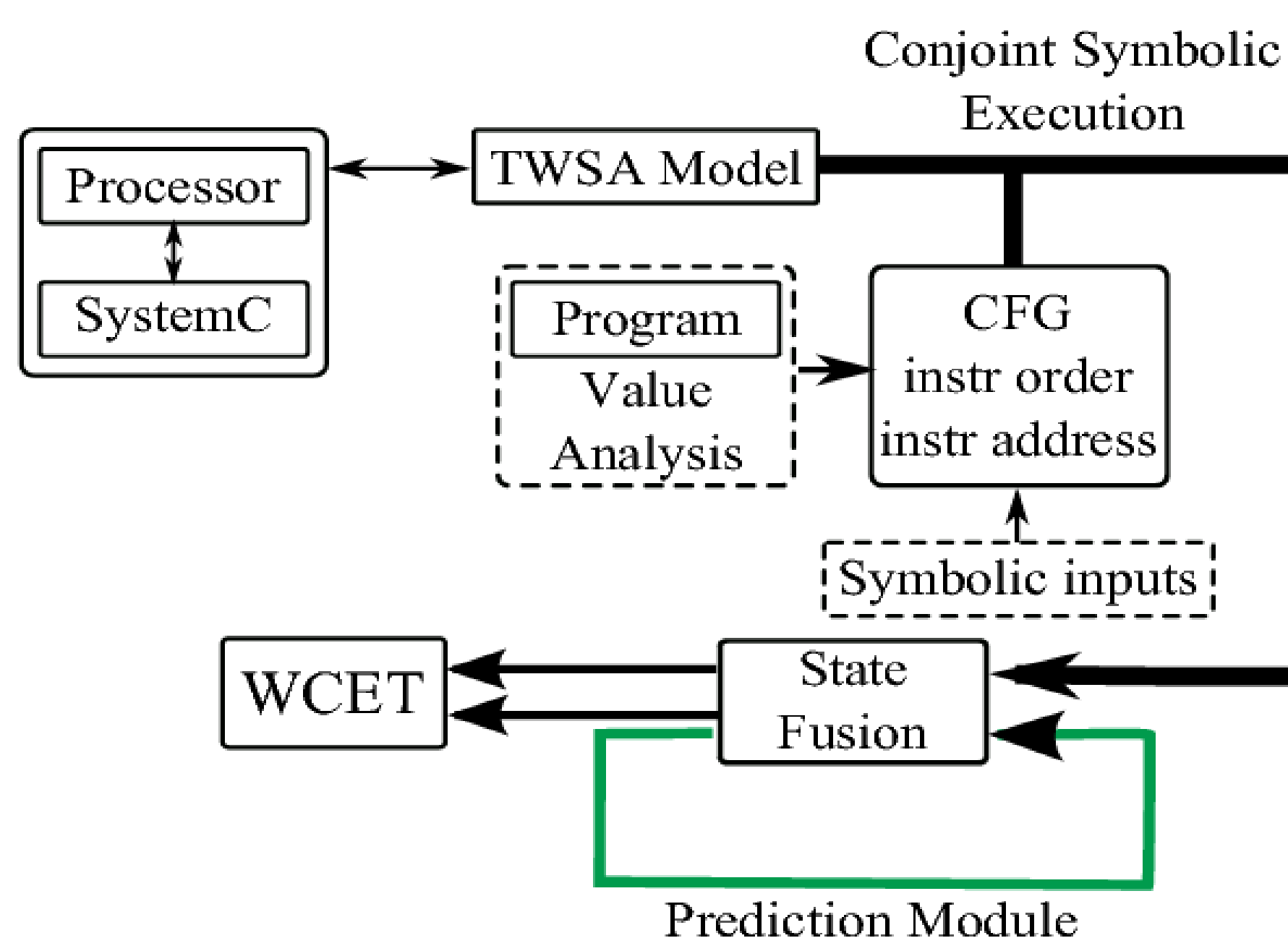


2. The worst case execution time analysis



Global approach

- Conjoint Symbolic Execution of the system model and the program
- With every executed instruction all reachable states of the processor are explored
- Handling the state space explosion with controlled precision:
 - Using the TWSA model that keeps only valid and relevant states and that gives a precise and yet compact representation of the global system.
 - Apply abstraction techniques to merge states and dynamically fusion states during the conjoint symbolic execution.
- Determining worst case behavior of the system



References

- N. Harrath, and B. Monsuez, Timed SystemC Waiting-State Automata, On Third International Workshop on Verification and Evaluation of Computer and Communication Systems, Rabat, Morocco, 2009.
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- B. Benhamamouch, B. Monsuez, Computing worst case execution time (wcet) by symbolically executing a time-accurate hardware model (extended version), International Journal of Design, Analysis and Tools for Circuits and Systems, Vol. 1, No. 1, 2009.
- B. Benhamamouch, B. Monsuez, F. Vdrine, Computing wcet using symbolic execution, Second International Workshop on Verification and Evaluation of Computer and Communication Systems, Leeds, England, 2008.

Results

- Modularity and adaptability to ever changing architectural models
- Generate the system model directly from the HDL code that served to create the system
- Ability to verify the correctness of the system model with regard to the upcoming certification standards

Future work

- Refine the SystemC model to capture precise information about the system behaviour.
- A joint study of system precision and dynamically changing architectures to give a precise estimation of WCET.