Study of short-circuit robustness of SiC MOSFETs, analysis of the failure modes and comparison with BJTs

Cheng Chen, Denis Labrousse, Stéphane Lefebvre, Mickael Petit, Cyril Buttay, Hervé Morel

Study of short-circuit robustness of SiC MOSFETs, analysis of the failure modes and comparison with BJTs

Cheng Chen[a,b], Denis Labrousse[a], Stéphane Lefebvre[a], Mickael Petit[a], Cyril Buttay[b], Hervé Morel[b]

[a]*SATIE, CNAM, CNRS, ENS Cachan, 61 Av. du Président Wilson, 94234 Cachan, France*
[b]*Ampère, INSA-Lyon, Bâtiment Léonard de Vinci, 69621 Villeurbanne, France*

Abstract

This paper presents experimental robustness tests made on Silicon Carbide (SiC) MOSFETs and SiC Bipolar Junction Transistors (BJTs) submitted to short-circuit operations (SC) or current limitation modes. For SiC MOSFETs, a gate leakage current is detected before failure without being responsible for the immediate failure. Nevertheless this gate leakage current is not without effect on the integrity of the SiC MOSFETs. Based on several robustness tests performed on SiC MOSFETs and on the comparison with experimental results obtained with SiC BJTs, the paper points out two main failure modes for SiC MOSFETs. The first one results in a simultaneously short circuit between drain and gate and drain and source and the second one in a degradation of the insulation between gate and source leading to a short circuit between gate and source. For some tested devices, the failure appears in a very interesting open state mode between drain and source after physical short-circuit between gate and source with a mode of failure very similar to those observed for SiC BJT.

Keywords: SiC; MOSFET; BJT; short circuit

1. Introduction

Various scientific literatures reported the excellent switching performances of silicon carbide (SiC) power devices in large market applications [1,2]. From an industrial point of view, aside from switching performances, the robustness is also a major feature which has to be considered for power conversion systems [3]. By comparison to Si ones, SiC MOSFETs possess smaller oxide thickness, coupled with a higher electric field for a given gate bias. This can make these devices sensitive to electron tunneling into and through gate oxide. Tunneling current is one of the main degradation mechanisms on gate oxide layer to SiC power MOSFETs [4]. Short circuit with high current density and high electric field in the oxide may increase the tunneling effect. So, it is of the first importance to carry out studies on the SC capability of SiC MOSFETs. In this paper, short circuit tests are achieved on two types of 1200 V SiC MOSFETs (respectively A and B MOSFETs) manufactured by Cree (CMF20120 and C2M0080120) and a third type of MOSFETs (C-MOSFET) from Rohm (SCT2080KE), and compared to SC tests performed on 1200V SiC BJT. Destructive tests are carried out in order to analyze the behavior of the different SiC MOSFETs under SC but also to analyze the mechanisms of failure. Similar behavior between MOSFETs and BJTs will help to understand some of the origin of the failure modes.

TABLE 1: ELECTRICAL CHARACTERISTICS OF TESTED POWER SIC DEVICES

	V_{BR} (V)	$I_{D(max)}$ (A)	On-state performance
A-MOSFET	1200	42.0	$R_{DS(on)}$ = 80 mΩ
B-MOSFET	1200	31.6	$R_{DS(on)}$ = 80 mΩ
C-MOSFET	1200	40.0	$R_{DS(on)}$ = 80 mΩ
BJT	1200	20.0	$V_{CE(on)}$ = 0.85V

Fig. 1 shows the schematic of the experimental setup proposed to perform the short circuit tests for MOSFETs or BJTs. The IGBT mounted into the test bench is used to keep the device under test (DUT) from further damage after short-circuit failure. MOSFETs are turned on and off through a voltage varying between 18V and -5V respectively. The gate driver was also adapted to SiC BJT.

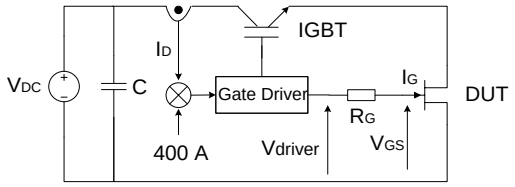

Fig. 1 Schematic of short-circuit test circuit for MOSFET

Critical energy E_C, which is an essential feature of robustness to power devices, refers to the minimal dissipated energy that leads to the failure of the tested device after one short-circuit. With the purpose of estimation of critical energy, the short-circuit duration is regularly increased from a low value (where the device is able to turn-off the SC current) up to the failure appears. The maximum energy the device is able to sustain during a safe short-circuit test is recorded as critical energy. In the current limitation mode, the DUT is maintained in an on-state during a very long short-circuit duration. The failure appears as the component is held in a conductive state.

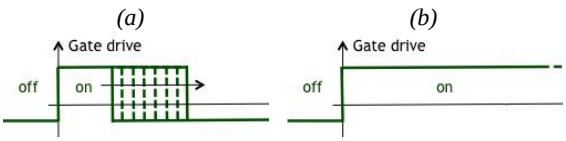

Fig. 2 Robustness tests under (a) short-circuit and (b) current limitation.

Meanwhile, influence of gate driver resistor and of temperature (from 25°C up to 150°C) on robustness will be investigated.

2. Failures under long duration short-circuits

2.1. Experimental results for SiC BJTs

Fig. 3 plots evolutions of waveforms on a BJT under destructive SC tests measured for a base current (I_B) equals to 0.2 A and 0.6 A. The saturation collector current is proportional to base current, since it is around 3 time higher for I_B = 0.6 A than that for I_B = 0.2 A. A sudden decrease of the base voltage (V_{BE}) from 10 µs after SC is observed for I_B = 0.6 A. This failure observed on the voltage between base and emitter can be explained by the fusion of metallization which is responsible for a short-circuit between base and emitter contacts. Without voltage drop on base-emitter junction, I_B increased to 0.4 A and collector current (I_C) was driven to zero after failure. Collector voltage remains equal to +600 V that implies no failure occurs between collector ans emitter electrodes, and failure appears in a safe status for the power electrodes (collector and emitter). Similar behavior is also observed for a lower base current after a longer time (30 µs) due to a lower dissipated energy, with a gradually decrease of the base voltage caused by the temperatue increae of the die.

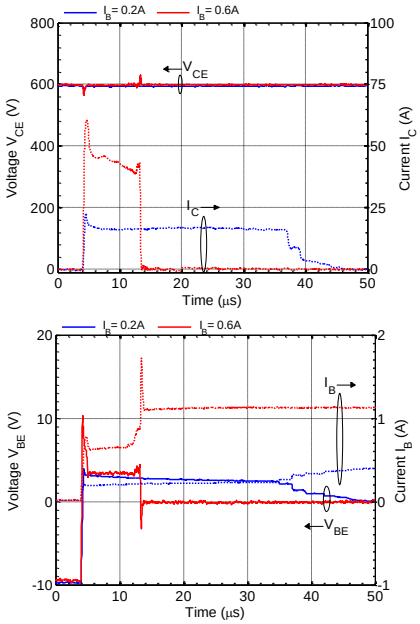

Fig. 3 Failure of BJT for T_{CASE} = 25°C.

2.2. Experimental results for SiC MOSFETs

The first set of destructive tests are performed with a DC bus voltage (V_{DC}) equals to 600 V and temperature of the case (T_{case}) equals to 25°C. The duration of short circuit (t_{SC}) is set up long enough (80 µs) to ensure the presence of failure under every single test. The waveforms recorded during failure are shown on Fig. 4 for A-MOSFET. After a peak of drain current due to temperature increase (reduction in the threshold voltage), a significant decrease to about 100 A about 10 µs after SC is noticed due to the reduction in carrier mobility with higher temperature growth. In addition, gate voltage (V_{GS}) falls gradually after few µs to the occurrence of failure. The decrease of V_{GS} results from the occurrence of a leakage current between gate and source measured during the tests. This particular behavior has already been shown on other SiC

MOSFETs in [5] where the increase of this leakage current has been explained by tunneling effect. Maximum gate leakage current is about 100 mA. In these current limitation operations, failure appears with simultaneous gate-drain and drain-source short-circuits. Similar results have been observed for B-MOSFET [6].

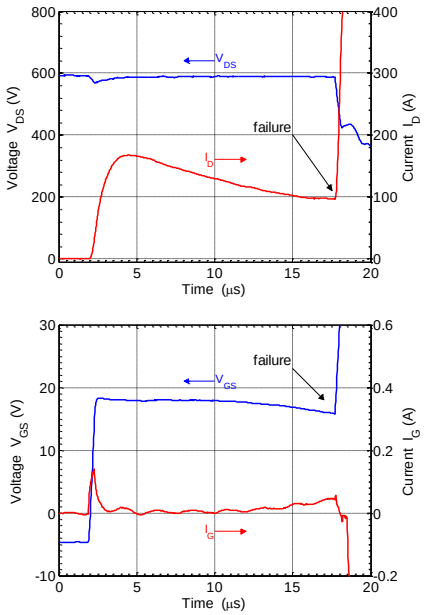

Fig. 4. Destructive test for A-MOSFET, $R_G = 47\ \Omega$, $T_{CASE} = 25°C$.

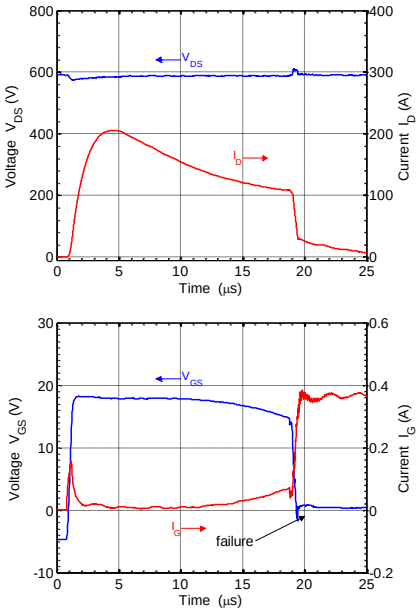

Fig. 5 Destructive test of C-MOSFET#1, $R_G = 47\ \Omega$, $T_{CASE} = 25°C$.

A failure between gate and source after about 19 µs was observed for C-MOSFET under the same experimental conditions (Fig. 5). The failure results in a short circuit between gate and source. Moreover, it seems that the failure between gate and source allows switching off the drain current and allows protecting the device from destruction between drain and source. In this condition, the failure between gate and source self-protects power electrodes. The same phenomenon has been observed for SiC BJT, which is a very interesting safe failure. For other tested C-MOSFETs, the first failure between gate and source was also observed with the suppression of the channel. Moreover a drain leakage current of approximate 50 A is high enough to be responsible for a thermal runaway depicted in Fig. 8 and in [6]. In this case a dramatic delayed failure appears between drain and source which is finally very similar to that observed for A and B MOSFETs.

2.3. Discussions

All tested MOSFETs waveforms during long short circuit operations show the occurrence of a gate leakage current after few µs of short-circuit. This gate leakage current is specific to SiC devices and is not observed on Si components. Nevertheless, there is no indication after these initial observations proving that this leakage current is responsible for the failure. Table 2 summarizes the experimental results for these different tests on SiC devices.

TABLE 2: SUMMARY OF SC TESTS ON MOSFETS AND BJT

	t_{fail} (µs)	E_{SC} (mJ)	Failure mode	N_{fail}/ N_{total}
BJT(I_B=0.6A)	32.0	348	SC_{BE} & OC_{CE}	2/2
MOS-A	16.0	1118	SC_{GD} & SC_{DS}	5/5
MOS-B	12.5	714	SC_{GD} & SC_{DS}	5/5
MOS-C #1	18.0	1567	SC_{GS} & OC_{DS}	2/6
MOS-C #2 [6]	17.5	1582	SC_{GS} & OC_{DS} then SC_{DS}	4/6

(V_{DC} = 600V, T_{CASE} = 25°C) where t_{fail} is the failure time, E_{SC} is the dissipated energy leading to failure, N_{fail} is the device number in this failure mode, N_{total} is the total number of device under test, (SC_{GS}) refers to short-circuit between gate and source, (OC_{DS}) refers to open-circuit between drain and source.

The tested BJTs show a failure leading to a SC between base and emitter and an open circuit between collector and emitter. The short circuit between base and emitter controls the collector current and leads to “safe” failure between collector and emitter. A physical short circuit can be involved between base and emitter, such as melting of the emitter aluminum metallization and/or base, which short-circuits the two electrodes. A similar safe mode of failure has been observed for C-MOSFETs, and for some of them followed by a delayed failure between drain and source. Nevertheless a first SC

failure between gate and source has been observed for these devices. For A and B MOSFETs, observed failure mode is very similar to those encountered in Si devices with uncontrollable gate-drain and drain-source failures.

3. Effect of case temperature on SiC MOSFET robustness

Fig. 6 shows the waveforms measured on A-MOSFET under destructive short circuit stress for T_{CASE} = 25°C and 150°C. The dissipated energy leading to failure is about 1.21 J for T_{CASE} = 25°C and 1.10 J for T_{CASE} = 150°C.

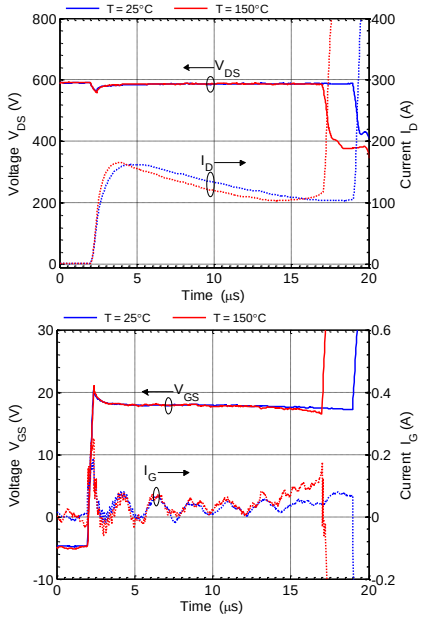

Fig. 6 Failure of A-MOSFET: drain and gate waveforms, for R_G = 10 Ω, T_{CASE} = 25°C and 150°C.

The dissipated energy the device can sustain decreases by only 10% when ambient temperature is varying from 25°C to 150°C. Another set of tests on C-MOSFETs are performed with gate driver resistor R_G = 47 Ω. First failures between gate and source is observed 21 µs after SC with dissipated energy of 1.58 J and 1.46 J for 25°C and 150°C respectively in [6]. According to these experiments, results show little dependence of robustness of SiC MOSFETs on the case temperature. Experimental and numerical results presented in [4] and [7] propose that even if the initial case temperatures are different, the increase of the die metallization temperature beyond a critical value (e.g. melting temperature of aluminum metallization of 900 K) is responsible for device failure. Under these conditions it is understandable that the SiC MOSFET robustness is little affected by the ambient temperature varying between 25 °C and 150 °C.

4. Effect of gate resistor on SiC MOSFET robustness

A significant gate leakage current appears during SC. In this part, we will analyze the effect of the maximum leakage current on the robustness of the devices.

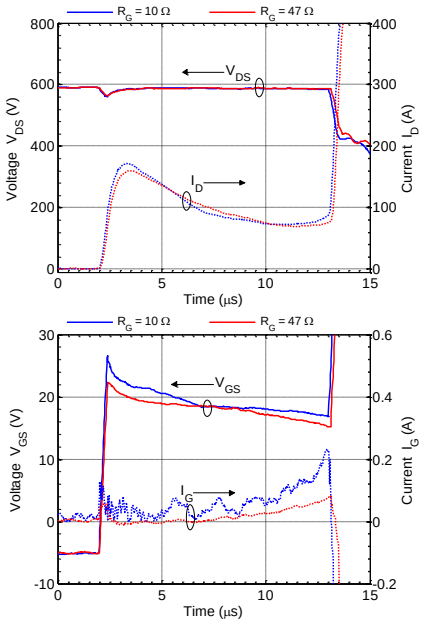

Fig. 7 Failure of B-MOSFET: drain and gate waveforms, at T_{CASE} = 150°C for R_G = 10 Ω and 47 Ω.

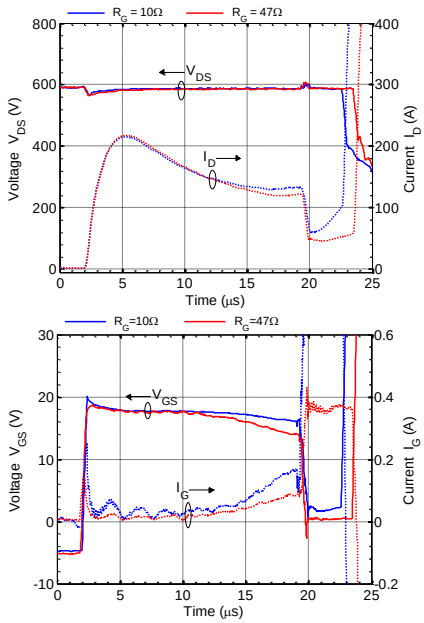

Fig. 8 Failure of C-MOSFET: drain and gate waveforms, at T_{CASE}= 25°C for R_G = 10 Ω and 47 Ω.

B-MOSFET was tested for two values of gate

resistance (10 and 47Ω). We observe a lower gate leakage current for R_G = 47Ω (Fig. 7). Nevertheless, in both cases the failure appears almost at the same moment and dissipated energies leading to failure are very closed, estimated about 669 mJ and 660 mJ for R_G = 10 and 47 Ω respectively. Fig. 8 reports waveforms of C-MOSFET measured at ambient temperature T_{CASE} = 25°C. First failure appearing simultaneously, C-MOSFET is capable to sustain dissipated energy about 1.61 J for R_G = 10 Ω and 1.59 J for R_G = 47 Ω. As dissipated energies until failure are much close, we have not noticed any proof of improving robustness by increasing gate resistance values. These results tend to show that the gate leakage current appearing during SC of SiC MOSFETs is not responsible for the first device failure. A failure mode of thermal origin should be considered.

5. Robustness of SiC MOSFETs under short circuit and critical energy estimation

A series of non-destructive short circuit tests are carried out for the purpose of critical energy evaluation. The critical energy is estimated by successive short circuit tests with t_{SC} increasing by step of 1 µs until MOSFET failed. The first results on A-MOSFET are presented in [6]. For test duration of 10 µs and 11 µs, after A-MOSFET turns off, current returns to zero. For test duration equal to 12 µs the gate to source voltage controls the drain current, but few µs after the drain current switch off, failure appears with a short-circuit between the three terminals of the device. The estimated critical energy is about 852 mJ corresponding to 11 µs, whereas this device failed for duration t_{SC} = 12 µs, which is similar to failure of B-MOSFET. A sample of C-MOSFET does not present a failure until duration reaching to 12 µs as well as A-MOSFET (Fig. 9). However its critical energy is about 1.06 J for duration of 11 µs, 24% higher than that of A-MOSFET. Due to gate failure, gate and source terminals were shorted 11 µs after turning-off. On the other hand, drain voltage still takes +600V and drain current is maintained to zero, which indicates the drain electrode is not degraded. In these conditions, the failure between is characterised by a short circuit between gate and source which allow maintaining a safe off-state between drain and source. This particular mode of failure is attractive to power electronics applications.

Similar tests have been extended to B-MOSFET, but this time with a gradual increase in the SC duration varying from 4 to 15.8 µs by steps of 100 ns. Results are represented on Fig. 10.

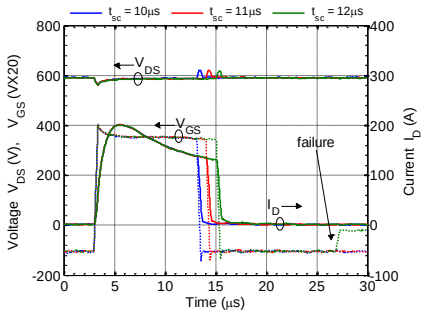

Fig. 9 Short circuit behavior of C-MOSFET for R_G = 10 Ω and T_{CASE} = 150°C.

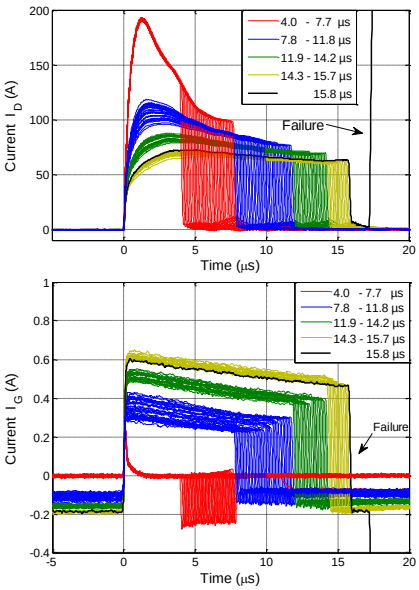

Fig. 10 Ageing of SiC B-MOSFETs during repetitive SC by increasing SC duration with a low time step.

These results clearly show that while the transistor is able to sustain SC up to 15.7 µs, irreversible damage appears during a sequence of short circuit cycles with an increase in test duration. The drain saturation current decreases, in contrast the gate leakage current increases. The evolution of drain current is not continuous which seems to be a consequence to a physical degradation of the device. At the same time a permanent leakage current in reverse bias also increases stepwise. It is important to note that these degradations appear after a short circuit time of only about 7.8 µs, which also corresponds to the appearance of the gate leakage current during the short-circuit phase. These results show that the gate leakage current seems to have a significant effect on the robustness of SiC MOSFETs.

6. Ageing of SiC MOSFETs under short circuit

Previous studies have shown that for short short-circuit duration (before apparition of the gate leakage

current) SiC MOSFET are able to sustain a number of short-circuit operations. Here, we will observe the behaviour of these devices with relatively longer short-circuit duration that is not able to cause the failure under a single SC stress. Short circuit duration of 9 µs has been chosen for B-MOSFETs. Results are presented in Fig. 11, where only gate and drain currents are presented.

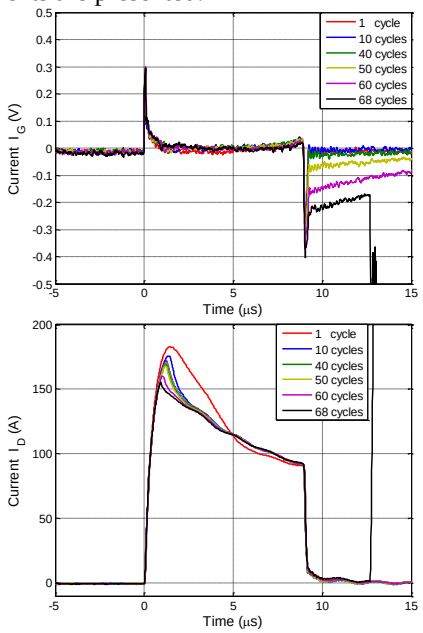

Fig. 11 Ageing of B-MOSFETs during repetitive SC, t_{SC} = 9µs repetition, R_G = 10 Ω, T_{CASE} = 25°C

These results clearly show a very low robustness in the repetition of the short-circuit events in this case, when the short-circuit duration is sufficiently long enough to bring about the gate leakage current. We observe a regular decrease of the drain saturation current and the appearance of a significant leakage current at turn-off.

7. Conclusion

The results presented in this paper show that failure modes of some SiC MOSFETs in short circuit operation are comparable to those observed for SiC bipolar transistors, with a short circuit between gate and source (respectively base and emitter) that provides a safe open circuit between drain and source (collector and emitter respectively) and, in fact, self protection of the circuit. This failure mode is extremely interesting from an application point of view and can be correlated to the melting of the metallization.

Robustness tests on SiC MOSFETs show good robustness in the case of long-term short circuit with the possibility to control the opening of the current until a short-circuit duration in the order of 10 to 15 µs. These tests, however, revealed the occurrence of a leakage current between gate and source that is specific to SiC MOSFETs and which appears only few µs after the beginning of the short-circuit. This gate leakage current seems not to be directly responsible for the failure of transistors in the case of single long-term short circuit events. In contrast, we have shown that, once we repeat sufficiently long short circuit duration to bring up this gate leakage current, irreversible damages appear and the repetition of just a few short circuits could cause the failure of transistors. In these circumstances it would be important to limit the robustness of the SiC MOSFETs under short-circuit operations to short circuit durations of less than the onset of this leakage gate grid; in the case of transistors tested here under 600V (half of the breakdown voltage) only to about 5us.

References

[1] A. Knop, W. T. Franke, and F. W. Fuchs, "Switching and conducting performance of SiC-JFET and ESBT against MOSFET and IGBT," *2008 13th Int. Power Electron. Motion Control Conf. EPE-PEMC 2008*, pp. 69–75, 2008.

[2] M. S. Chinthavali, B. Ozpineci, and L. M. Tolbert, "High-temperature and high-frequency performance evaluation of 4H-SiC unipolar power devices," *Conf. Proc. - IEEE Appl. Power Electron. Conf. Expo. - APEC*, vol. 1, pp. 322–328, 2005.

[3] M. Riccio, a. Castellazzi, G. De Falco, and a. Irace, "Experimental analysis of electro-thermal instability in SiC Power MOSFETs," *Microelectron. Reliab.*, vol. 53, no. 9–11, pp. 1739–1744, 2013.

[4] A. Fayyaz, L. Yang, and A. Castellazzi, "Transient robustness testing of silicon carbide (SiC) power MOSFETs," *15th Eur. Conf. Power Electron. Appl. EPE 2013*, 2013.

[5] D. Othman, S. Lefebvre, M. Berkani, Z. Khatir, a. Ibrahim, and a. Bouzourene, "Robustness of 1.2kV SiC MOSFET devices," *Microelectron. Reliab.*, vol. 53, no. 9–11, pp. 1735–1738, 2013.

[6] C. Chen, D. Labrousse, S. Lefebvre, M. Petit, C. Buttay, and H. Morel, "Robustness of SiC MOSFETs in short-circuit mode," *Proc. 2015 PCIM Eur.*, pp. 611–618, 2015.

[7] C. Abbate, G. Busatto, and F. Iannuzzo, "Operation of SiC normally-off JFET at the edges of its safe operating area," *Microelectron. Reliab.*, vol. 51, no. 9–11, pp. 1767–1772, 2011.