



HAL
open science

Low-frequency noise spectroscopy of bulk and border traps in nanoscale devices

E. Simoen, Bogdan Cretu, W Fang, M. Aoulaiche, Jean-Marc Routoure, Régis Carin, J Luo, Chao Zhao, Cor Claeys

► **To cite this version:**

E. Simoen, Bogdan Cretu, W Fang, M. Aoulaiche, Jean-Marc Routoure, et al.. Low-frequency noise spectroscopy of bulk and border traps in nanoscale devices. *Solid State Phenomena*, 2016, 242, pp.449. 10.4028/www.scientific.net/SSP.242.449 . hal-01196556

HAL Id: hal-01196556

<https://hal.science/hal-01196556>

Submitted on 1 Sep 2020

HAL is a multi-disciplinary open access archive for the deposit and dissemination of scientific research documents, whether they are published or not. The documents may come from teaching and research institutions in France or abroad, or from public or private research centers.

L'archive ouverte pluridisciplinaire **HAL**, est destinée au dépôt et à la diffusion de documents scientifiques de niveau recherche, publiés ou non, émanant des établissements d'enseignement et de recherche français ou étrangers, des laboratoires publics ou privés.

Low-frequency noise spectroscopy of bulk and border traps in nanoscale devices

SIMOEN Eddy^{1,2, a *}, CRETU Bogdan^{3, b}, FANG Wen^{4, c}, AOULAICHE Marc^{5, d},
ROUTOURE Jean-Marc^{6, e}, CARIN Regis^{6, f}, LUO Jun^{4, g}, ZHAO Chao^{4, h}
and CLAEYS Cor^{1,7, i}

¹ Imec, Kapeldreef 75, B-3001 Leuven, Belgium

² also at Depart. of Solid-State Sciences, Ghent University, 9000 Gent, Belgium

³ ENSICAEN, UMR 6072 GREYC, F-14050, Caen, France

⁴ Key Laboratory of Microelectronic Devices & Integrated Technology, Institute of Microelectronics, Chinese Academy of Sciences, Beijing, 100029, China

⁵ presently at Micron Technology Belgium, imec Campus, Belgium

⁶ University of Caen, UMR 6072 GREYC, F-14050, Caen, France

⁷ also at E.E. Dept., KU Leuven, Leuven, Belgium

^a eddy.simoen@imec.be, ^b bogdan.cretu@ensicaen.fr, ^c fangwen@ime.ac.cn,

^d marc.aouliache@imec.be, ^e jean-marc.routoure@unicaen.fr, ^f regis.carin@unicaen.fr,

^g luojun@ime.ac.cn, ^h zhaochao@ime.ac.cn, ⁱ cor.claeys@imec.be

Keywords: Random Telegraph Signal; silicon-on-insulator; gate oxide trap; metal-oxide-semiconductor field-effect transistor, generation-recombination noise

Abstract. The principles and application of Generation-Recombination (GR) noise spectroscopy will be outlined and illustrated for the case of traps in Ultra-Thin Buried Oxide Silicon-on-Insulator nMOSFETs and for vertical polycrystalline silicon nMOSFETs. It will be shown that for scaled devices the GR noise is originating from a single defect, giving rise to a so-called Random Telegraph Signal (RTS). Several methods will be described for an accurate extraction of the RTS parameters (amplitude, up and down time constant). It will be demonstrated that besides the deep-level parameters also the position of the trap in the channel can be derived from a numerical modeling of the RTS amplitude.

Introduction

Performing defect spectroscopy in nano-scaled structures is a challenging endeavor. One technique which appears to be very suitable for this task is Generation-Recombination (GR) noise spectroscopy [1]. Originally, the method has been developed for rather large area semiconductor devices, like, e.g., MOSFETs [1-4], Charge-Coupled Devices [5] or Junction Field-Effect Transistors [6] to study deep levels in the semiconductor depletion region. It is an alternative to the popular Deep Level Transient Spectroscopy (DLTS) technique [2], the main difference being that the GR centers are studied in dynamic equilibrium, i.e., the noise is due to subsequent capture and emission of free carriers, while in DLTS an emission transient is monitored after trap filling. If the GR events are mainly related to either the valence (p-type) or conduction band (n-type material), the corresponding low-frequency (LF) noise spectrum is a Lorentzian as a function of the frequency and it is the result of fluctuations in the current through the device by alternating carrier capture and emission from a deep-level trap. The advantage of GR noise spectroscopy compared with DLTS is that it can be applied to any device size, since the LF noise Power Spectral Density (PSD) generally scales with $1/A$ [7], with A the active device area, implying that the relative noise amplitude becomes higher for smaller devices. As a consequence, GR noise may become the dominant LF noise source in small-area MOSFETs and can be caused by a single defect [8]. At the same time, discrete switching of the device current as a function of time becomes visible and corresponds in the most simple case to the charging (carrier capture) and discharging (emission) of a single trap. Such

behavior in the time domain is called a Random Telegraph Signal (RTS) and its parameters (amplitude, up and down times) can equally be used for deep-level characterization [8].

In this paper, an overview will be given regarding GR noise and RTS spectroscopy in MOSFETs. It will be outlined how the main defect level parameters (activation energy E_T ; capture cross section for holes (electrons) $\sigma_{p,n}$ and trap concentration N_T) can be derived from the Lorentzian noise spectrum as a function of temperature T . In the case of single-defect RTSs, the same information can be extracted from time domain measurements. In addition, it will be shown that studying the gate voltage (V_G) or drain voltage (V_D) dependence of the RTS amplitude yields in many cases information on the position of the trap. Criteria will be proposed to distinguish Lorentzian noise belonging to an ensemble of traps in the depletion region of a semiconductor material or to a single defect in the gate dielectric. The methods will be illustrated for processing-induced defects present in the silicon film of Ultra-Thin Buried Oxide (UTBOX) Silicon-on-Insulator (SOI) MOSFETs and for RTSs present in the polysilicon layer of a vertical transistor for Non-Volatile Memory (NVM) applications [9,10].

Principle of GR Noise and RTS Spectroscopy

GR Noise. As schematically shown in Fig. 1, the GR noise power spectral density (PSD) (S_I) exhibits a plateau A_0 at low frequency (f) and a $1/f^2$ roll-off, corresponding to [1-4]:

$$S_I = A_0 / [1 + (f/f_0)^2] \quad (1)$$

with $f_0 = 1/2\pi\tau_0$ the characteristic frequency of the GR center and τ_0 the characteristic time constant, given by the Shockley-Read-Hall (SRH) expression [1-4]:

$$\tau_0 = 1/(2\pi f_0) = [c_n(n(x,y) + n_t) + c_p(p(x,y) + p_t)]^{-1} \quad (2)$$

with c_n , c_p the capture coefficient for electrons and holes at position (x,y) in the channel, respectively, given by the product of the corresponding capture cross section and thermal velocity, i.e., $c_n = \sigma_n v_{thn}$. Further, we have that $n(x,y)$ and $p(x,y)$ are the free electron and hole densities and n_t and p_t is the free electron or hole density when the Fermi level E_F coincides with the trap level E_T . In the depletion region of a bulk or a partially depleted MOSFET, one can neglect the minority carrier terms in Eq. (2) so that the characteristic time constant can be approximated by the sum of an emission (τ_e) and a capture term (τ_c):

$$1/\tau_0 = 1/\tau_e + 1/\tau_c \quad (3)$$

The characteristic frequency can be determined from a plot of $f \times S_I$ versus f , resulting in a peak with a maximum occurring at f_0 . In general, a LF noise spectrum may consist of different Lorentzians, occurring at different f_{0i} , a $1/f$ noise component K_f/f and frequency-independent white noise (PSD B_w) [11,12]. Fitting of the following expression:

$$S_I f = B_w f + K_f + \sum_{i=1}^j A_{0i} f / [1 + (f/f_{0i})^2] \quad (4)$$

gives accurate values for the parameters A_{0i} and f_{0i} of the $i=1, j$ Lorentzians in the spectrum [11,12]. Measuring the f_{0i} values at different sample temperatures enables to construct an Arrhenius law like in Fig. 2 [11,12]:

$$\ln(\tau_0 T^2) = \frac{E_C - E_T}{kT} + \ln \left(\frac{\hbar^3}{4k^2 \sigma_n \sqrt{6\pi^3 M_C m_e^{*1/2} m_n^{*3/2}}} \right) \quad (5)$$

In Eq. (5) k is the Boltzmann constant, h Planck's constant, M_c the equivalent minima in the conduction band, m_e^* and m_h^* the transport effective mass for electrons and holes, respectively. It is clear that from the slope of an Arrhenius plot one derives the activation energy $E_C - E_T$ and from the intercept the (electron) capture cross section. An example of an Arrhenius plot obtained on an UTBOX SOI nMOSFET is given in Fig. 2, showing an electron trap with activation energy $\Delta E = E_C - E_T = 0.42$ eV and 0.45 eV, respectively.

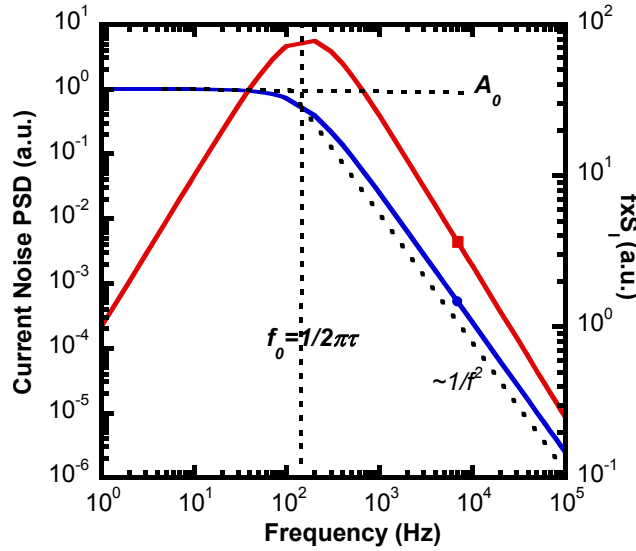


Fig. 1. Schematic representation of a Lorentzian noise spectrum and definition of its main parameters.

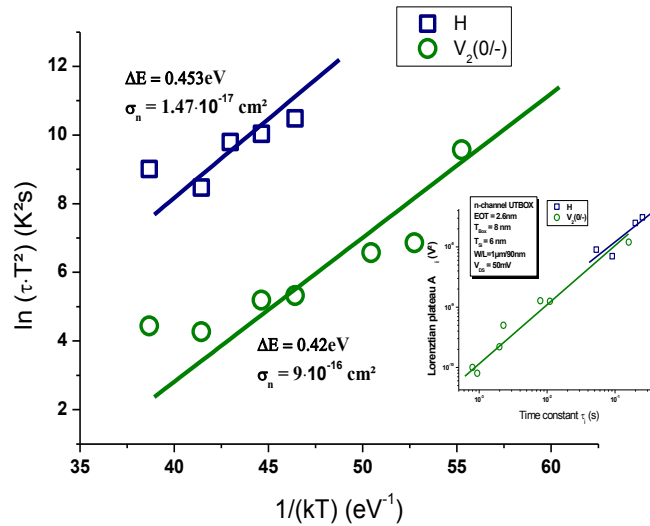


Fig. 2. Arrhenius plot obtained on an UTBOX SOI nMOSFET with area WL, silicon film thickness T_s and front gate oxide thickness T_{ox} , exhibiting two Lorentzian noise components. Inset shows the relationship between the plateau amplitude and the time constant.

Finally, the trap concentration N_T can be derived from [1,4,12]:

$$A_{0i} = \frac{q^2 N_e f f}{W L C_{ox}^2} \tau_{0i} = \frac{B q^2 W_d N_T}{W L C_{ox}^2} \tau_{0i} \tag{6}$$

with WL the effective width times the length of the transistor; C_{ox} the oxide capacitance density of the gate, q the elementary charge and W_d the width of the depletion region. In the case of a bulk or partially depleted SOI transistor, the empirical factor B is given by $1/3$ [1,4].

RTS. A typical time trace of a two-level RTS in a small-area MOSFET is given in Fig. 3, defining the main parameters: the current amplitude ΔI_D , the up time t_{up} and the down time t_{down} . From the histogram of the drain current (I_D) values, an average amplitude ΔI_D can be derived, while the time constant ratio τ_c/τ_e can be found from the ratio of the area under the two peaks in the amplitude histogram of Fig. 4 [13]. The inverse sum of the time constants can be obtained from the corner frequency of the corresponding Lorentzian spectrum [8,13] or by constructing the probability distribution of the up (t_{up}) and the down (t_{down}) time constants. They usually follow an exponential distribution, given by [8,13]:

$$P(t)=1/\tau \exp(-t/\tau) \quad (7)$$

whereby the average value corresponds to the capture (up time) or emission (down time) constant. Performing time domain analysis at different temperatures enables constructing an Arrhenius diagram from which the activation energy of carrier capture and emission is obtained [8].

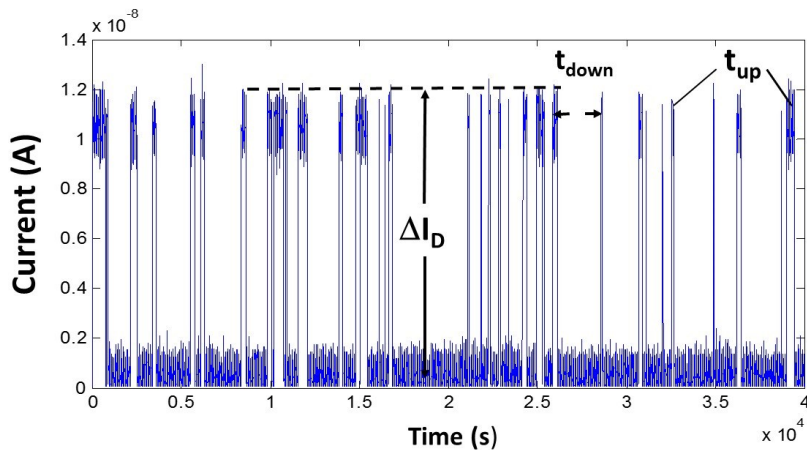


Fig. 3. Time series of the drain current obtained on a small-area MOSFET operated in weak inversion, showing a random two-level switching between a low and a high drain current state.

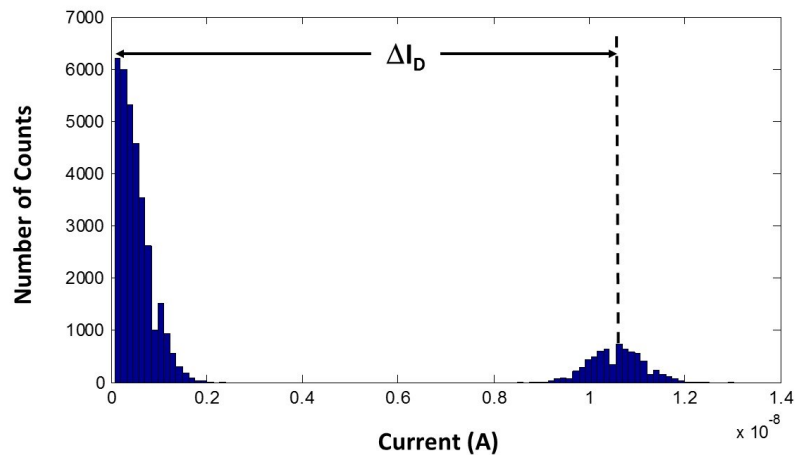


Fig. 4. Histogram of the amplitudes derived from the time series of Fig. 3.

In the case of a complex multilevel RT signal, like in Fig. 5 containing a small and a large amplitude signal, the usual time series analysis method may become inadequate. In order to discriminate multiple RTSs in the same time trace, one can rely on the statistical analysis of a so-called Time Lag Plot (TLP) which consists in the representation of the current at n^{th} sample $I_D(n)$ versus the current at $n+1^{\text{th}}$ sample $I_D(n+1)$ [13-15], taking into account the autocorrelation in time series data. One normally expects the TLP points to align along a diagonal, with higher intensity clouds corresponding with each discrete drain current level present in the time series. Improved TLP can be utilized to extract the centre of the data clouds, as shown in Fig. 6, by obtaining a value related to the probability of each data point in the cloud, which means the probability of observing the $n+1^{\text{th}}$ sample after the n^{th} sample. Moreover, a combination of the TLP with a so-called Hidden Markov modeling (HMM) approach can yield accurate RTS amplitude and time constants, even for RTSs hidden in large random noise [16].

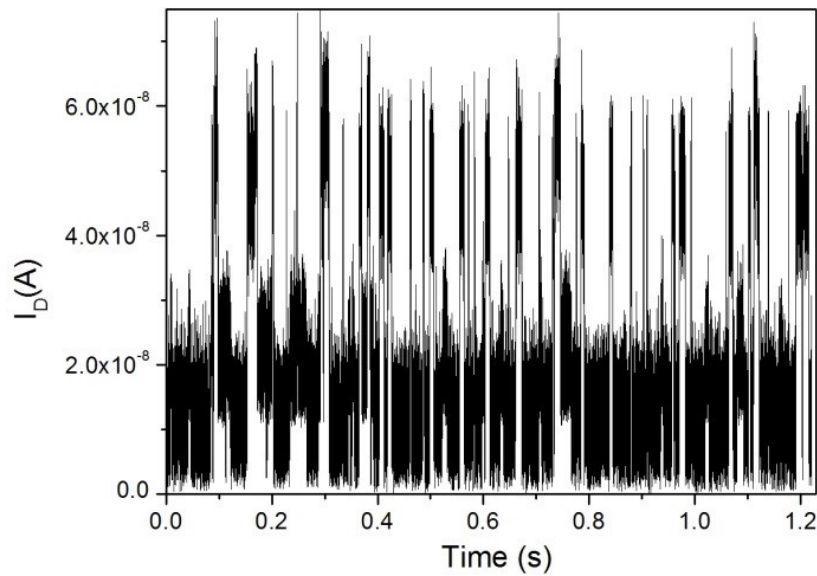


Fig. 5. Time series containing a large and a small RTS.

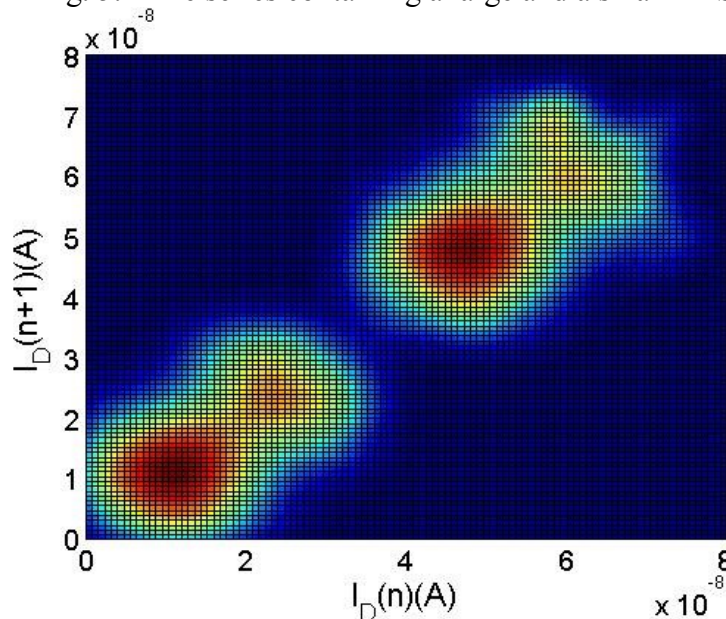


Fig. 6. Improved Time Lag Plot (TLP) analysis of the time series, revealing four drain current levels corresponding with two RTSs.

Finally, it can be shown that for an RTS due to a trap in the gate oxide, the analysis of the time constant ratio versus gate voltage [8,17] or drain voltage [18] yields the trap position in the gate oxide with respect to the silicon/dielectric interface or along the transistor channel, respectively.

GR Noise and RTS in UTBOX SOI MOSFETs

The structure of an UTBOX SOI MOSFET is schematically represented in Fig. 7a. The study of GR noise in such devices offers some unique opportunities given the fully-depleted nature of the ~ 10 nm thick silicon film [11,13,19]. Usually, it is assumed that Lorentzians which do not shift markedly with gate voltage in strong inversion belong to GR centers in the silicon depletion region [1-4]. An example is given in Fig. 7b. In that case, T-dependent GR noise spectroscopy as presented above can be applied [11,13,19]. Conversely, the Lorentzians corresponding with a gate-oxide RTS exhibit a clear gate-voltage dependence, like in Fig. 7c [13]. However, as pointed out recently [20], GR noise due to defects in the fully depleted film of an UTBOX SOI transistor can also show a strong variation of the corner frequency f_0 with gate bias in linear operation. This is related to the fact that both the Fermi level and the free carrier concentrations undergo a strong variation with front- (V_{GS}) and back-gate bias (V_{BS}), resulting in a gate-bias dependent change in the SRH time constant of Eq. (2).

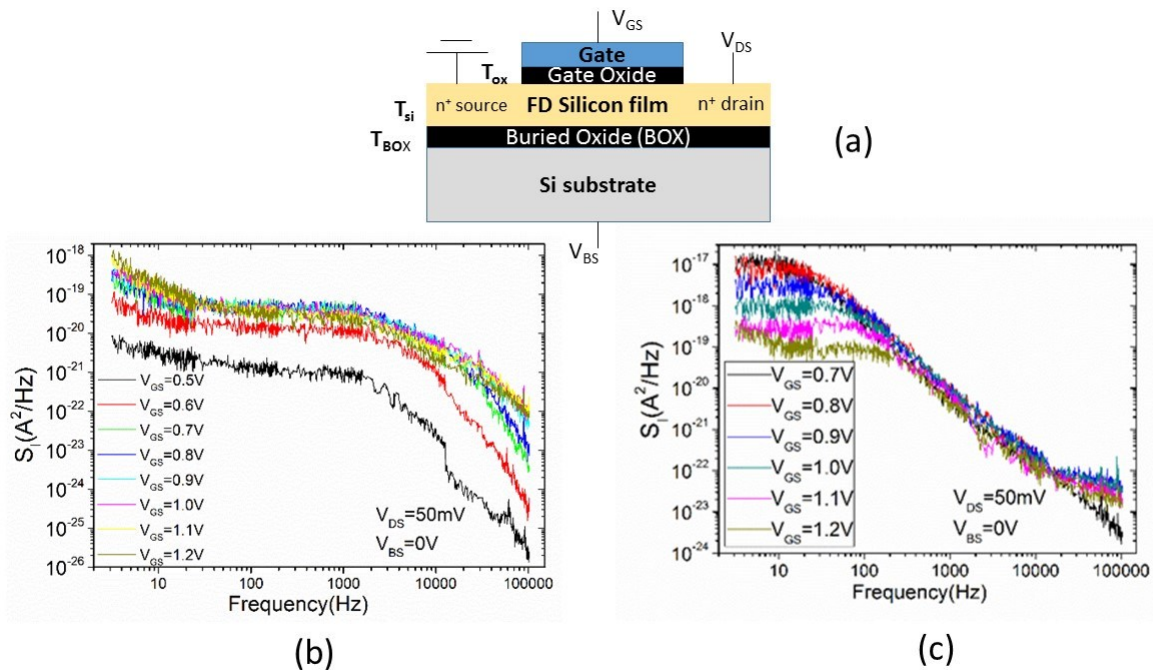


Fig. 7. (a) Schematic representation of a FD UTBOX SOI nMOSFET. (b) Lorentzian GR noise spectra for different front-gate biases in linear operation at a $V_{DS}=50$ mV and back-gate bias $V_{BS}=0$ V, showing little shift of the corner frequency and (c) showing a clear increase of the corner frequency with increasing front-gate voltage V_{GS} .

As a consequence, the distinction between RTS and GR noise becomes more complicated in the case of FD SOI transistors and more refined criteria have to be worked out [13,21]. A first possibility is to measure the noise in the front channel with the back channel biased in accumulation and next in the back channel current with the front channel accumulated [21]. In this way, the impact of the opposite interface and oxide is screened. When the Lorentzians are only present in one type of spectra, one may assume that they originate from traps in the corresponding oxide, while if the Lorentzians are present in both cases, there is a strong probability that the GR noise is due to defects in the fully depleted silicon film [21]. However, for ultra-thin films (<10 nm) the strong front-back coupling prevents accumulation of either of the interfaces so that this method may break down for deeply scaled technology nodes.

A second method relies on combining noise measurements with time domain measurements. At first sight, the presence of RTS in the drain current points to single traps in one of the gate oxides. Unfortunately, this criterion is also not sufficient for typical UTBOX SOI transistor sizes (i.e.,

$L=0.1\ \mu\text{m}$; $W=1\ \mu\text{m}$ and $t_{\text{film}}=10\ \text{nm}$), since the GR noise in such devices corresponds with only a few similar traps [19], as has also been derived from charge retention time measurements and modeling [22]. As a result, RTS has been found which could be ascribed to the capture and emission by a single GR center in the silicon film [19]. This has led to the development of a set of criteria, which are based on the RTS parameters and summarized in Table I [13]. One of the most important guidelines is based on the gate voltage behavior of the capture and emission time constant and their ratio. At sufficiently high drain currents, τ_c and τ_e become independent on V_{GS} and show a ratio close to 1, which is in strong contrast with the exponential dependence of τ_c on V_{GS} for an oxide RTS [8,17]. An additional benefit of the exploitation of film-related RTSs is that one can derive the position of the trap in the silicon film when combining with 2D or 3D device simulations [13].

A third possibility is to analyze the gate voltage dependence of the Lorentzian parameters based on 2D numerical simulations of the FD SOI UTBOX nMOSFET characteristics including a dedicated GR noise model [20]. This enables to perform GR noise spectroscopy at room temperature.

Table 1 Variation of RTS and Lorentzian parameters for a gate oxide and a film trap with front gate voltage in UTBOX SOI nMOSFETs, at constant V_{DS} .

Parameter	gate oxide RTN	film RTN
τ_c	expon. decrease	moderate decrease
τ_e	\sim constant	\sim constant
τ_c/τ_e	expon. decrease	~ 1
$\Delta I_{\text{D}}/I_{\text{D}}$	certain variation + nearly constant	decrease
$S_{\text{I}}(0)$	decrease	const. + increase

Application of standard T-dependent GR noise spectroscopy to the UTBOX SOI nMOSFETs has revealed the presence of around ten different deep level centers [11,23,24], which are believed to be processing-related, e.g., by ion implantation of the source/drain regions or by dry etching damage. Moreover, it has recently been shown that the empirical B factor in Eq. (5) is most likely smaller for FD transistors, compared with $\sim 1/3$ for PD or bulk devices [24].

GR Noise and RTS in Vertical Polysilicon MOSFETs

Vertical polysilicon n-channel transistors are potentially of interest for 3D Non-Volatile Memory (NVM) applications [9,10]. The structure is schematically represented in Fig. 8a, whereby the grain boundaries are a likely source of RTS in the drain current (Fig. 8b). Detailed noise measurements have indicated that there are two types of RTS present [10]: slow, large-amplitude signals, which are predominantly related to traps in the gate oxide or at the GBs and smaller amplitude signals, with faster time constants, which are believed to reside in the polysilicon channel. In order to validate this assumption, 3D device simulations have been executed, using the structure of Fig. 9, whereby the GR center location was varied along the channel between source and drain (positions A to C) and at the Si/SiO₂ interface or in the center of the cylinder (primed positions A', B' and C'). The RTS amplitude ΔI_{D} has been calculated as the difference in the current without $I_{\text{D}}(0)$ or with $I_{\text{D}}(-)$ a negatively charged electron trap present. As can be seen from Fig. 10, the RTS amplitude is a sensitive function of the trap location, so that a comparison with actually measured data should reveal the position of the trap along the channel and in diameter [10]. Again, as for oxide-related RTSs the study of the trap time constants as a function of temperature should provide the activation energy and can then be compared with DLTS results obtained on similar devices [9].

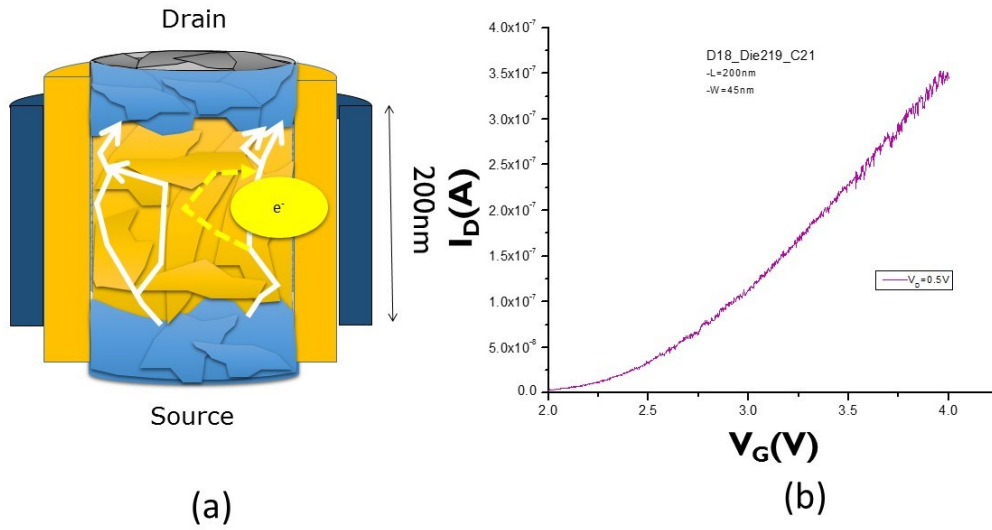


Fig. 9. (a) Schematic structure of a vertical polysilicon nMOSFET and (b) input characteristics (I_D - V_G) at fixed drain voltage $V_D=0.5$ V, showing the presence of small-amplitude RTS fluctuations.

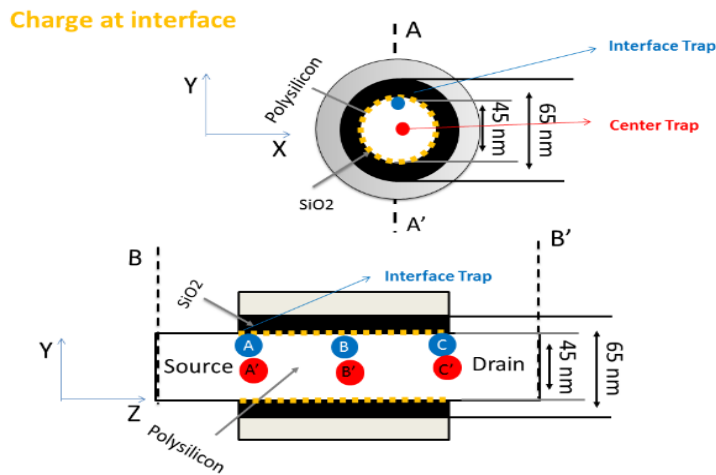


Fig. 9. Schematic structure of a polysilicon nMOSFET with bulk trap positions.

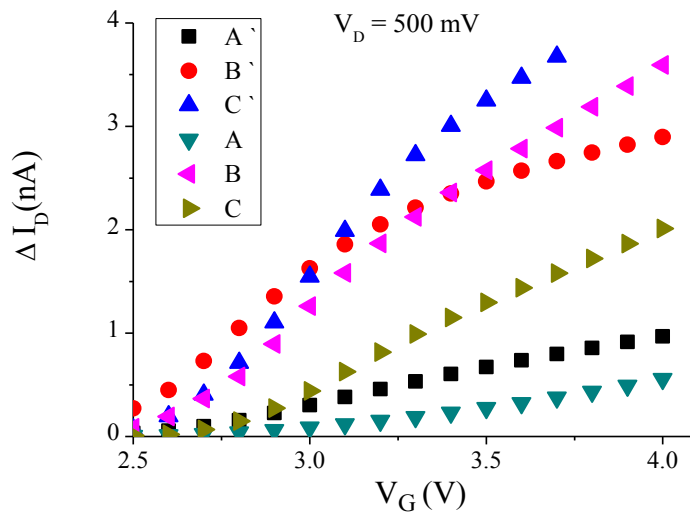


Fig. 10. Simulated RTS amplitude as a function of gate voltage corresponding with the different trap positions between source (S) and drain (D) defined in Fig. 9.

Summary

In this paper, it has been shown that Lorentzian noise, associated with trap-assisted GR events and measured on different kinds of MOSFETs enables the study of deep levels in deeply scaled devices. Traps either in the semiconductor, at its interface(s) or in the oxide can in principle be distinguished. The advantage of employing time domain measurements is that the RTS parameters can also be exploited for deriving the trap location of the single defect responsible for it. At the same time, scaling of the device dimensions leads to small active volumes, so that RTSs in the semiconductor itself start to contribute to the noise, which opens up new perspectives for deep-level studies.

References

- [1] N.B. Lukyanchikova, Sources of the Lorentzian components in the low-frequency noise spectra of submicron metal-oxide-semiconductor field-effect transistors, in: A. Balandin (Ed.) *Noise and Fluctuations Control in Electronic Devices*, American Scientific, Riverside, CA, 2002, pp. 201-233.
- [2] F. Scholz, J.M. Hwang, D.K. Schroder, Low frequency noise and DLTS as semiconductor device characterization tools, *Solid-St. Electron.* 31 (1988) 205-217.
- [3] D.C. Murray, A.G.R. Evans, J.C. Carter, Shallow defects responsible for GR noise in MOSFET's, *IEEE Trans. Electron Devices* 38 (1991) 407-416.
- [4] I. Lartigau, J.M. Routoure, W. Guo, B. Cretu, R. Carin, A. Mercha, C. Claeys, E. Simoen, Low temperature noise spectroscopy of 0.1 μm partially depleted silicon on insulator metal-oxide-semiconductor field effect transistors. *J. Appl. Phys.* 101 (2007) 104511/1-5.
- [5] T. Hardy, M.J. Deen, R.M. Murowinski, Low-frequency noise in proton damaged LDD MOSFET's, *IEEE Trans. Electron Devices* 46 (1999) 1339-1346.
- [6] V. Grassi, C.F. Colombo, D.V. Camin, Low frequency noise versus temperature spectroscopy of recently designed Ge JFETs, *IEEE Trans. Electron Devices* 48 (2001) 2899- 2905.
- [7] M. von Haartman, M. Östling, *Low-frequency noise in advanced MOS devices*, Springer (2007).
- [8] M.J. Kirton, M.J. Uren, Noise in solid-state microstructures: A new perspective on individual defects, interface states and low-frequency (1/f) noise, *Adv. in Physics* 38 (1989) 367-468.
- [9] M. Toledano-Luque, B. Tang, R. Degraeve, B. Kaczer, E. Simoen, J. Van Houdt, G. Groeseneken, Spectroscopic study of polysilicon traps by means of fast capacitance transients, *J. Vac. Sci. Technol. B* 31 (2013) 01A110/1-5.
- [10] M.G.C. de Andrade, M. Luque Tolenado, F. Fourati, R. Degraeve, J.A. Martino, C. Claeys, E. Simoen, G. Van den Bosch, J. Van Houdt, RTN assessment of traps in polysilicon cylindrical vertical FETs for NVM application, *Microelectron. Engrg.* 109 (2013) 105-108.
- [11] S.D. dos Santos, B. Cretu, V. Strobel, E. Simoen, J.-M. Routoure, R. Carin, M. Aoulaiche, M. Jurczak, J.A. Martino, Low-frequency noise assessment in advanced UTBOX SOI n-channel MOSFETs, *Solid-St. Electron.* 97 (2014) 14-22.
- [12] H. Achour, B. Cretu, J.-M. Routoure, R. Carin, R. Talmat, A. Benfdila, E. Simoen, C. Claeys, In depth static and low-frequency noise characterisation of n-channel n-FinFETs on SOI substrates at cryogenic temperature, *Solid-St. Electron.* 98 (2014) 12-19.
- [13] W. Fang, E. Simoen, M. Aoulaiche, J. Luo, C. Zhao, C. Claeys, Distinction between silicon and oxide traps using single-trap spectroscopy, *Phys. Stat. Sol. A* 212 (2015) 512-517.
- [14] S. Realov, K.L. Sheppard, Analysis of random telegraph noise in 45-nm CMOS using on-chip characterization system, *IEEE Trans. Electron Devices* 60 (2013) 1716-1722.

- [15] T. Tsuchiya, N. Tamura, A. Sakakidani, K. Sonoda, M. Kamei, S. Yamakawa, S. Kuwabara, Characterization of oxide traps participating in random telegraph noise using charging history effects in nano-scaled MOSFETs, *ECS Trans.* 58 (9), The Electrochem. Soc. (Pennington, NJ) (2013) 265-279.
- [16] M. Li, R. Wang, J. Zou, R. Huang, Characterization of Random Telegraph Noise in scaled high- κ /metal gate MOSFETs with SiO₂/HfO₂ gate dielectrics. *ECS Trans.* 52 (1) (2013) 941-946.
- [17] K.S. Ralls, W.J. Skocpol, L.D. Jackel, R.E. Howard, L.A. Fetter, R.W. Epworth, D.M. Tennant, Discrete resistance switching in submicrometer inversion layers: Individual interface traps and low-frequency ($1/f$) noise, *Phys. Rev. Lett.* 52 (1984) 228-231.
- [18] N.V. Amarasinghe, Z. Çelik-Butler, P. Vasina, Characterization of oxide traps in 0.15 μm^2 MOSFETs using random telegraph signals, *Microelectron. Reliab.* 40 (2000) 1875-1881.
- [19] E. Simoen, M. Aoulaiche, S. D. dos Santos, J.A. Martino, V. Strobel, B. Cretu, J.-M. Routoure, R. Carin, A. Luque Rodríguez, J.A. Jiménez Tejada, C. Claeys, Lessons learned from low-frequency noise studies on fully depleted UTBOX Silicon-on-Insulator nMOSFETs, *ECS J. of Solid St. Science and Technol.* 2 (2013) Q205-Q210.
- [20] A. Luque Rodríguez, J.A. Jiménez Tejada, S. Rodríguez-Bolívar, M. Aoulaiche, C. Claeys, E. Simoen, Dependence of generation-recombination noise with gate bias in FD SOI MOSFETs, *IEEE Trans. Electron Devices* 59 (2012) 2780-2786.
- [21] S. D. dos Santos, T. Nicoletti, J.A. Martino, M. Aoulaiche, A. Veloso, M. Jurczak, E. Simoen, C. Claeys. On the variability of low frequency noise of front/back-channels in UTBOX SOI nMOSFETs, *IEEE Trans. Electron Devices* 60 (2013) 444-450.
- [22] M. Aoulaiche, E. Simoen, M. Veloso, P. Blomme, G. Groeseneken, M. Jurczak, T. Nicoletti, L. Mendes Almeida, Junction field effect on the retention time for one Transistor Floating Body RAM memory, *IEEE Trans. Electron Devices* 59 (2012) 2167-2172.
- [23] E. Simoen, B. Cretu, W. Fang, M. Aoulaiche, J.-M. Routoure, R. Carin, S. dos Santos, J. Luo, C. Zhao, J.A. Martino, C. Claeys, Towards single-trap spectroscopy: Generation-Recombination noise in UTBOX SOI nMOSFETs, *Phys. Stat. Sol. C* 12 (2015) 292-298.
- [24] B. Cretu, E. Simoen, J.-M. Routoure, R. Carin, M. Aoulaiche, C. Claeys, Low frequency noise spectroscopy in rotated UTBOX nMOSFETs, to be published in the Proc. of ICNF 2015, Xi'an (China), 1-6 June 2015, The IEEE (New York).

Gettering and Defect Engineering in Semiconductor Technology XVI

10.4028/www.scientific.net/SSP.242

Low-Frequency Noise Spectroscopy of Bulk and Border Traps in Nanoscale Devices

10.4028/www.scientific.net/SSP.242.449