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Thermal management of lateral GaN power devices

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Abstract—This article investigates several thermal management techniques for GaN transistors with a Wafer-Level Packaging (WLP): advanced techniques are used to mount them on Direct-Bonded Copper (DBC) ceramic substrates, with the heat removed either through the topside of the die (as recommended by the manufacturer), or through the backside. The thermal resistance of the assembly is measured in the different configurations, for different die thicknesses. The paper describes the manufacturing process and the thermal simulation and experimental results will be shown.

Keywords—GaN power device; thermal management; Flex circuit; 3D packaging; flip-chip

I. INTRODUCTION

In the recent years, as the silicon technology has approached its theoretical limits, power devices made out of Gallium Nitride (GaN) have emerged as alternatives that outperform Si devices by overcoming the limitation of higher switching frequencies, efficiency and reliability [1]. As a wide bandgap material, GaN has a superior relationship between on-resistance and breakdown voltage due to its higher critical electric field strength. This allows devices to be more compact.

The studied GaN transistors are shown in Fig. 1. Provided by EPC, they are eGaN FET (enhancement mode, 40V - 33A) with a very small die size ($4075 \times 1602 \times 685 \mu\text{m}$) [2]. These devices are based on Si substrate and have a “lateral” structure, with all the terminals on the same side of the power die. As a consequence, they are equipped with solder bumps for “flip-chip” mounting. This is efficient from an electrical point of view, with very short distances between the active area of the GaN transistor and the other components. From a thermal point of view, however, this is not so efficient: the bumps have

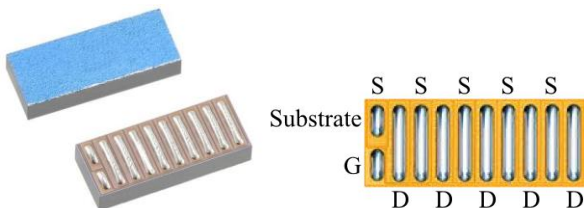


Fig. 1 EPC 2015 GaN transistor [2]

limited thermal conductivity, and cover only a fraction of the die surface area.

Therefore, it is worth comparing the thermal performance of GaN transistors cooled either through their bumps (topside cooling) or through their silicon substrate (backside cooling). We also compare the thermal performance of die mounted on ceramic substrate or on a more standard PCB substrate.

II. FABRICATION PROCESS

Three functioning prototype designs are fabricated for comparing the cooling path of GaN transistors. Their cross-section structures are shown in Fig. 2. In the first configuration (prototype I), GaN transistors were flip-chip-mounted on a DBC substrate with an alumina layer of $635 \mu\text{m}$. A special etching technique was used to achieve the high resolution ($200 \mu\text{m}$ pitch) required to mount the transistors. In the second configuration (prototype II), the backside of the transistors was attached to the DBC substrate. This required grinding down the silicon substrate of the transistors, to reduce their thickness and to remove the marking. A Ti/Ag layer was deposited on the silicon substrate, and the dies were attached to the DBC substrate using silver sintering. A flex substrate is used on the topside for the electrical interconnects. The third configuration (prototype III) is the classical flip-chip mounting on PCB, used as a basis for comparison. The three prototypes are shown in Fig. 3.

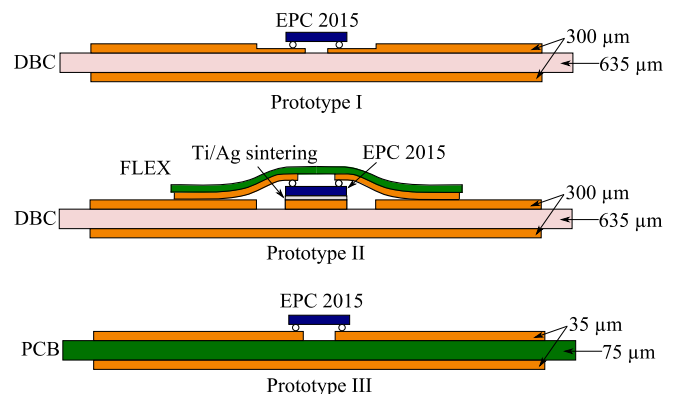


Fig. 2 Cross-section of the three prototypes

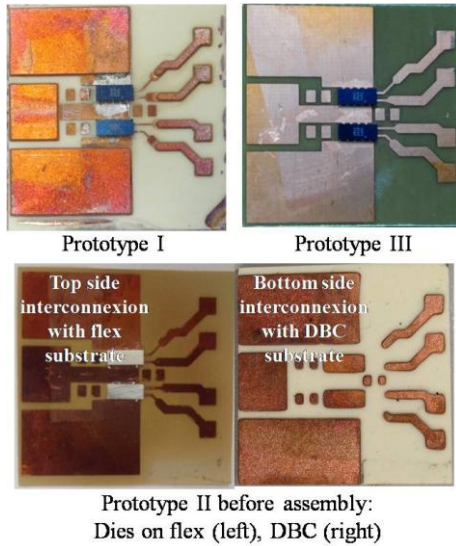


Fig. 3 Photographs of the three prototypes

A. Prototype I

For prototype I, a dual-step etching is used. This allows for using thick copper on most of the surface (for low electric resistance) while having thin copper (high resolution) around the GaN die. In order to realize the double etching, two masks have been designed. The first mask is used for etching the complete electric circuit and the second one addresses only the copper leads for chip soldering. The substrate supplied by Curamik is coated by a photosensitive resin (MC Dip Coating) with a "Dip Coating" machine. After this step, the substrate is exposed to the ultraviolet (UV) through the first mask and developed. The copper etching is performed in ferric chloride, with a spray system (Bernier Electronik PR2030) for 11m30s. This removes approximately 250 μm of the 300 μm thick copper layer. After cleaning, the second etching repeats the same process from coating to etching as the first one but with the second mask and a etching time of 2m30s. The etching result is shown in Fig. 4.

Once the substrates were etched and cleaned, GaN transistors were soldered. The bumps of the EPC's eGaN transistors utilize a Sn/Ag/Cu solder with a composition of 95.5% Sn, 4% Ag, 0.5% Cu (melting point: 217 $^{\circ}\text{C}$). The total reflow process is realized by ZEVAC ONYX 21 can control the process temperature while ensuring proper alignment

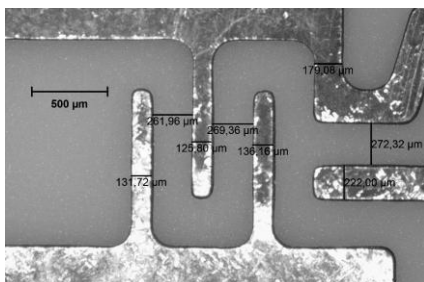


Fig. 4 Etching result with footprint of a EPC2014 die

between dies and substrate. No additional solder is used, the bonding is achieved by the reflow of the solder bumps themselves, as presented in [3]. In order to ensure the adhesion of component and to avoid the local oxidation of the copper, a little of tacky flux has been dropped on the chip contact area just before the component placement. A thermocouple (TC) has been attached near the component to measure the actual device temperature in real time. The solder reflow profile for DBC is shown in the Fig. 5(a). Top Heater and Bottom Heater correspond to the temperature of the heating elements of the soldering equipment (ZEVAC ONYX 21). The TC corresponds to the actual thermocouple measurement on the substrate. Due to its superior thermal performance, the DBC substrate require much more energy to achieve the reflow temperature ($\text{TC} = 250^{\circ}\text{C}$).

B. Prototype II

The realization of prototype II can be divided into two parts, the soldering of the components to the flex substrate and the sintering of the components to the DBC substrate. The first part begins with the grinding down of the silicon substrate of the GaN transistors. This is necessary to remove the marking at the back of the die, and to reduce the thermal resistance of the

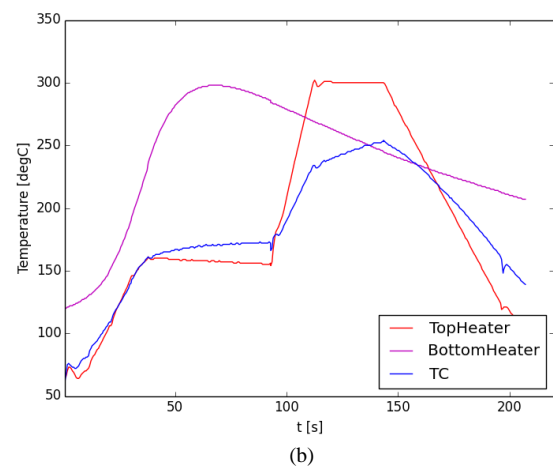
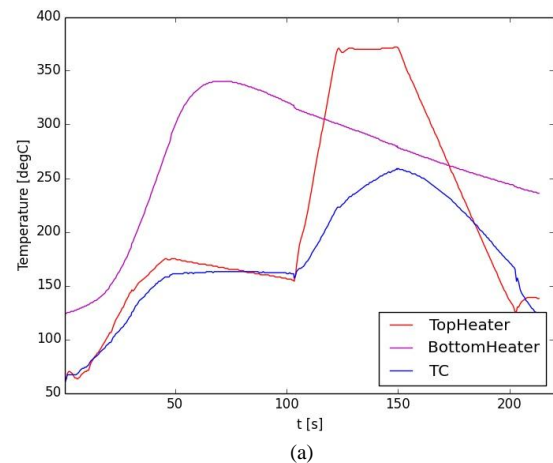


Fig. 5 Solder reflow profile. (a) DBC, (b) PCB

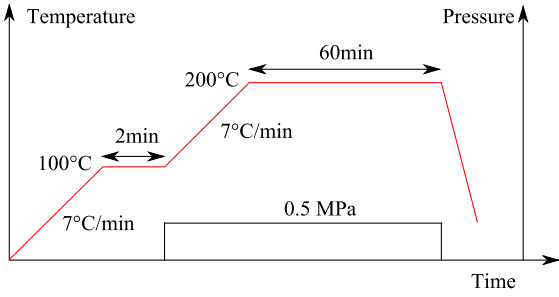


Fig. 6 Sintering temperature profile

device, as we want to mount the backside of the chip to the DBC substrate. The components are first bonded on a sample holder (Struers' AccuStop) by utilizing some mounting wax (Buehler). Then, the holder is put on a polishing machine (MECATECH 334) with a P1200-grade grit paper. The next step is to metalize the backside of the polished part. This is done in an EVA300 PVD system. 50 nm Ti and 150 nm Ag are deposited by evaporation. Afterwards, the chips are soldered to the flex substrate by using the same process described for prototype I.

The second part uses silver sintering technology at low temperature and low pressure. It offers excellent electrical and thermal conductivity so that the reliability is much better than traditional solders. The first step is to apply the selected silver paste (NBE Tech Nanotach-X) on the DBC by screen printing. Then, the soldered GaN transistors and flex substrate are placed onto the paste. Finally, the DBC substrate is subjected to a heated mechanical press, where the silver sinter layer is formed. The temperature profile used in this study is shown in the Fig. 6.

C. Prototype III

The fabrication process of the prototype III is nearly the same as the first one, but without the second etching. The soldering process, as shown in Fig. 5(b), needs a lower temperature for the heaters because of the PCB's lower thermal mass and thermal conductivity.

III. THERMAL ANALYSIS AND CHARACTERISTICS

A. FEM simulation

The power loss will heat up the module and the steady-state junction temperature depends on cooling system. To evaluate the temperature distribution of the prototypes, a 3-D model has been developed. This analysis was conducted using COMSOL finite element method (FEM) tool on the three prototypes. A heat dissipation of 10W was used for one GaN transistor, and an equivalent heat-transfer coefficient of $8 \text{ W}/(\text{m}^2 \cdot \text{K})$ from the surfaces of substrate and component. The bottom surface of the bottom copper layer is assumed as the reference temperature of 27°C . The thermal conductivity of different materials in simulation are shown in Table I. The results of the temperature distribution in the three prototypes obtained by thermal analysis is shown in Fig. 7. Comparing to the PCB, the DBC has much better thermal performance for its lower thermal resistance. Prototype II, where the heat dissipates through

TABLE I. THERMAL CONDUCTIVITY OF DIFFERENT MATERIALS IN SIMULATION

| Material | Thermal conductivity |
|-------------------|----------------------|
| Copper | 400 |
| Ceramic | 27 |
| GaN Bumps | 62 |
| GaN Encapsulation | 130 |
| Prepreg | 0.4 |
| Silver paste | 200 |

encapsulation to DBC, has better thermal management capability than the first prototype where the heat dissipates through bumps because of the lower thermal resistance of the wide area joint.

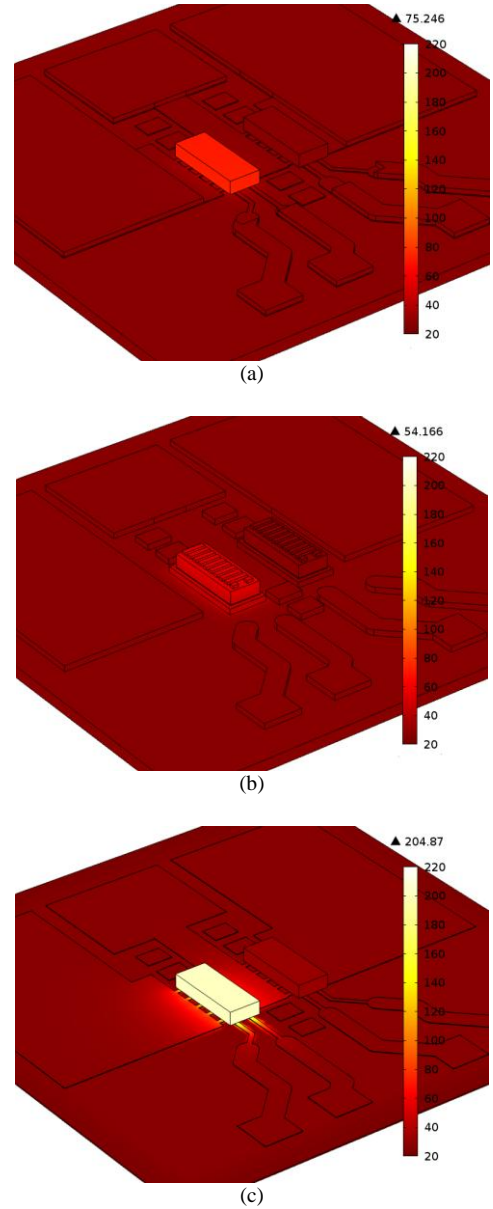


Fig. 7 Temperature distribution by thermal simulation. (a) Prototype I, (b) Prototype II, (c) Prototype III

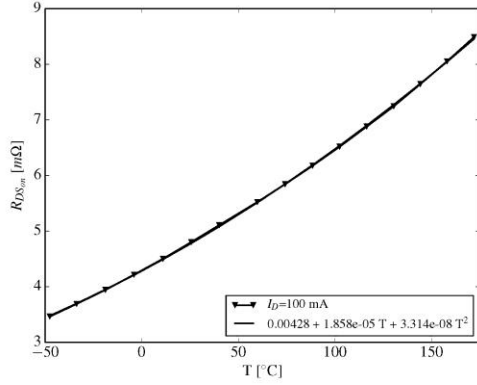


Fig. 8 Calibration Curve (R_{DSon} as a function of T)

B. Experimental characteristics

The junction temperature should be monitored during the device operation. In this study, a thermosensitive electrical parameter is proposed for the measurement of the junction temperature. R_{DSon} is an excellent indicator because it is actually measuring the heat rise in the exact physical location where the heat is being generated. However, the calibration of R_{DSon} as a function of T is a time consuming procedure and requires precise instrumentation techniques.

In order to calibrate R_{DSon} , a thermal conditioner has been used (Thermonics T2500/E). The calibration curve (Fig. 8) is acquired using a Keithley 2410 SMU and shows that R_{DSon} measurement is an accurate way of monitoring the junction temperature of a GaN transistor.

We used the test circuit in Fig. 9: the temperature rise in the Device Under Test (DUT) is estimated by monitoring the drain-to-source resistance (R_{DSon}) of the transistor as a large current (up to 30 A) flows in the component. The resistors in series with the power supply are used for the stabilization of the current before the turn ON of GaN transistor. The voltage between Drain and Source (V_{ds}) is measured by a differential analog input module (NI 9205) and the current I_d is measured by a current probe (Tektronics TC-0030). The prototypes are mounted on a $15 \times 15 \text{ cm}^2$ heatsink, with a sil-pad interface.

The experimental results of the prototype I and III, shown in Fig.10, demonstrates that the temperature of prototype III rises much more than that of prototype I. A static test has also been done to compare the thermal resistance of each prototype. The results are shown in Table II. The experimental results for prototype II are not ideal, the new development is currently in progress concerning the redesign of the flex circuit.

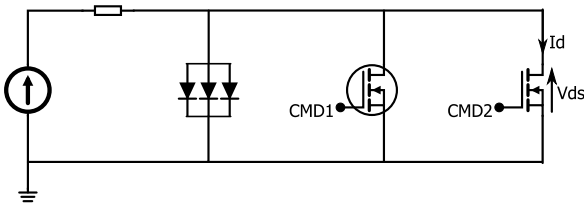


Fig. 9 Circuit diagram used for the transient thermal test

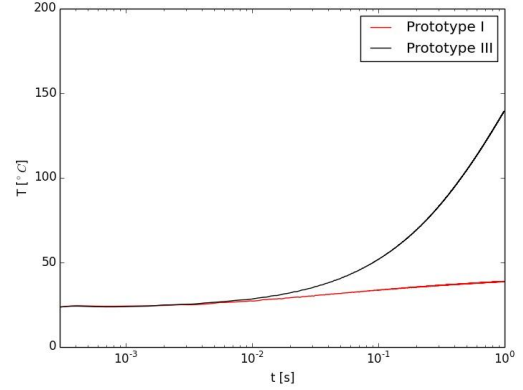


Fig. 10 Temperature as a function of time

TABLE II. STATIC TEST RESULTS

| Prototype | Vds (V) | Id (A) | Rdson (mΩ) | P (W) | Experimental/Simulation Thermal resistance (°C/W) |
|-----------|---------|--------|------------|--------|---|
| I | 0.0926 | 20 | 4.63 | 1.8526 | 4.5/4.8 |
| III | 0.1534 | 20 | 7.67 | 3.068 | 15.6/17.8 |

IV. CONCLUSION

In this paper, the realization of three packaging prototypes for GaN transistors, a flip-chip solution with DBC and PCB substrate and a flex circuit approach is presented. The manufacturing process flow for the three technology developments is given. Thermal analysis and measurements show the feasibility of the approaches. Based on the simulations, thermal dissipation through the topside of the die is expected to have the best thermal performance. Due to the high electrical resistance of the flex interconnects we used, we were not able to measure the thermal resistance of this backside of this configuration.

Regarding the effect of the substrate, it is shown that a ceramic substrate (DBC) makes it possible to reduce the total thermal resistance (from junction to ambient) from 15°C/W down to 4.5°C/W , despite the use of an extremely thin PCB ($145 \mu\text{m}$).

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