

Silver Sintering for Power Electronics Integration

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17/4/15

Introduction

Integration of gate driver circuit

Double-side Cooling

Conclusion

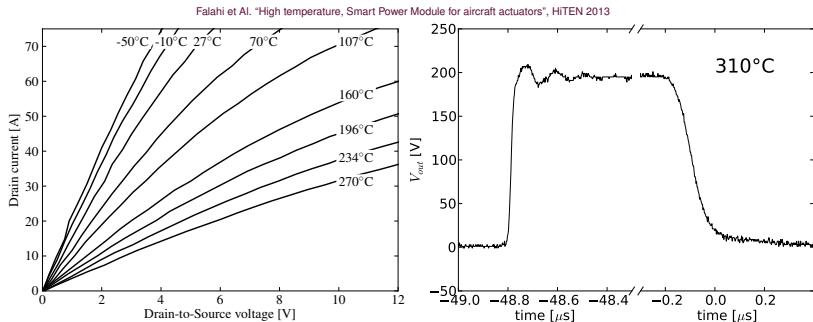
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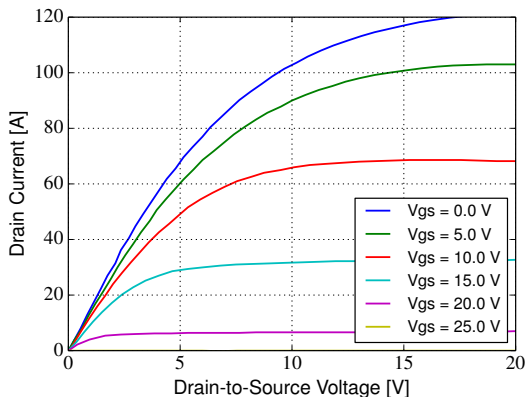
Active Power Devices for High Temperature



Previous results show that SiC JFETs are attractive for
> 200 °C operation:

- ▶ rated at 1200 V (or more), several Amps
- ▶ Voltage-controlled devices
- ▶ No reliability issue related to gate oxide degradation

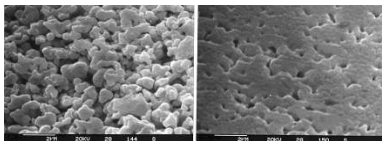
Gate Drivers for SiC JFETs



- ▶ Normally-on devices
- ▶ negative blocking voltage
- ▶ threshold ≈ 20 V.

- ▶ Custom-designed gate driver
- ▶ SOI technology for high temperature capability.

Bonding Material: Silver Sintering



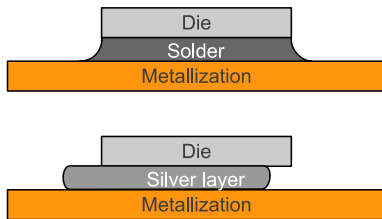
Göbl, C. et al "Low temperature sinter technology Die attachment for automotive power electronic applications" proc of APE, 2006

Silver Paste

- ▶ Based on micro-scale silver particles (Heraeus LTS-11702P2)
- ▶ Low temperature (240 °C) sintering
- ▶ Low pressure (2 MPa) process

No liquid phase involved:

- ▶ No movement of the die
- ▶ No bridging across terminals
- ▶ No height compensation thanks to wetting



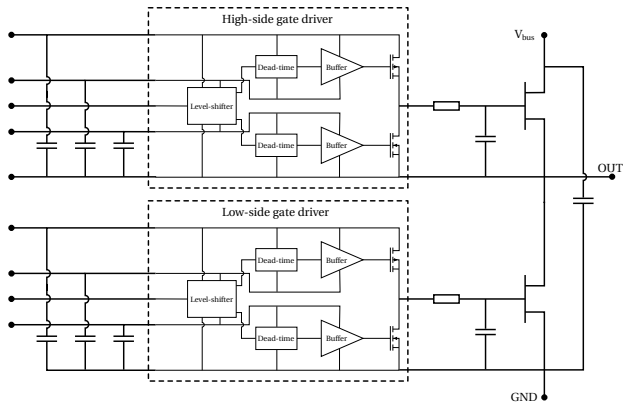
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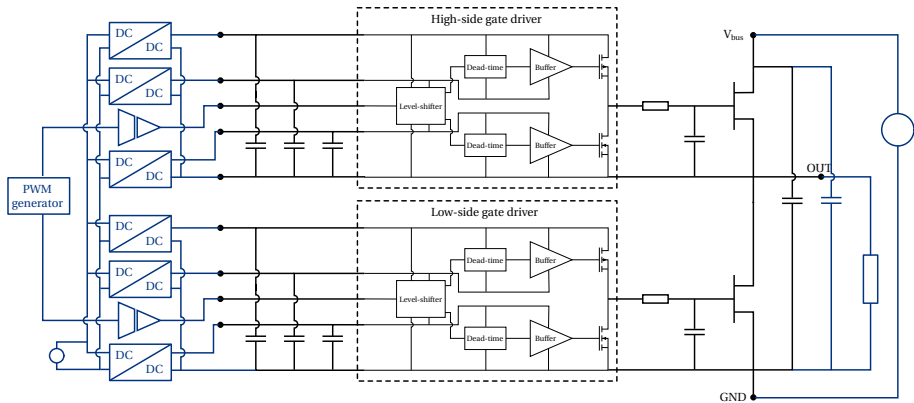
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What's Inside and What's Not?

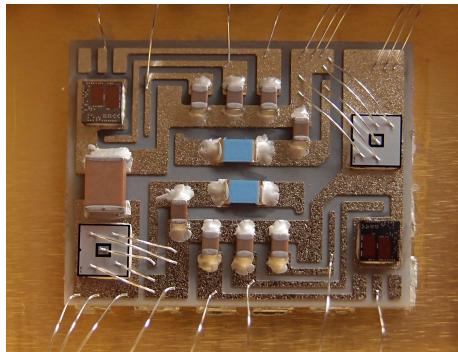
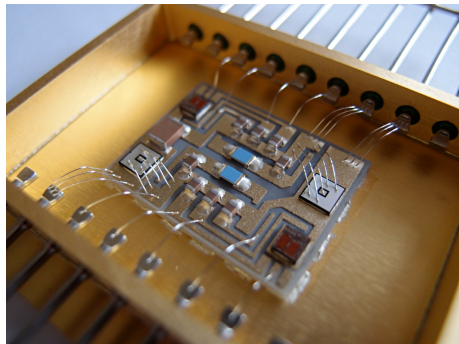


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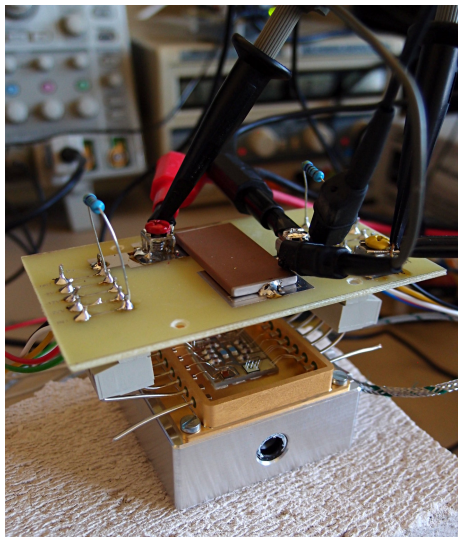
- ▶ Isolation functions (signal and power)
- ▶ PWM signal generation
- ▶ Large value decoupling capacitor ($1 \mu F$)

Pictures of the power module



- ▶ CuMo leadframe / NiFe frame case
- ▶ ceramic substrate (AlN) $\approx 20 \times 30 \text{ mm}^2$
- ▶ high temperature passives (Vishay, Presidio)
- ▶ Al wedge Wirebonds, except Au ball for driver
- ▶ Bonding: silver sintering

The Test Setup



No encapsulation used

→ V_{DC} limited to 200 V

Power module attached to a hotplate

→ test from ambient to 315°C

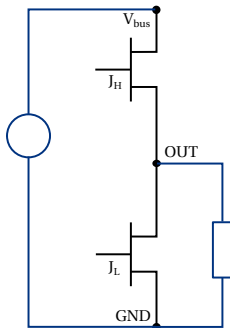
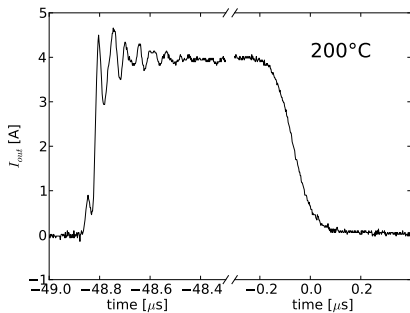
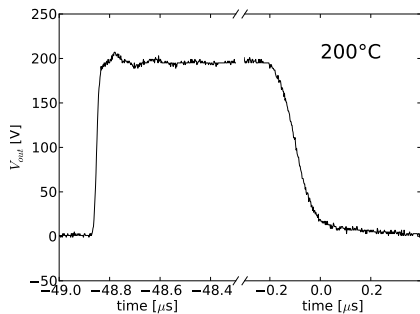
External components at room temp.

→ signal and power isolation

→ large DC capacitor

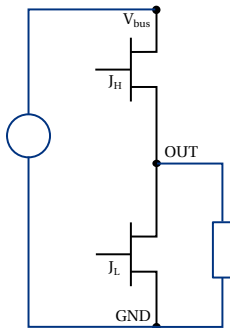
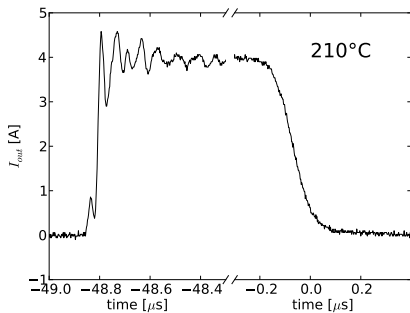
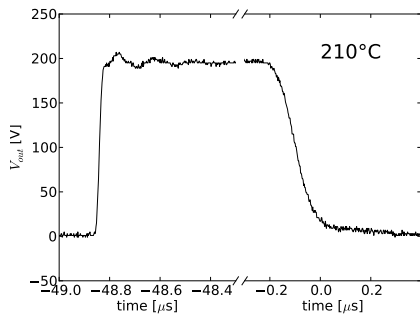
Continuous operation on resistor

Measurements



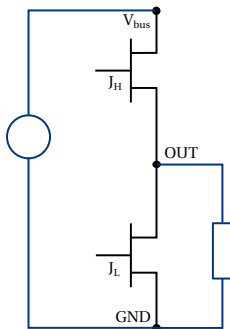
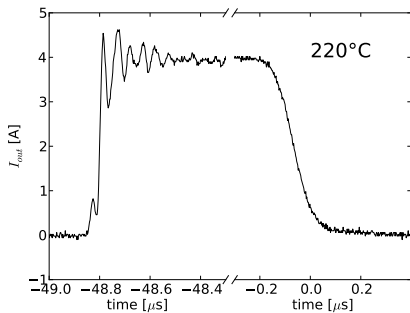
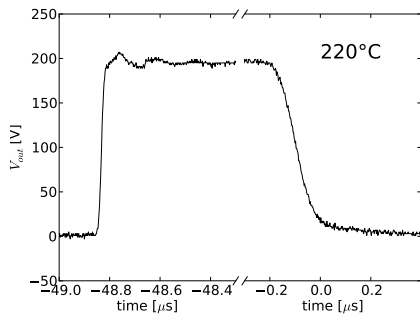
- ▶ $V_{DC} = 200 \text{ V}$ (no encapsulation)
- ▶ $R_{load} = 50 \Omega$
- ▶ $F_{switch} = 10 \text{ kHz}$
- ▶ $t_{dead-time} = 1.2 \mu\text{s}$

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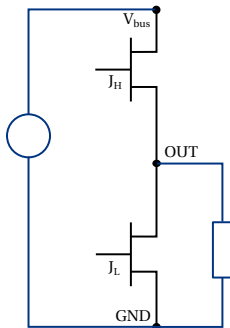
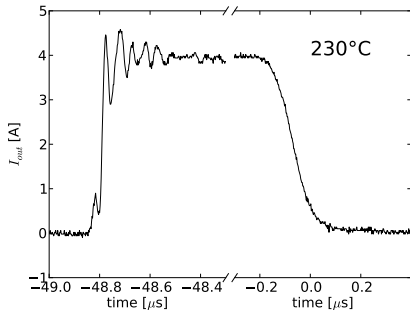
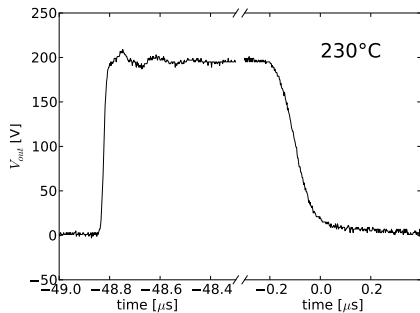
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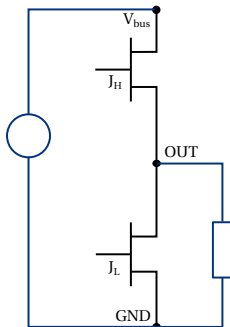
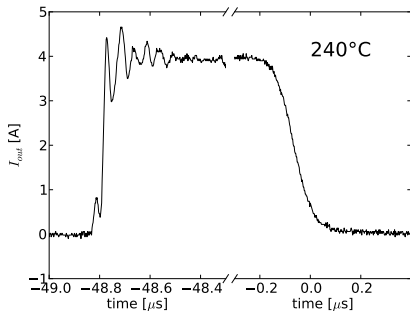
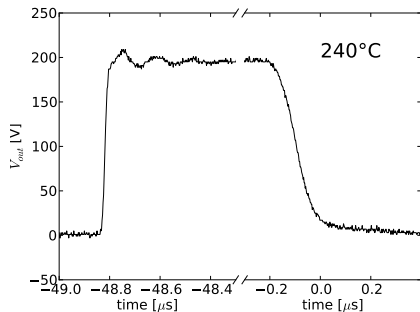
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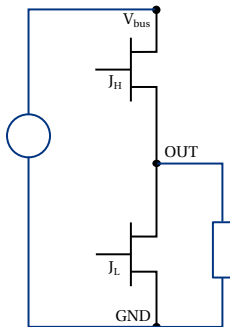
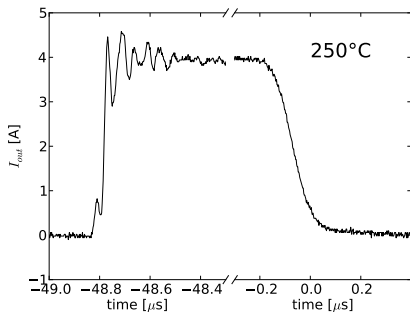
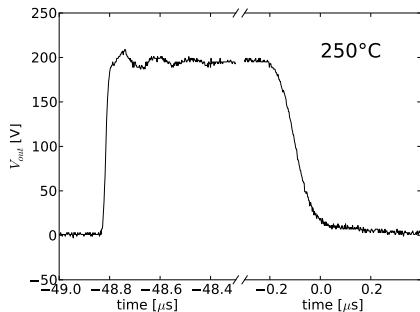
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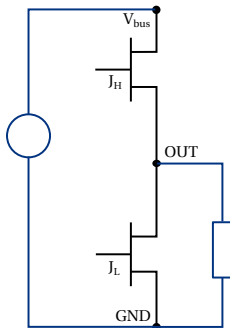
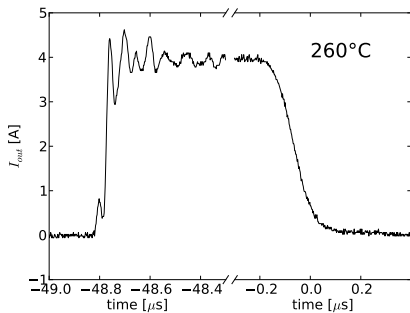
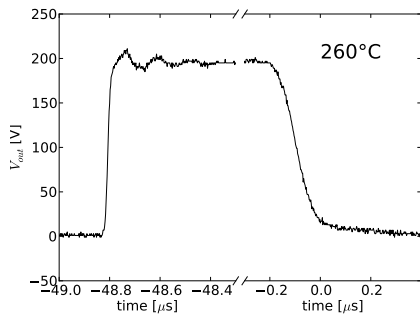
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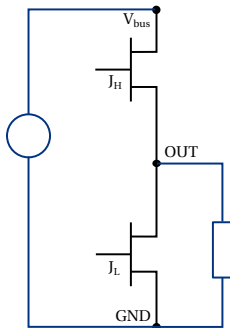
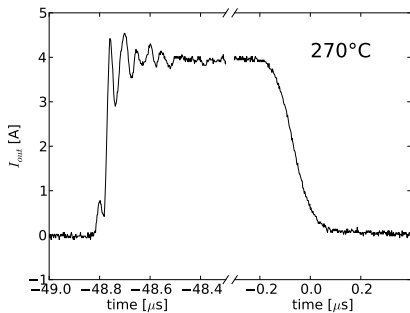
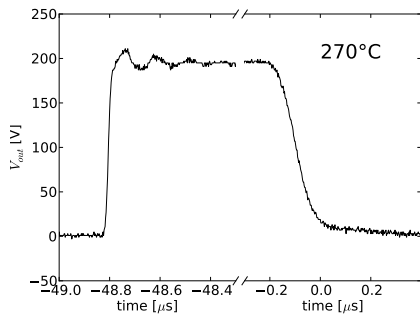
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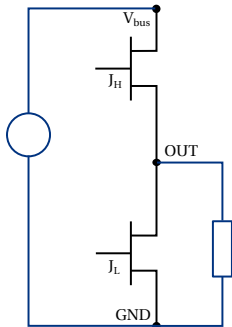
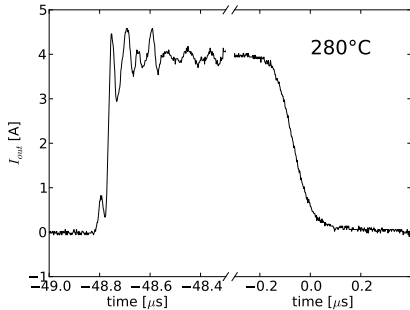
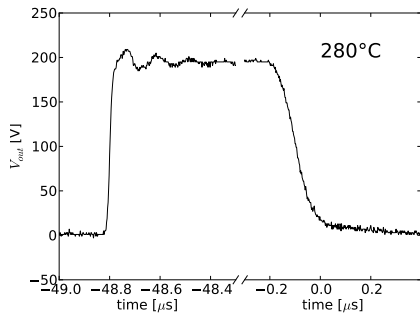
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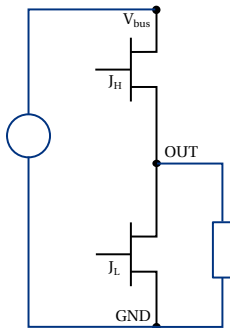
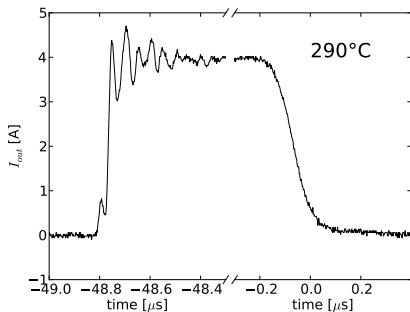
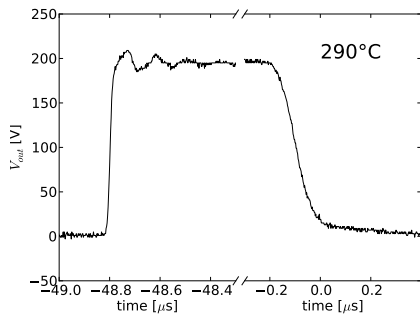
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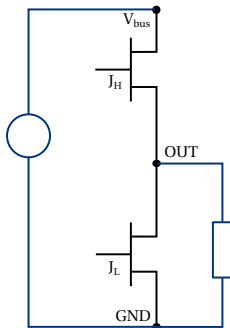
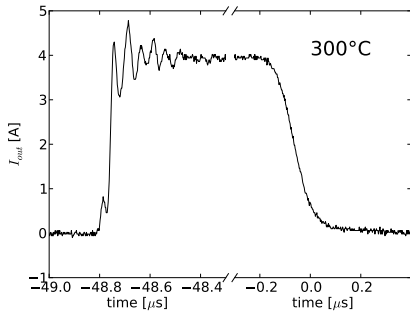
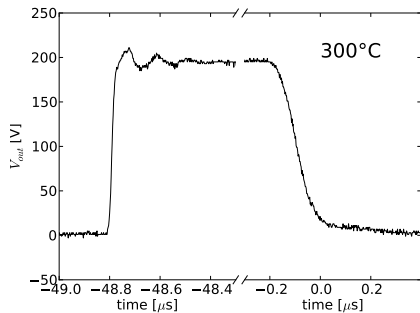
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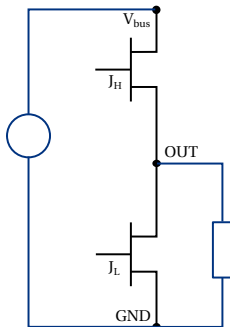
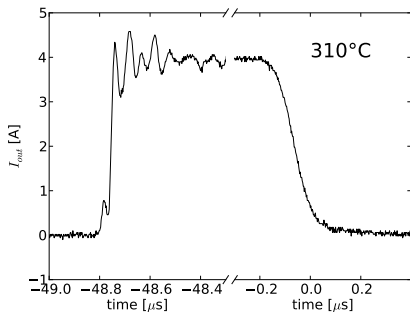
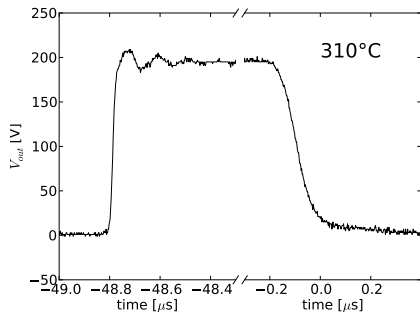
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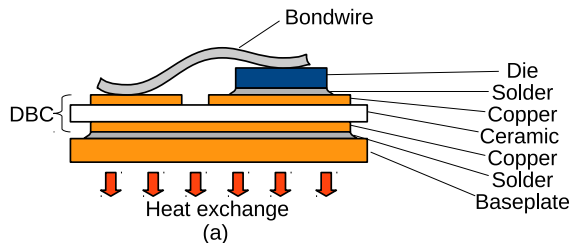
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Double-side Cooling

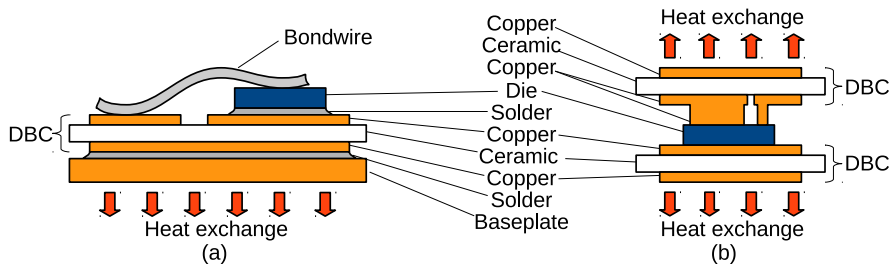
Conclusion

Double Side Cooling



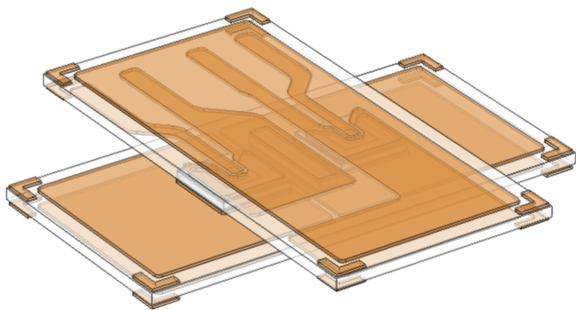
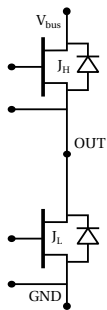
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- ▶ “3-D” or “Sandwich” package performs thermal management on both sides
- ▶ Requires suitable topside metal on the die
- ▶ Requires special features for topside contact

Double Side Cooling



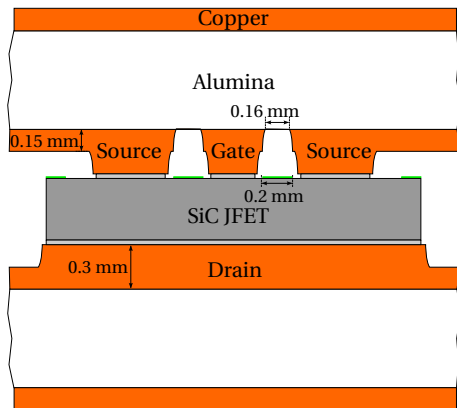
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The proposed 3-D Structure



- ▶ Two ceramic substrates, in "sandwich" configuration
- ▶ Two SiC JFET dies (SiCED)
- ▶ assembled using silver sintering
- ▶ 25.4 mm × 12.7 mm (1 in × 0.5 in)

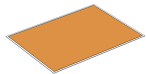
Ceramic Substrates



Scale drawing for $2.4 \times 2.4 \text{ mm}^2$ die

- ▶ Si_3N_4 identified previously for high temperature
- ▶ For development: use of alumina
- ▶ Etching accuracy exceeds standard design rules
- ▶ Double-step copper etching for die contact
- ➔ Custom etching technique

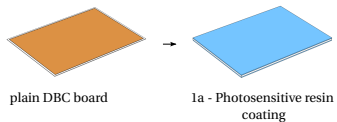
Preparation of the Substrates



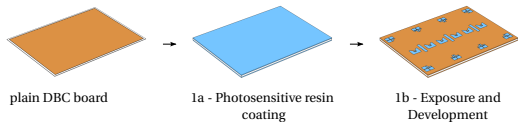
plain DBC board



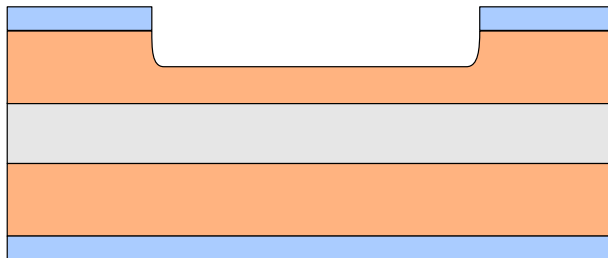
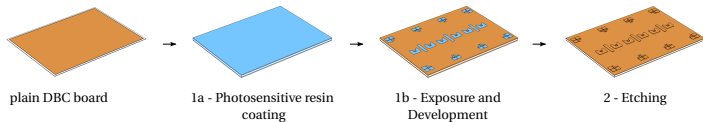
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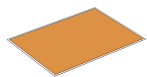
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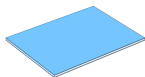
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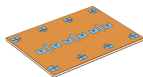
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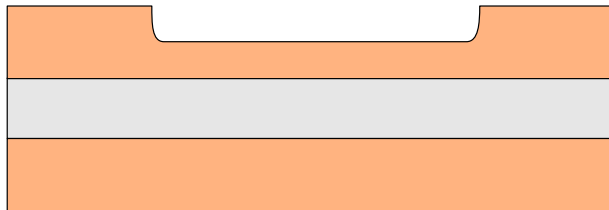
1a - Photosensitive resin coating



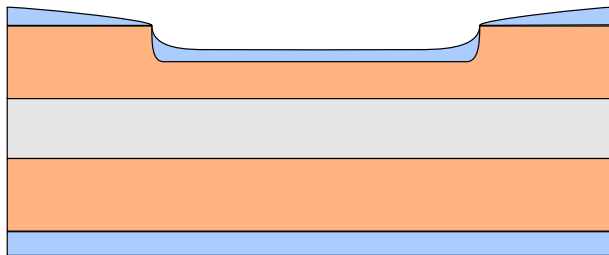
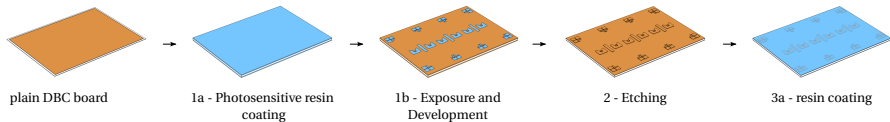
1b - Exposure and Development



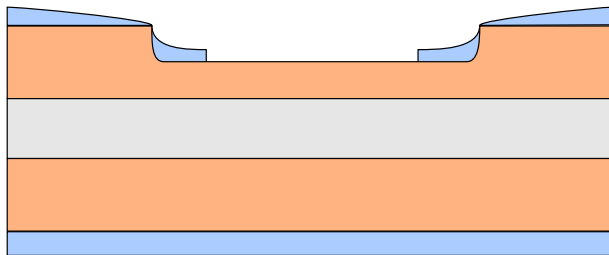
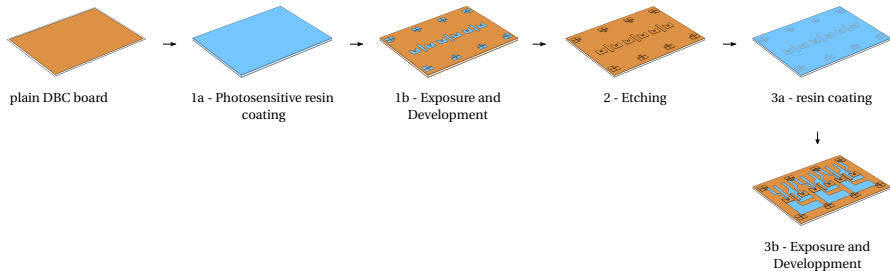
2 - Etching



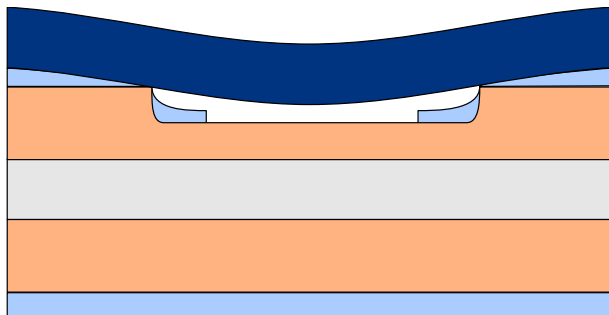
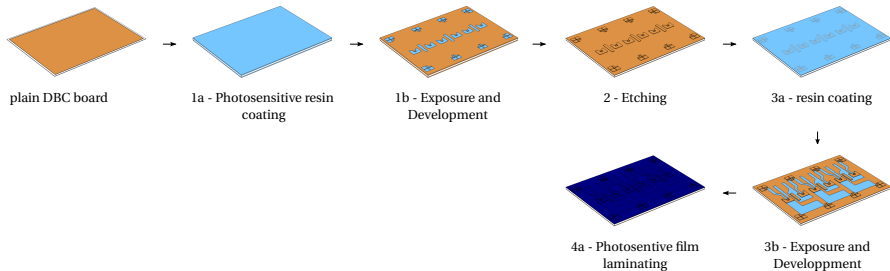
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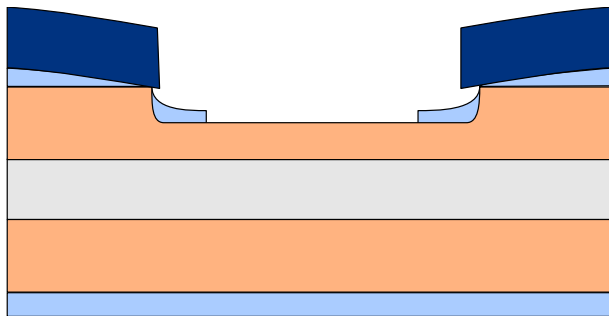
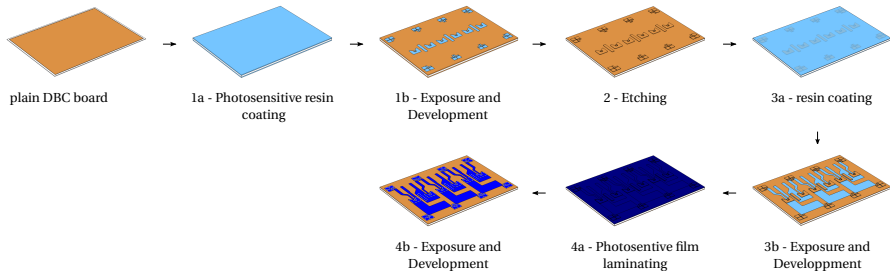
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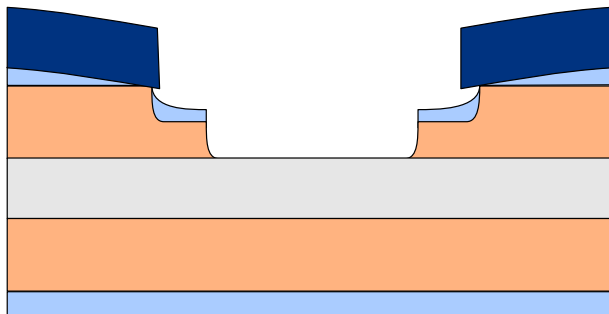
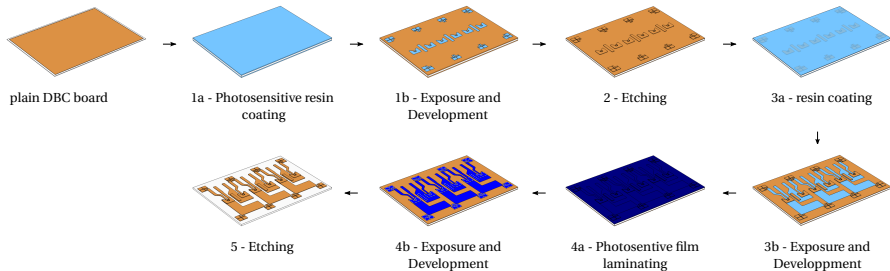
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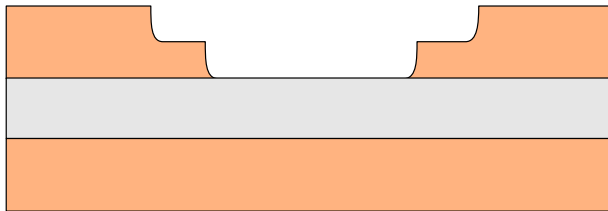
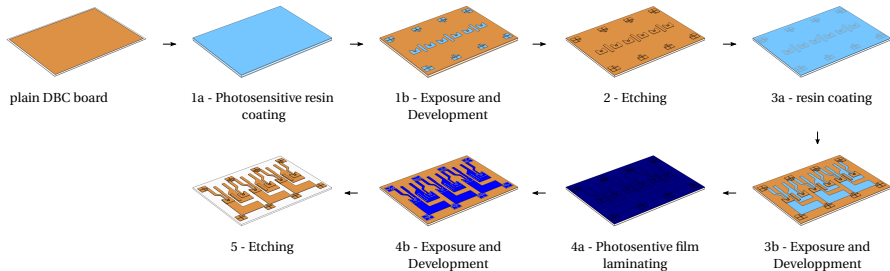
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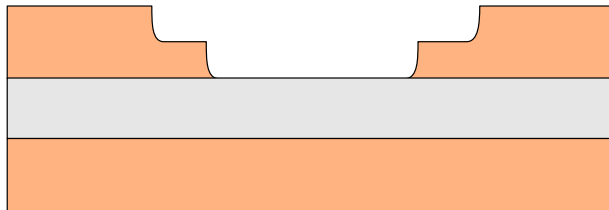
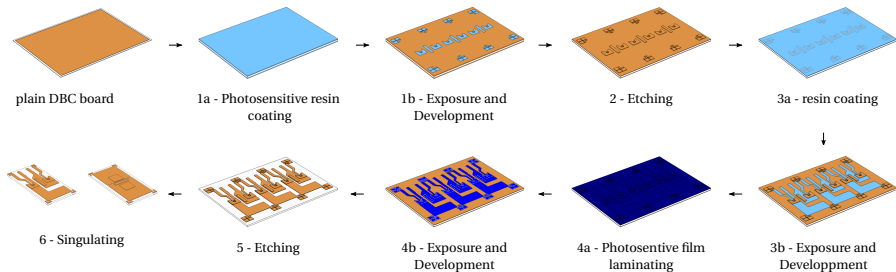
Preparation of the Substrates



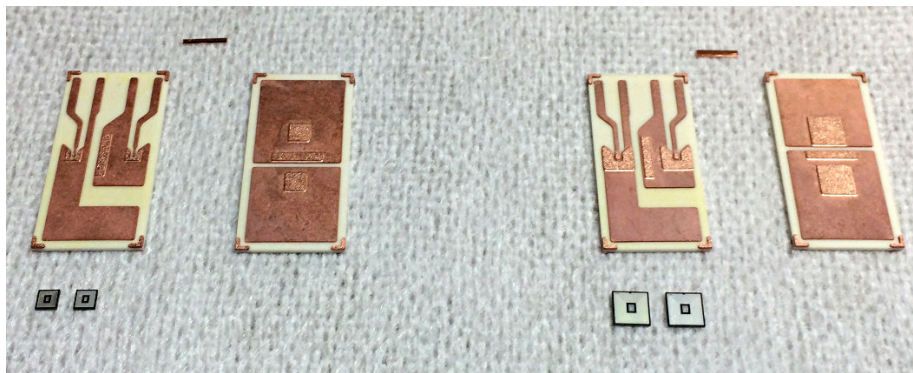
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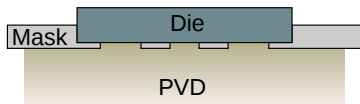
Preparation of the Substrates



- ▶ Final patterns within $50\ \mu\text{m}$ of desired size
- ▶ Two designs, for $2.4 \times 2.4\ \text{mm}^2$ and $4 \times 4\ \text{mm}^2$ dies
- ▶ Total copper thickness $300\ \mu\text{m}$, $\approx 150\ \mu\text{m}$ per step

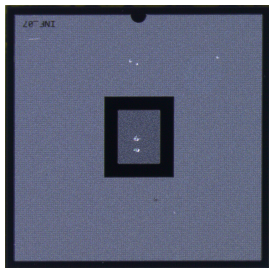
Preparation of the Dies

- ▶ Standard aluminium topside finish not compatible with silver sintering
- ▶ Ti/Ag PVD on contact areas
- ▶ Need for a masking solution
- jig with locating pockets.

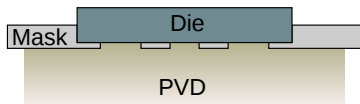


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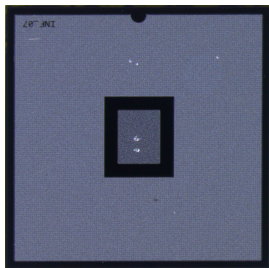
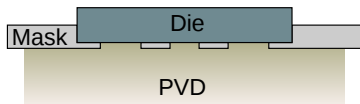


Before PVD

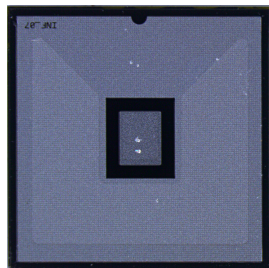


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Before PVD



After Ti/Ag PVD



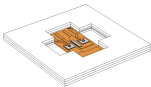
Screen printing

- ▶ Ceramic laser-cut jigs for precise alignment of dies and substrate
- ▶ Two sintering steps using the same temperature profile
- ▶ Sintering under (low) pressure (2 MPa, 240 °C)

Assembly



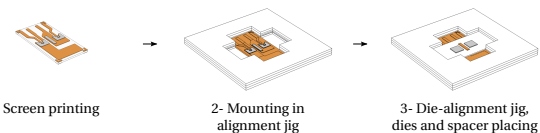
Screen printing



2- Mounting in alignment jig

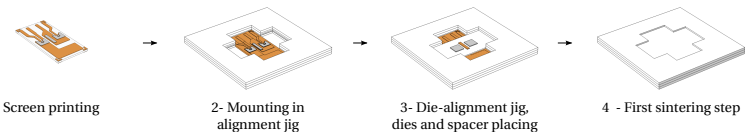
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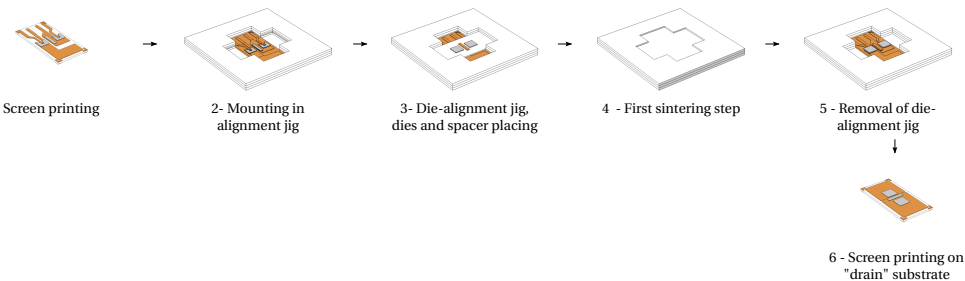
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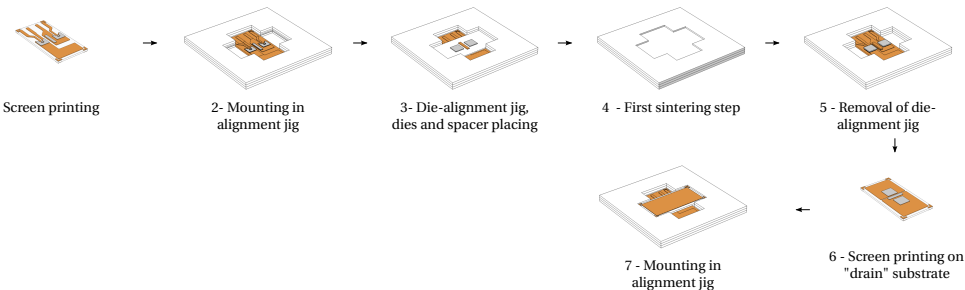
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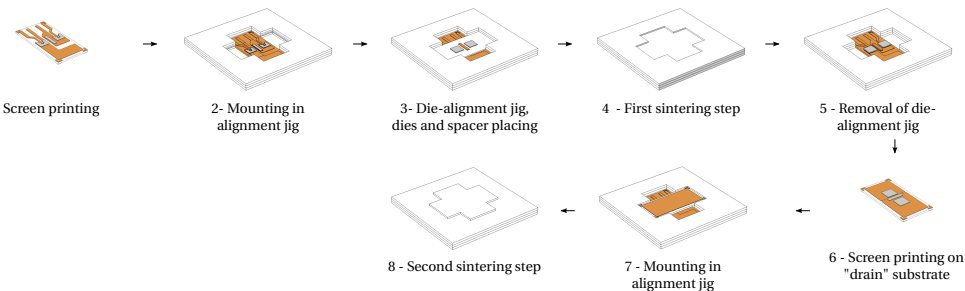
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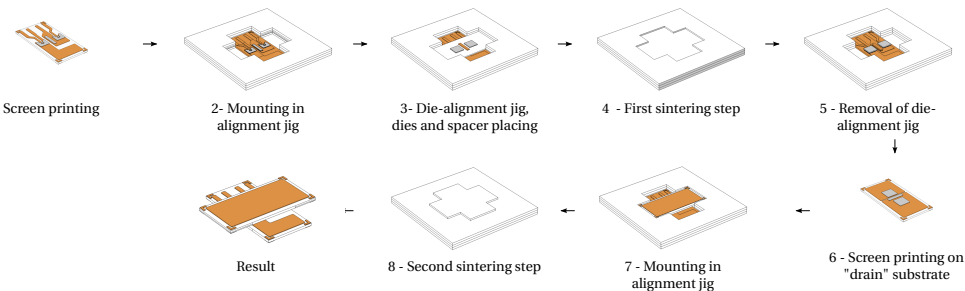
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Sintering process



assembly without drying

- ▶ 30 min Drying step at 85 °C, 30 min sintering at 240 °C.
- ▶ 5 minutes pre-drying before assembly, to increase paste viscosity
 - ▶ use of a glass die to observe paste spreading

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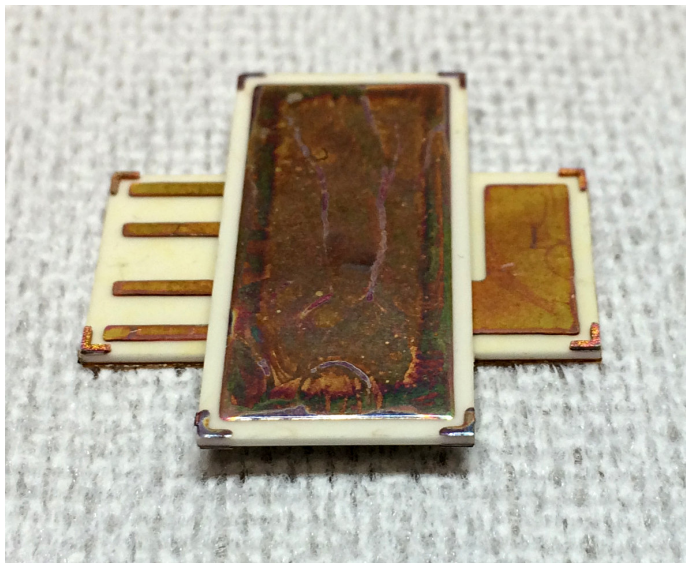
assembly without drying



5 min pre-drying

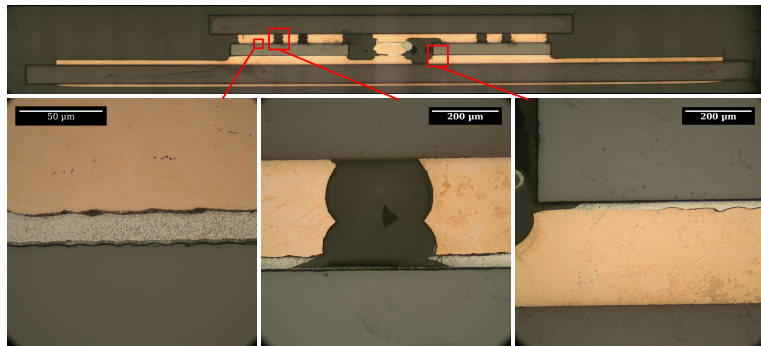
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Prototype



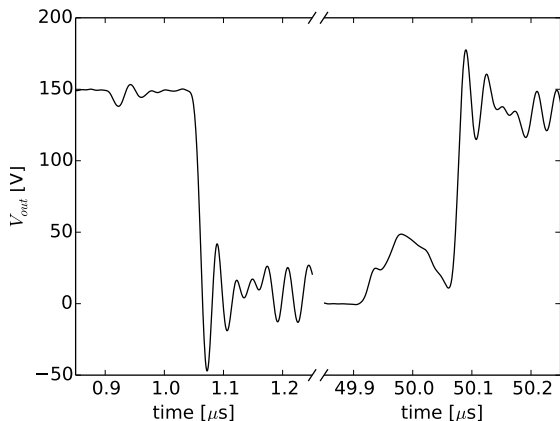
Size: $25 \times 25 \text{ mm}^2$

Prototype – 2



- ▶ Good form factor achieved using the two-step copper etching process
- ▶ Satisfying alignment
- ▶ Poor quality of Al-Cu attach

Switching waveforms



- ▶ Tests performed on the smallest dies ($2.4 \times 2.4 \text{ mm}^2$, $R_{DS_{on}} = 500 \text{ m}\Omega$)
- ▶ 300Ω Resistive load, 0.5 A current (no cooling system used)
- ▶ oscillations dues to external layout (and capacitances of the JFETs)

Introduction

Integration of gate driver circuit

Double-side Cooling

Conclusion

- ▶ Silver sintering useful for a lot more than just die attach
 - ▶ attach of auxiliary devices (gate driver. . .)
 - ▶ dual-side bonding
- ▶ Short-term, high temperature operation demonstrated
- ▶ Long-term operation to be assessed:
 - ▶ risks of silver migration?
 - ▶ thermo-mechanical strength?
 - ▶ what is the most suitable metal finish?

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Thank you for your attention,

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