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Identification of Si film traps in p-channel SOI FinFETs using low temperature noise spectroscopy

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A B S T R A C T

The aim of this study is to analyse the excess low frequency noise from 100 K up to room temperature in p-channel triple-gate standard and strained FinFET transistors fabricated on silicon on insulator (SOI) substrates. The low frequency noise measurements as a function of temperature can be successfully used as a non-destructive device characterisation tool in order to evaluate the quality of the silicon film and to identify traps induced during the device processing. Several identified traps which can be related to boron and carbon, in particular for strained substrate devices, were observed.

Keywords:
SOI
FinFET
Strain engineering
Low temperature
Low frequency noise spectroscopy
Traps in silicon film

1. Introduction

The continuous downscaling of devices requires new materials, structures and design in order to achieve the ITRS [1] specifications. It is already known that the multi-gate FinFETs are considered as strong contenders for the nano MOS device structures, mainly because of the 3D geometry, which through a better electrostatic control of the gate over the conduction channel leads to an improved control of the short-channel effects and provides an enhanced mobility due to the undoped channel. Using strain engineering techniques, an enhancement of the electrical performances of FinFETs can be achieved without adding major process complexity. Concerning the channel architecture, the carrier mobility improvement can be obtained by the use of biaxial strain (sSOI) or of uniaxial strain, implemented by contact etch stop layers (CESL) [2,3]. For the source and drain regions, the implementation of SiGe realized by selective epitaxial growth (SEG) leads to a reduction of the access resistances [4].

The low frequency noise (LFN) analysis has been proposed as a non-destructive diagnostic tool in order to evaluate the quality of the gate oxide interface and of the depleted silicon film [5–9]. The evolution of the low frequency noise with the applied gate voltage at different temperatures was already studied for p-channel standard and strained SOI FinFETs with the aim to investigate the quality of the gate oxide interface through the 1/f noise analysis [10].

The study of the generation–recombination (G–R) noise, corresponding to a Lorentzian type of spectrum, allows to carry out the so-called low frequency noise spectroscopy, when performed as a function of temperature at fixed biasing, and provides information on the nature of traps located in the depletion region of the device [11]. In this work, the study is focused on the G–R contribution in the total low frequency noise versus the temperature in order to investigate the quality of the depleted Si film (fin) of p-channel standard and strained SOI FinFETs.

2. Experimental

The studied devices are p-channel triple-gate FinFETs processed at imec in a 32 nm SOI technology with standard and

strain-engineered channels. The tested devices have five fins in parallel, with a fin width (W_{Fin}) of 25 nm and a fin height (H_{Fin}) of 65 nm and a fixed mask length (L_G) of 1 μm. The gate oxide consists of a high-k dielectric (HfSiON) on top of the 1 nm interfacial SiO_2, resulting in an equivalent oxide thickness (EOT) of 1.5 nm; the metal gate consists of 10 nm TiN covered by 100 nm polysilicon. The devices are on standard SOI substrates (SOI) and on biaxial globally strained silicon films (sSOI); these substrates can be combined with uniaxial local strain (CESL) and/or using SEG in the source and drain regions.

Low frequency noise measurements were performed directly at wafer-level for temperatures from 100 K up to room temperature by a step of 10 K using a 2 in. Lakeshore TTP4 prober. The experimental noise set-up, which allows to bias the devices by choosing the V_{DS} and V_{GS} voltages, consist in an I to V converter, a low noise voltage amplifier and a HP3562A spectral analyser which is used to obtain the noise spectral density from 1 Hz to 100 kHz. The set-up allows to measure the small signal parameters: the total dynamic resistance between drain and source (r_t), defined as $(r_t)^{-1} = \frac{\partial I_D}{\partial V_{DS}}\Big|_{V_{GS}=const.}$ and the transconductance (g_m) over the same frequency range by applying a small signal at the source and gate nodes, respectively. The measurements were performed at fixed $V_{DS} = -20$ mV and V_{GS} was adjusted in order to keep a fixed drain current ($|I_D| = 1$ μA) over the whole temperature range. Noise is calculated at the input of the device by dividing the measured noise voltage by the square of the measured voltage gain between the gate and the output, cancelling the set-up bandwidth limitation.

3. Low frequency noise spectroscopy – identification of traps located in the depletion region

3.1. Theory

The Lorentzian type of spectra associated to generation–recombination phenomena (trapping and detrapping) are related to processes of capture and emission of free carriers by single time constant traps, which can be located at different regions of the transistor structure. For conventional (planar and with one gate) transistors these traps can be situated: in the dielectric layer or at the interface channel/dielectric or in the silicon depletion region. For devices having a gate active area lower than 1 μm^2, random telegraphic signals (RTS), which are commonly attributed to individual carrier trapping at the silicon–oxide interface, can be observed.

For generation–recombination phenomena, the noise spectral density of carrier number fluctuations $\delta S_N(f)$ for a trap of energy E_T, with a trap density N_T in the case of a single time constant τ is described by the formula [8,11]:

$$\delta S_N(f) = N_T(E_T) f_t(E_T)[1 - f_t(E_T)] \frac{4\tau}{1 + (2\pi f \tau)^2}. \quad (1)$$

where $f_t(E_T)$ is the Fermi–Dirac function, and $f_t(E_T)[1 - f_t(E_T)]$ expresses that only the traps close to the Fermi energy level participate to the G–R fluctuations.

Thereafter, we briefly present the noise model of G–R due to traps located in the depletion region of the transistor, which, according to the theory developed in [6] leads to Lorentzians for which the characteristic frequency does not change with the applied gate voltage. In this case, the total spectral density of the carrier number fluctuations is obtained by integration of Eq. (1) over the gate active surface, which is defined by the product of the effective length (L) and the effective width of the inversion channel and can be expressed as [12]:

$$S_N(f) = \frac{\tau N_{eff}}{1 + (2\pi f \tau)^2} WL. \quad (2)$$

where N_{eff} is the effective (surface) density of the traps.

In the ohmic operation regime, the drain current is proportional to the number of carriers; the expression of the gate voltage spectral density is then given by the relation [12]:

$$S_{V_{Glor_i}}(f) = \frac{q^2 W_d N_T \tau_i}{BWLC_{ox}^2} \frac{1}{1 + (2\pi f \tau_i)^2}. \quad (3)$$

For each Lorentzian G–R type contribution to the total noise one can associate a surface (effective) trap density (N_{eff}) or a volume trap density (N_T) and a time constant defined as $1/(2\pi f_{0i})$. The relationship between N_{eff} and N_T is given by: $N_{eff} = BN_T W_d$ where B is a coefficient estimated to be 1/3 [12,13] and $W_d = \sqrt{4\varepsilon_0 \varepsilon_{Si} kT \ln(N_A/n_i)/(q^2 N_A)}$ is the silicon film depletion depth, n_i is the intrinsic carrier density, N_A is the silicon film doping concentration, ε_0 is the permittivity of vacuum and ε_{Si} is the relative silicon permittivity.

Each Lorentzian contribution is characterised by a plateau level A_i, defined as:

$$A_i = \frac{q^2 N_{eff}}{WLC_{ox}^2} \tau_i = \frac{q^2 W_d N_T}{BWLC_{ox}^2} \tau_i \quad (4)$$

Eq. (4) indicates that, for traps located in the depletion region of the transistor, the evolution of the Lorentzian plateau A_i versus τ_i (A_i and τ_i associated to the same trap) should be linear. As the fin width (W_{Fin}) for the studied devices is very small (i.e. 25 nm), the depletion zone of the FinFET transistor can be assumed to be $W_d = W_{Fin}/2$.

The variation of the characteristic time constant τ_i (associated to the same trap) as a function of the temperature allows to plot an Arrhenius diagram; according to [11] one can write:

$$\ln(\tau_i T^2) = \frac{E_T - E_V}{kT} + \ln\left(\frac{h^3}{4k^2 \sigma_p \sqrt{6\pi^3 M_c m_e^{*3/2} m_h^{*1/2}}}\right). \quad (5)$$

where h is the Planck constant; m_e^*, m_h^* are the effective mass of electrons and holes, respectively, and M_c is the number of conduction band energy minima.

From the slope and the y-intercept of the evolution of $\ln(\tau_i T^2)$ versus $1/(kT)$ one can extract the energy difference between the appropriate band energy and the trap energy (i.e. $\Delta E = E_T - E_V$) and the capture cross section σ_p of the trap, respectively.

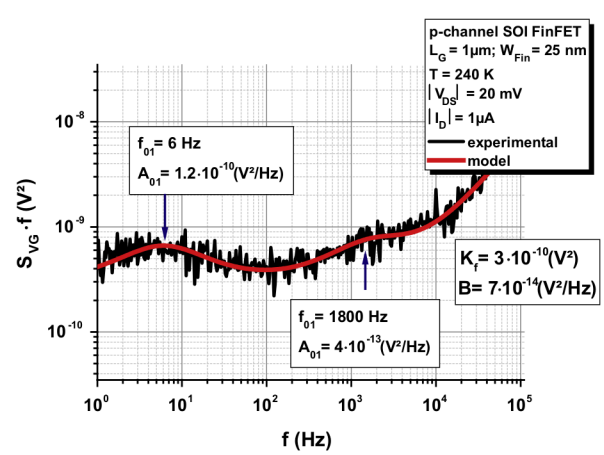

Fig. 1. Typical gate voltage noise spectral density normalized by the frequency. Using the model of Eq. (6), white noise, flicker noise and two Lorentzian contributions are considered to obtain the best fit between the experimental noise and the model.

3.2. Experimental methodology

Fig. 1 illustrates an example of the gate voltage noise spectral density normalized by the frequency for a standard SOI device at 240 K.

Considering white noise, $1/f$ and Lorentzian contributions, the total low frequency noise can be written as:

$$S_{V_G}(f) = B_w + \frac{K_f}{f^{\gamma}} + \sum_{i=0}^{N} \frac{A_i}{1 + \left(\frac{f}{f_{0i}}\right)^2}. \quad (6)$$

where B_w is related to the white noise level, K_f/f^{γ} presents the flicker noise (the frequency exponent γ may deviate from 1 if the gate oxide trap density is not uniform in depth), and the third term of the equation presents a sum of Lorentzian components, with A_i the plateau value and f_{0i} the characteristic frequency. Assuming contributions of these three noise sources, all the observed noise spectra can be perfectly modelled by Eq. (6) as shown in Fig. 1. By using plots in which the frequency normalized noise spectral density versus frequency is represented, one can identify the different noise parameters, in particular the plateau A_i and the characteristic frequency f_{0i} values of the different Lorentzian contributions.

In Fig. 2 are plotted the time constant τ_i estimated from noise measurements performed at room temperature as a function of the applied gate bias. It can be observed that there are three Lorentzian contribution categories: one which is characterised by the fact that the characteristic time constant does not change with applied gate bias; another for which the characteristic time constant decreases with increasing applied gate bias; also some Lorentzian contributions in strong inversion can be correlated with a random telegraph signal (RTS) noise mechanism [14] which is confirmed by the behaviour of the drain current in the time domain.

The traps located at the oxide dielectric/channel are characterised by a continuous distribution of their levels over the energy depth [15]. Then, if the gate bias varies, the Fermi level also varies and it scans traps of different nature. The characteristic time constant of the Lorentzian decreases with the gate voltage increasing. The dependence of τ_i with the applied gate voltage overdrive ($V_{GT} = V_G - V_T$, where V_T is the threshold voltage) is according to the law exp $(-\beta_{GR}V_{GT})$, with a β_{GR} of 29 V^{-1} (Fig. 2). This value is close to the values reported in the literature for G–R noise at the Si/SiO_2 interface (channel/interface layer) [12].

The traps located in the depletion region are traps with discrete and unique deep energy levels. The Fermi level changes with the applied gate bias. Since the energy level of the trap is discrete and unique, the Fermi level scans the same traps (but for increasing depth in the depletion zone). The characteristic time constant of the Lorentzian associated with this trap does not change with gate bias variation [6]. Similar trends were observed for all the investigated devices: the RTS contributions and the G–R noise which can be related with traps located at the gate dielectric/Si interface appear in particular in strong inversion. As the measuring set-up permits a very good control of the drain current, all the noise measurements were performed in moderate inversion at a fixed drain current $|I_D| = 1$ μA.

At different temperatures, noise measurements as a function of the applied gate voltage were performed, as in [10]. This permits to put in evidence, for a fixed temperature operation, Lorentzian contributions which can be assigned to traps located in the depleted fins. In this case the characteristic frequency should vary with temperature [11]. This study considered only Lorentzians which satisfy these two conditions.

Fig. 3 illustrates an example of the frequency normalized noise spectral density versus the temperature, from which variations of the characteristic frequency with the temperature can be observed. For each Lorentzian originating from traps in the depletion region, the characteristic frequency f_{oi} and the plateau value A_i were extracted using the model of Eq. (6).

The physical nature of these traps can be identified by comparing the energy and capture cross section of the traps, which are estimated from the slope and intercept of the Arrhenius diagrams (Eq. (5)), with data in the literature.

One method to estimate the density of traps located in the depletion region is the use of Eq. (4), for each Lorentzian plateau [16]. However, from Eq. (3), one can observe that $S_{V_{Glor_i}}(f,T) \propto \frac{\tau_i(T)}{1+[2\pi f \tau_i(T)]^2}$. For a given frequency f_0, if $2\pi f_0 \tau_i(T) \gg 1$, $S_{V_{Glor_i}}(f_0,T) \propto \tau_i(T)^{-1}$ and $S_{V_{Glor_i}}(f_0,T)$ increases with increasing temperature because τ_i decreases. If $2\pi f_0 \tau_i(T) \ll 1$, then $S_{V_{Glor_i}}(f_0,T) \propto \tau_i(T)$ and $S_{V_{Glor_i}}(f_0,T)$ decreases with increasing temperature. This means that the measured $S_{V_{Glor_i}}(f_0,T)$ dependence with temperature passes through a maximum. The density of the

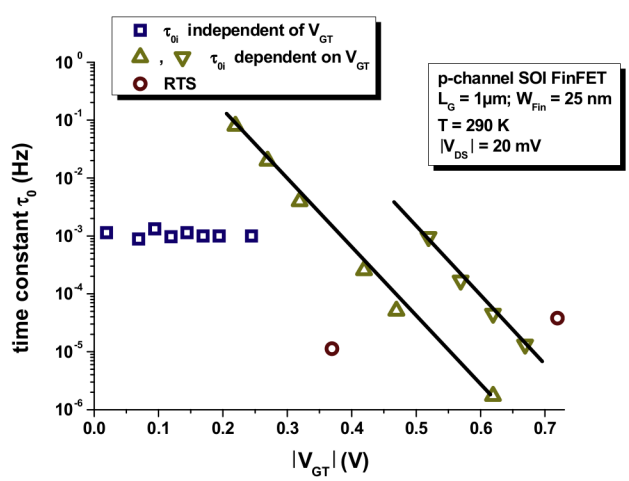

Fig. 2. Characteristic time constant evolution with the applied gate voltage overdrive for a standard device at 290 K. A time constant independent of the gate voltage overdrive is correlated to traps located in the Si film; a time constant depending exponentially on the gate voltage overdrive (with an exponential coefficient of about 29 V^{-1}) is correlated to traps located at the gate dielectric/Si film interface; two RTS contributions are confirmed by the evolution of the drain current in the time domain representation. For a gate bias close to the threshold voltage (close to the $|I_D| = 1$ μA) only time constants related to traps located in the Si film are observed.

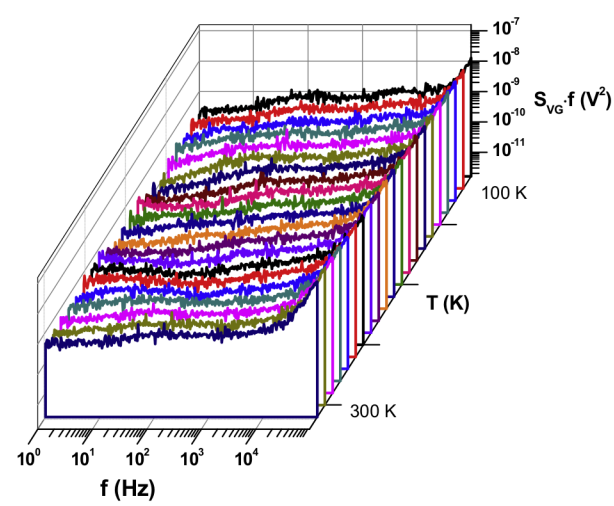

Fig. 3. Typical frequency normalized gate voltage noise spectral density evolution with the temperature, from 100 K up to room temperature, using a step of 10 K, for a constant applied bias of $|I_D| = 1$ μA, in the case of a SOI structure with a gate length of 1 μm.

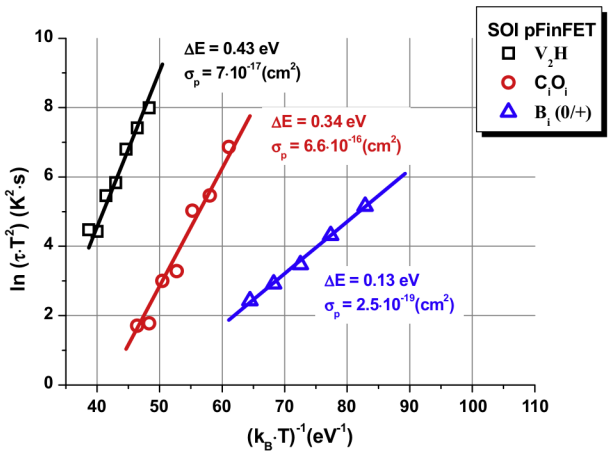

Fig. 4. Example of an Arrhenius plot for a standard SOI pFinFET. Three traps located in the Si film are identified.

traps (which includes $B = 1/3$) can then be estimated as in the following expression [12,17]:

$$N_T = \frac{12\pi\left[S_{V_{Glor_i}}(f_0,T)\right]_{\max} f_0 C_{ox}^2 WL}{q^2 W_d} \tag{7}$$

4. Results and discussion

A typical Arrhenius diagram for a standard SOI device is plotted in Fig. 4. Three traps can be clearly identified: – one which is activated from 250 K up to 290 K and can be related to hydrogen (V_2H) [18]; the second one which is activated from 200 K up to 250 K and is related to the interstitial carbon – interstitial oxygen complex (C_iO_i) [19,20], and the last one which is activated from 140 K up to 180 K and could be related to interstitial boron (B_i) [20,21].

Fig. 5(a–c) shows examples of the Arrhenius diagram and of the identified traps for standard and strained devices.

The traps related to hydrogen may be present due to hydrogen residues after annealing. Diffusion from the highly boron doped source and drain regions may explain the presence of an important number of identified traps related to boron. A contamination due to the SiC liner deposition step can explain the important number of traps related to carbon. The presence of the divacancies (V–P) could be caused by the evolution to a stable state of the unstable defects like Frenkel pairs, which could be generated during the implantation. The nature of one trap was not identified in the case of a strained device (sSOI + SEG + CESL). However, it may be related to the dry-etching or the implantation damage processes.

Using the methodology of Eq. (7), the associated volume trap densities N_T can be estimated from the evolution of $S_{V_{Glor_i}}(f_0,T)$ with the temperature at fixed frequency. As expected, a bell-shaped behaviour can be observed in Fig. 6, showing the evolution of $S_{V_{Glor_i}}(f_0,T)\cdot f_0$ associated to the hydrogen trap, for a fixed frequency f_0 of 30 Hz. The evolution of the characteristic frequencies in the temperature range where this trap is active is shown in the second Oy axis of Fig. 6. It can be easily observed that this fixed frequency allows to obtain the factors f_0/f_{0_1} and f_{0_2}/f_0 which have values (in our case, 5 and 5.3) close to each other; and this guaranties maximum limits of $2\pi f_0\tau_1(T_1) \ll 1$ and $2\pi f_0\tau_2(T_2) \gg 1$, where $T_1 - T_2$ is the temperature interval where this trap is active ($T_2 = 250$ K and $T_1 = 290$ K). From the maximum of the $S_{V_{Glor_i}}(f_0,T)\cdot f_0$ evolution with temperature (at fixed f_0 of 30 Hz) a trap density N_{T1} of $3.7\cdot 10^{16}$ cm^{-3} is obtained.

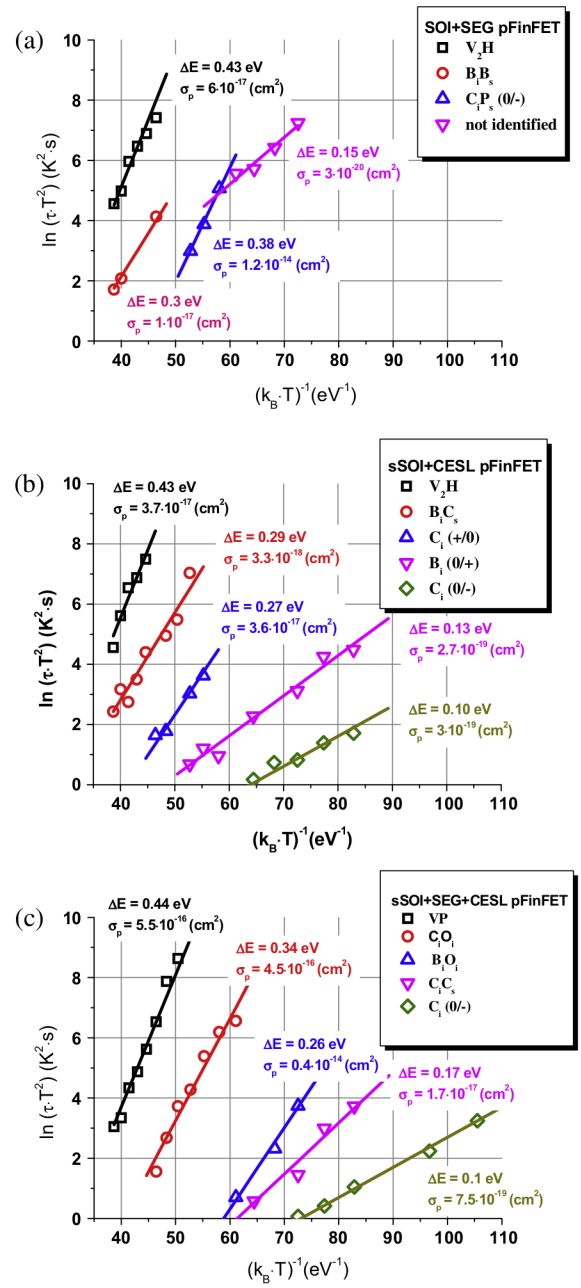

Fig. 5. Example of Arrhenius plots for all p-channel structures (a) SOI + SEG; (b) sSOI + CESL and (c) sSOI + SEG + CESL.

However, as pointed out by Eq. (4), the evolution of the Lorentzian plateau A_i versus τ_i (A_i and τ_i associated to the same trap) should be linear. This was verified for all studied devices. A value of $5.4\cdot 10^{-9}$ (V^2) for the slope of A_i versus τ_i (which is associated to the V_2H identified traps in a standard device (SOI)) is obtained, as shown in Fig. 7. The value of the effective trap density is $N_{eff} = 8.6\cdot 10^{11}$ cm^{-2}. By using the relationship between the effective trap density and the volume trap density (i.e. $N_T = (N_{eff}B)/W_d$ from Eq. (4), with $W_d = W_{Fin}/2$), finally, the volume N_{T2} traps density can be estimated at $2.3\cdot 10^{17}$ cm^{-3}. By comparison between these two methods to determine the volume trap densities N_T, the value of B is estimated at 0.05. For all investigated devices and identified traps, using the same procedure, the obtained values of B coefficient are in the range of 0.04 up to 0.17. This variation could be related to the fact that on the one hand, the estimation of the trap density using the method

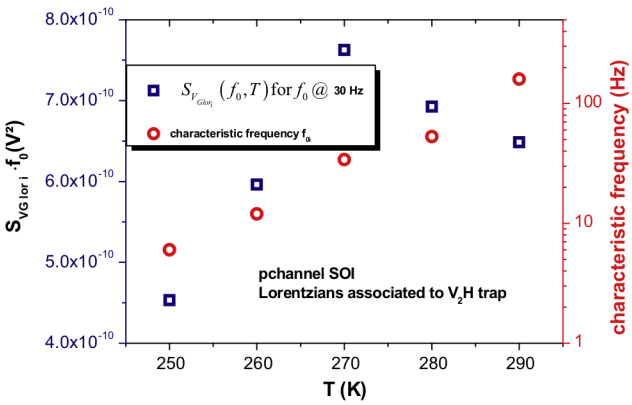

Fig. 6. Temperature evolution of the parameters related to V_2H traps identified in SOI structure: on the Oy1 axis: $S_{V_{Glor_i}}(f_0,T)\cdot f_0$ for a fixed frequency f_0 of 30 Hz; on the Oy2 axis: characteristic frequency f_{0_i} of Lorentzians.

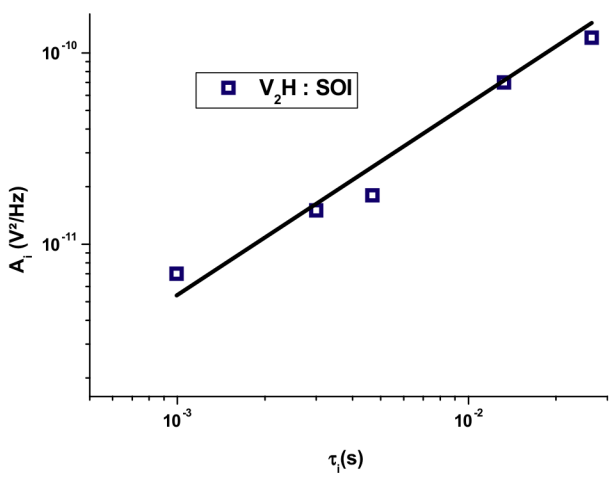

Fig. 7. Example of the linear evolution of the Lorentzian plateau A_i versus the time constant τ associated to the same trap.

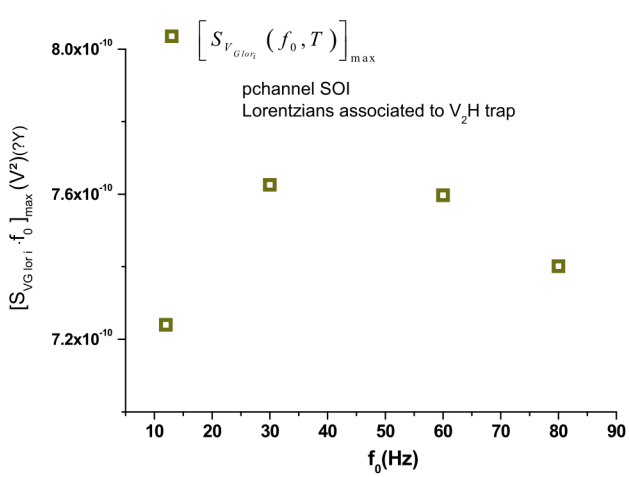

Fig. 8. $[S_{V_{Glor_i}}(f_0,T)]_{max}$ for different fixed frequencies f_0, the error is minimal when a f_0 is chosen for which both conditions $2\pi f_0\tau_1(T_1)\ll 1$ and $2\pi f_0\tau_2(T_2)\gg 1$ are respected.

described by Eq. (5) is sensitive to the value of the fixed frequency f_0 for which the evolution of $S_{V_{Glor_i}}(f_0,T)$ for different fixed frequencies f_0 is plotted as shown in Fig. 8. The error is minimal when a f_0

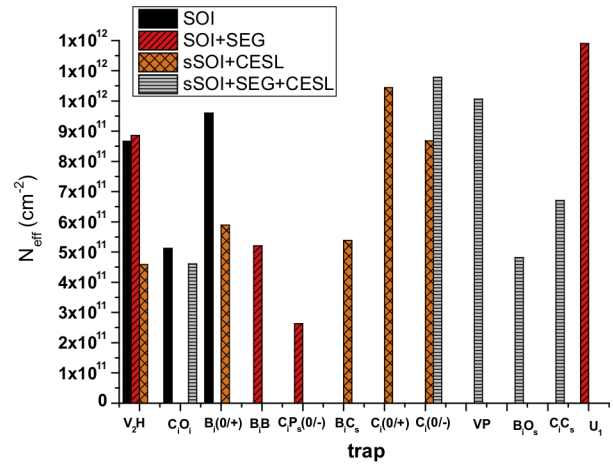

Fig. 9. Effective trap densities extracted from the slope of the Lorentzian plateau A_i versus τ_i (A_i and τ_i associated to the same trap).

is chosen for which both conditions $2\pi f_0\tau_1(T_1)\ll 1$ and $2\pi f_0\tau_2(T_2)\gg 1$ are respected, as observed in Fig. 8. On the other hand, the measurement relative error (less than 5%) and the estimation of the plateau and characteristic frequency of the Lorentzian contributions (which is less than maximum 10% when 4 Lorentzian contributions on 5 frequency decades of noise spectra are observed [22]) could have an impact on the calculation of the B coefficient.

The difference between the predicted value of $B = 1/3$ [12,13] and the experimental value (less than 1/3) could be related to the fact that the theoretical B coefficient was determined for conventional planar devices with one gate, and the investigated devices are multiple-gate 3D devices. For these reasons, even if the traps in the Si film are related to a volume phenomenon, we determined the surface (effective) density of the identified traps, for which no assumptions on the value of the B coefficient and on the value of the depletion zone of the Si film are necessary.

The extracted effective trap densities for each identified trap are summarized in Fig. 9. The number of the identified traps is important: this could be related to the relatively low value of the pure $1/f$ noise and also to the advanced technology used to process the devices. The use of the additional process steps (sSOI, CESL, SEG) in order to boost the device performances leads to an increase of the number and of the maximum of the effective trap density of the traps located in the Si film. However, the estimated effective densities of the identified traps have the same order of magnitude as those identified in n-channels FinFET [23].

5. Conclusions

The analysis of the temperature evolution of the Lorentzian time constant allowed to identify traps in the silicon film. Three traps were identified for devices processed on a standard SOI substrate. Using strain or SEG leads to an increase in the number of identified traps for a given technology. The nature of the identified traps suggests that the implantation and the SiC liner process are mainly responsible for all the observed traps. The nature of one trap was not identified. However, it can originate from the dry-etching or the implantation damage.

The experimental value of the correction factor B for multiple – gate 3D devices is lower than the theoretically predicted one for conventional planar transistors with one gate. In order to avoid making an assumption of the B value, for 3D multiple-gate the effective trap densities can be estimated directly from the plateau

versus the characteristic frequency of the Lorentzian contribution associated with the same traps. As expected, it was observed that the effective trap density seems to be sensitive to additional process steps employed to increase the device performances.

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