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# Review of high frequency, highly integrated inductive DC-DC converters

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## Summary / Abstract

This paper will review the state-of-the-art of high-frequency, highly integrated, inductive, low power DC-DC converters. This study aims to bring out the actual trade-offs between efficiency, level of integration, conversion ratio, technology ... The analysis will focus on the electrical and the physical/technological aspects of DC-DC converters. The context of this study is the design and manufacturing of a high frequency (200 MHz), highly integrated DC-DC converter, based on the ultimate association in 3D of an active die to an interposer of passive devices.

## 1 Introduction

DC-DC converters are widely used in portable electronic devices. The need for integration of these converters comes from their actual significant area impact on the PCB of embedded devices. As the main area of a standard DC-DC converter is occupied by passive elements (inductors and capacitors), one way to reduce their footprints is to increase the switching frequency, leading to reducing the required values. Increasing the frequency will have a negative impact on switching losses.

The state-of-the-art has been build upon 22 of the most significant papers presenting physical implementations and chip measurement of inductive converters. Capacitive converters are omitted because of their actual power density, incompatible for output power of 500 mW in few square millimeters. No references could be included for the sake of place.

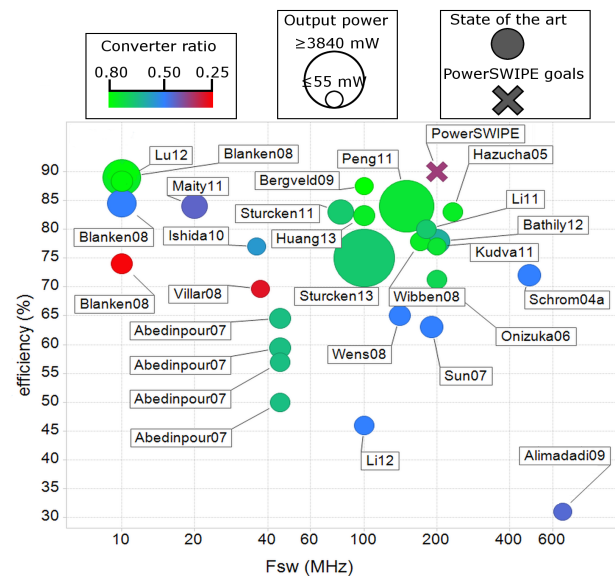
## 2 State of the art

### 2.1 Electrical analysis of DC-DC converters

Populated space is represented in **Figure 1**. All values are extracted from papers by taking the electrical values when the efficiency is explicitly given by the author – in some papers, 2 or more points are reported. In this plot, the X-axis is the switching frequency (logarithmic scale) of the converter and the Y-axis is the efficiency. The color of the dots represents the converter ratio (output voltage divided by input voltage). The diameter of the dots is proportional to the output power of the converter. The cross represents the target of a recently started design project. Many comments can be drawn from this landscape to highlight the challenges and trade-offs for higher switching frequency.

- When the frequency is kept constant, the efficiency decreases if the converter ratio decreases [Blanken08].
- For all converters listed, frequency is above 10 MHz, and efficiency is below 90 %.
- At really high frequencies (greater than 200 MHz), the efficiency drops drastically.
- Only few converters present a low conversion ratio: in most converters, output voltage is close to the input voltage.

- The vast majority of converters have an output power of approximately 500 mW.



**Figure 1** Electrical landscape of high frequency inductive DC-DC converter

State-of-the-art addresses a reasonable range of switching frequencies. The factors that impact mostly the efficiency are the frequency – as predicted by analytical models – and the conversion ratio.

More comments and conclusions will be given in final paper based on other landscape views.

Missing elements in this landscape are mainly converters with a lower conversion ratio.

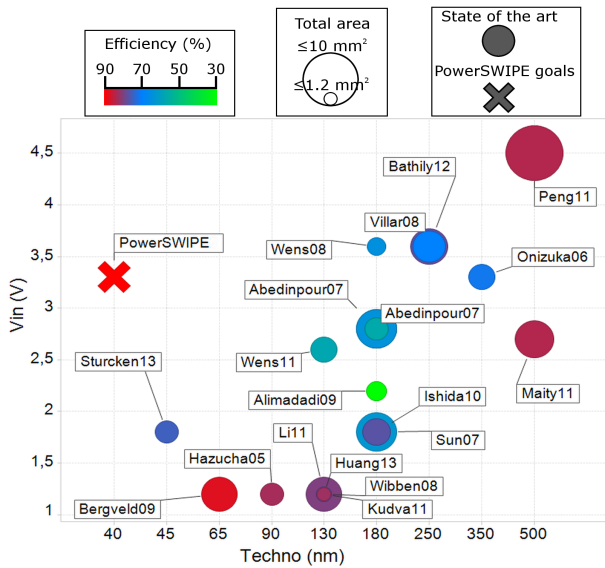
There is also no converter reaching 90 % efficiency. Some are quite close, but 90 % seems to be a difficult target to reach.

### 2.2 Physical and technological analysis of DC-DC converters

**Figure 2** is a representation of the DC-DC converters using some physical and technological parameters, combined with input voltage and efficiency.

The X-axis is the technology node (categorical scale). The Y-axis is the input voltage of the converter. The color of the dot represents the efficiency, and the size of the dot is

proportional to the total converter area. The cross represents the target of a recently started design project. Note that [Peng11] uses GaAs, while all others use standard CMOS.



**Figure 2** Physical and technological landscape of DC-DC converter

The analysis of **Figure 2** shows:

- Smallest technology used for DC-DC converter manufacturing is 45 nm.
- Maximum input voltage is 4.5 V.
- At constant input voltage, scaling down technology seems to increase efficiency (at 1.2 V input, from 130 nm to 65 nm).
- Converters with smaller technology also have smaller input voltage.
- At 130 nm and below, most of the converters have an input voltage close to the nominal technology voltage (1.2 V).
- When scaling down technology, there is no impact on total size of the converter.

State-of-the-art shows that scaling down technology and/or reducing input voltage have a positive impact on efficiency. Area is not dependent on these parameters. It is mainly impacted by output power and switching frequency (passive sizes).

More comments and conclusions will be given in final paper based on other landscape views.

There is no converter handling a high input voltage at a small technology node. Technology nodes under 45 nm are unexplored. And high efficiency converters with high input voltage are still missing.

### 3 Overcoming roadblocks

The design goal is a DC/DC non-isolated converter 3.3 V to 1.2 V (ratio is 0.36), exploring the 200 MHz switching frequency. The output power of the converter will be around 500 mW. The efficiency target is 90 %.

The converter will be implemented in 40 nm technology. The active area target is to be less than 1 mm<sup>2</sup> and the total area less than 5 mm<sup>2</sup>.

### 3.1 Passive integration

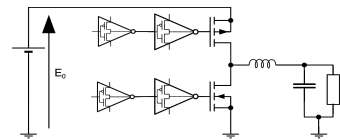
The converter will use high density trench capacitors, and high performance “racetrack” inductors. Passive and active chips will be stacked, using a 3D design approach and manufacturing. This design approach enhances passive performances and limits parasitic losses.

### 3.2 Active integration

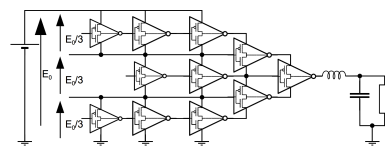
Active design will be made in 40 nm CMOS technology. Nominal technology voltage is 1.2 V. This technology contains high voltage switches (2.5, 3.3 and 5 V), but first simulations will show that their parasitic capacitances don’t allow reaching 90 % efficiency at 200 MHz using a standard power stage (**Figure 3**).

Regular switches will be used, using a cascoded power stage (**Figure 4**). First simulations have shown a significant improvement in efficiency (from 75 % with standard power stage to 85% with cascoded power stage). This structure will be extensively analyzed through simulation in final paper.

A circuit tape-out is scheduled in September allowing for experimental results at time of the conference.



**Figure 3** Standard power stage



**Figure 4** Cascoded power stage

### 3.3 Converter topology and control

Another way to improve efficiency of a DC-DC converter is to use an efficient topology. Many topologies are available for DC-DC conversion; the paper will present an overview of relevant topologies and an evaluation in terms of efficiency. Topologies presented in the state-of-the-art are mainly standard buck and some multi-phases.

## 4 Conclusion

State-of-the-art analysis has shown design objectives and highlighted design challenges. It also provides some ideas to overcome roadblocks.

## 5 Acknowledgements

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## 6 References

No references could be included for the sake of place.