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High Temperature Discrete Integrated Coreless Signal Insulator

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Abstract—For a few years now, some industrialists have been proposing commercial devices to realize the insulation of control signals in power conversion systems. Those devices have been used widely in the field with entire satisfaction. However, for some applications where extreme temperature requirements must be met, those components may not be adequate. In this paper, a discrete solution is presented using three chips: a transmitter, a coreless transformer and a receiver. The transformer chip is built using a copper on glass technology while transceivers and receivers use Silicon On Insulator. Operation with a Pulse Width Modulated signal is presented, the coreless technology was tested at 200°C.

I. INTEGRATED POWER CORE AND INSULATION

When it comes to implementing an Integrated Power Core (IPC), either as laboratory scale demonstrators or for industrial applications, a major issue has to be solved: insulation of the high voltage power circuit from the low voltage control circuit. The resulting voltage stress is focused at a specific point see figure 1. The on/off control digital signal, present on the primary side, is converted to some kind of voltage and current by the gate driver on the secondary site in order to switch the power device in the inverter leg. Engineers and scientists have produced a huge variety of solutions ranging from transformers to optical links systems, not all of them tuned for integration. Recent advances have brought to industrial levels the coreless technology for the insulation of control signals in an integrated driver chip [1]. However, there is an interest in developing a discrete coreless transformer, especially to extend the temperature range to 200°C for instance in order to address aerospace applications, or niches, such as down hole drilling. In that case, several stress parameters must be considered, table I lists the major constraints for a coreless transformer implemented in a high temperature IPC and the resulting impact on the system.

a) A few comments about table I : The temperature affects directly the materials such as resistivity or magnetic permeability, this is taken into account at design level. High temperatures also accelerates aging, this is very true for organic materials. This paper does not address reliability, however the technologies used have been selected for their high temperature capabilities. The insulation voltage is set by multiplying the nominal DC bus voltage by two and adding a safety margin of 50%, hence 1.5 kV for a 540 V supply. The voltage transients are produced by the inverter leg switches and are evaluated to be 50 kV/us. The footprint is a very important constraint

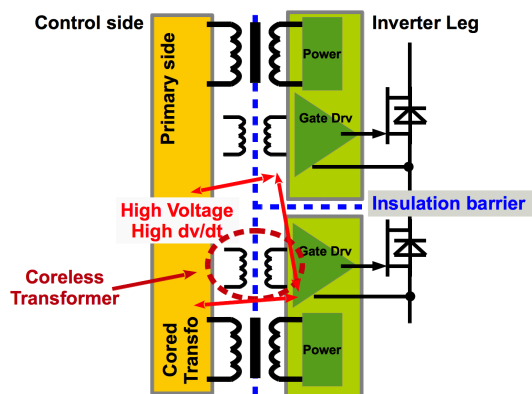


Fig. 1. Bloc diagram of an Integrated Power Core. Insulation is mandatory for both signal and gate driver supply. Coreless transformers are good candidates for the integration of the signal insulation. The insulation transformer is exposed to high voltages and high transients.

TABLE I. CONSTRAINTS

Constraint	Value	Impact
Temperature	200°C	Insulating material
Insulation	1.5 kV	Transformer geometry
Transients	50 kV/us	Transceiver
Footprint	minimal	Transformer inductance

as it affects volume and indirectly mass, two key specification parameters for airborne applications.

II. INTEGRATED CORELESS TRANSFORMER TECHNOLOGY

In this paper, the authors describe a hybrid solution to signal insulation using Silicon On Insulator (SOI) integrated circuits and Integrated Passive Device (IPD). SOI technology is used for the transmitter/receiver chipset and IPD technology for the coreless transformer. The SOI technology is commonly used to extend the temperature range of Silicon integrated circuits, [2]. However, IPD is less common. The IPD Technology developed by STMicroelectronics, see figure 2, is already used in large volumes by major customer worldwide looking for space saving, improved performance, and high standard quality at a competitive cost for Radio Frequency applications. The IPD technology provides superior assembly and test yield

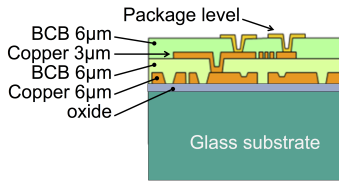


Fig. 2. Cross section of the IPD technology used, showing the two copper layers, the insulating medium and the glass substrate. *Courtesy of STMicroelectronics.*

on the final application as IPD device performance is lower tolerance compared to discrete Surface Mount Devices. The IPD technology uses glass wafers for a substrate and various materials to integrate capacitors and conductors. For a coreless transformer, integrated capacitors are not implemented. The remaining materials are glass, copper and an adhesive insulator based on Benzocyclobutene (BCB) of which the properties are listed in table II. In [3], the coreless technology was tested on a laboratory sample 1000 hours at 200°C, the magnetic properties were not affected, but due to the uncontrolled presence of oxygen, the insulation was damaged. Proper industrial packaging should solve this detrimental aspect.

TABLE II. ELECTRICAL AND THERMAL PROPERTIES OF PHOTO-BCB (CYCLOTENE 4000 RESIN SERIES)

Property	Value
Dielectric constant	2.65 (1kHz – 20GHz)
Dissipation factor	0.0008
Breakdown voltage	5.3 MV/cm
Leakage current	4.7×10^{10} A/cm ² at 1.0 MV/cm
Volume resistivity	1×10^{19} Ω-cm
Thermal conductivity	0.29 W/m ² K at 24°C
Thermal stability	1.7% weight loss per hour at 350°C

The IPD technology provides several means of building a coreless transformer. First, for compact, reduced footprint transformers, the stacked structure is obtained by using both layers of copper to print the windings. The major drawback is an increased inter-winding capacitance which must be as small as possible in order to improve insulation of transients and reduced distance between primary and secondary windings. Secondly, the single layer structure, which is less efficient in terms of uH per footprint, permits to increase the minimum distance between primary and secondary coils, an interesting feature for high voltage insulation and reduced capacitance. In [3], the design equations based on simple physics and analytical approximations, [4] are presented, they permit to estimate the inductance and resistance of the coils and the primary to secondary capacitance of the transformer. The IPD technology is used at its limits in terms of geometry: minimum distance between tracks (spacing = 10 µm), minimum winding cross-section (width = 10 µm), the transformer is built using the single layer layout, see figure 3. The electrical specifications are identical, the selected design parameters are listed in table III.

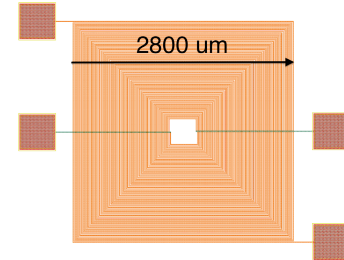
III. INDUCTIVE SIGNAL TRANSMISSION TECHNOLOGY

The principle of inductive signal transmission is to transmit an information through two isolated coupled inductors, such as

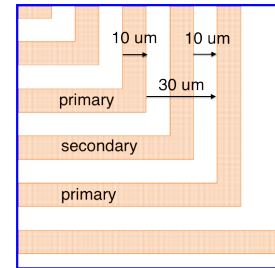
TABLE III. CALCULATED DIMENSIONS OF THE CORELESS TRANSFORMER

Transformer reference : TRS-10w30s300di30n

Design parameter	Value	Dimension	Value
inner diameter	300 [µm]	inductance	1.2 [µH]
width	10 [µm]	capacitance	17 [pF]
spacing	30 [µm]	size	2.6 [mm]
n	30	peak current	25 [mA]



(a) Complete view of the 1 µH transformer



(b) Close-up of the single layer windings

Fig. 3. Real design for 1 µH coils. *Courtesy of STMicroelectronics.*

in a transformer built using a magnetic core and two windings. Depending on the nature of the information, the signal can be directly fed to the transformer or has to be modulated. The widely used On-Off-Keying (OOK) modulation is implemented here. The digital control signal for a power switch presents two states: high and low. The resulting On/Off signal is simply modulated by a high frequency carrier: the on state is coded by the presence of the carrier while the off state is the absence of the carrier. This modulation is relatively safe, the consequence of the loss of signal is the off state and the on state is constantly refreshed by the presence of the carrier frequency. The primary side of the transformer is connected to a transmitter consisting of an OOK modulator and a voltage buffer that should be able to sink and source the current absorbed by the transformer's primary. On the secondary side, the transformer is connected to a receiver that processes the signal in order to output a demodulated signal. Single pulse techniques can be preferred in order to reduce the power consumption, as in [1]. In a wire wound winding transformer designers have a great degree of freedom to fulfill the voltage insulation and the transients specifications. For integrated transformers, the constraint is higher as insulating layers thickness is set by the technology and design rules. Coreless transformers, [5], [6] do not use a magnetic core which relieves some constraints on the design. For the sake of comparison, a reference design uses a transformer made with a toroid on a board implementing two transceivers. A second design implements coreless chips from a first run (RUN1). The

TABLE IV. KEY PARAMETERS FOR TWO INSULATORS

Property	Toroid	Coreless RUN 1
Operating temperature	300°C	> 200°C
Insulation voltage	> 2 kV	> 1.5 kV
Insulation capacitance	< 2 pF	16 pF
Inductance	1.7 uH	1.3 uH
Footprint	7mm x 7mm	3mm x 3mm

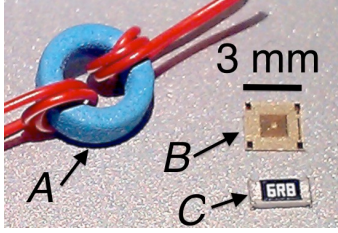


Fig. 4. Photograph showing the reference design toroid transformer, A, and the coreless transformer chip, B. Also shown on the picture, a size 1205 Surface Mounted Device, C.

two transformer technologies are photographed on figure 4. It should be noted that both designs use transceivers which have the same specifications. The key features of those two approaches are listed in table IV.

b) *Transceiver chipset*: the circuit used is a high-temperature, high reliability integrated circuit that implements a dual-channel isolated data transceiver, reference XTR40010. It can be used in any application where there is a need for galvanic isolation of a digital signal. The galvanic isolation is achieved by an external magnetic transformer for each digital signal, this transformer can be coreless, printed circuit board planar with ferrite cores or wire wound on a magnetic torus for instance. The XTR40010 integrates in a single package 2 transceivers (two full duplex channels). The complete solution is optimized to minimize the size of the transformer, the number of external components, the transmission delay (<120ns) and to maximize the noise margin, even in harsh dV/dt conditions (50kV/us across 2pF of insulating capacitance). It is operational beyond the -60°C to +230°C temperature range. The supply voltage ranges from 4.5V to 5.5V. Data rate up to 2 Mbits/second per channel can be achieved and the transient common mode current immunity is 100mA. The

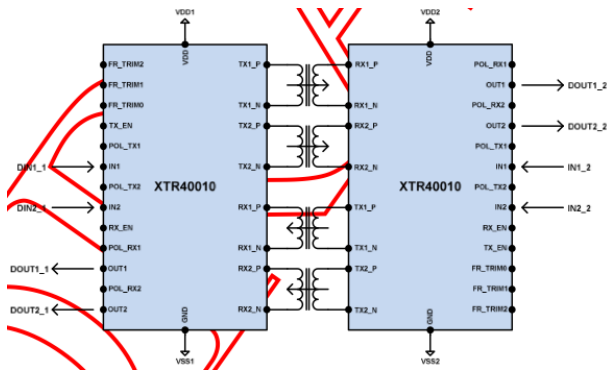


Fig. 5. Application circuit for the transceiver ship-set with the transformers. Courtesy of X-Relsemi.

XTR40010 implements OOK (On-Off Keying) modulation, and has a programmable carrier frequency. The maximum carrier frequency is around 20MHz, it can be noted that no external components are needed apart from the transformers.

IV. TRANSFORMER MODEL

A transformer model is determined for system simulation purposes. The primary impedance is studied to determine the frequency range in which the impedance is mainly inductive. It was found to be 100kHz to 20MHz. Below 100kHz the impedance is so low that the signal to noise ratio impairs the measurement. On a practical point of view, there is no interest in reducing the operating frequency of the transformer. What is looked after is, on the contrary, an increase of the carrier frequency to reduce the coil's driving current and to reduce the physical dimensions. The upper frequency limit for the transformer is set by the parasitic capacitances and the coil inductance with defines a self resonant frequency. Because this frequency is related to parasitics and electrical connections, it would not be a good idea to use this mode of operation for repeatability issues. The other limiting factor for the high frequencies is the ability of the transceiver to source and sink current at high frequency. The coils are measured by an impedance analyzer and matched to a simple equivalent circuit model because it is well adapted to low frequencies, lower than 100MHz. An electrical model schematic is proposed in figure 6.

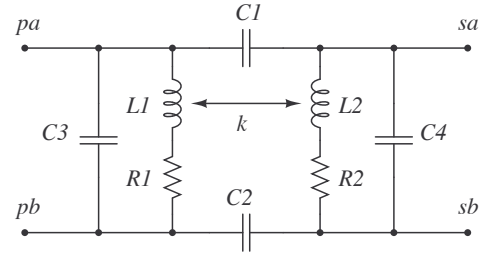


Fig. 6. Coreless transformer model and experimentally identified parameters. Primary terminals are pa and pb , secondary terminals are sa and sb .

TABLE V. EXPERIMENTALLY IDENTIFIED PARAMETERS OF THE CORELESS TRANSFORMER (TRS-10W30S300DI30N).

$L1 = 1300 \text{ nH}$	$C1 = 8 \text{ pF}$
$R1 = 54 \Omega$	$C2 = 8 \text{ pF}$
$L2 = 1300 \text{ nH}$	$C3 = 2 \text{ pF}$
$R2 = 54 \Omega$	$C4 = 2 \text{ pF}$
$k = 0.9$	

The transformer is characterized using an impedance analyzer and several techniques:

- for the inductive part of the model, standard open secondary/short secondary impedance measurement is used to provide $L1$, $R1$ ($L2$ and $R2$ are identical to $L1$ and $R1$ because the geometry is identical) and the coupling factor, k .
- for the primary to secondary capacitance, $C1$ and $C2$, a capacitance measurement is made using circuit (a) from figure 7.

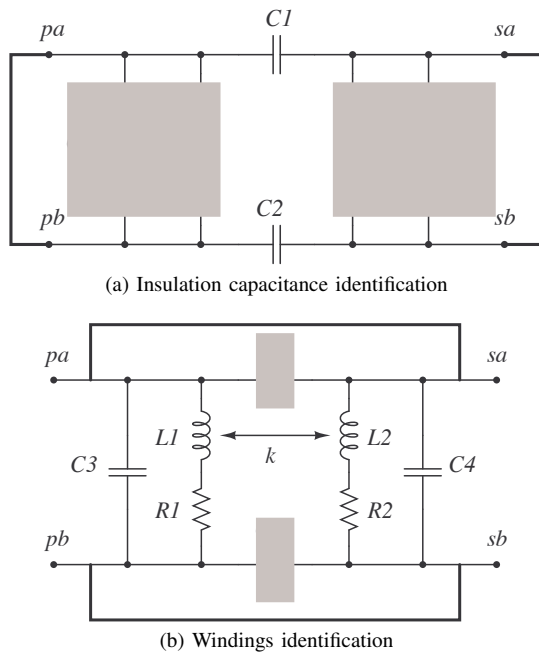


Fig. 7. Characterization of the electrical model of the coreless transformer using shorts, some parts of the circuit disappear because the voltage is nulled in grey areas. The impedance measurement takes place between the shorts. Due to the symmetrical design, the primary coil is identical to the secondary coil, identification can be simplified.

- for the capacitive part of the windings, C3 and C4, the resonance frequency is measured using circuit(b) from figure 7.

V. EXPERIMENTAL VERIFICATION

In order to validate the idea of making a digital signal insulator using a coreless transformer and two transceiver integrated circuits, an experimental board has been built implementing the application circuit of figure 5. The oscillogram plot of figure 8 shows the input signal, top trace (DATA I), the modulated signal and the output signal, bottom trace (DATA O). The performance is listed in table VI.

TABLE VI. MEASURED PERFORMANCE OF THE SIGNAL INSULATOR.

Parameter	Value
Rising edge delay	170 [ns]
Falling edge delay	87 [ns]
Modulation frequency	24 [MHz]

VI. CONCLUSION

A high temperature insulation system is provided using commercially available transceivers and custom made coreless transformers using an industrial process. The coreless transformer was designed to match the transceiver with a minimal footprint (3 mm x 3 mm) which is an improvement over the cored transformer reference design solution. The transmission delay is lower than 170 ns, a figure compatible with high temperature operating converters operating at a switching frequency around 50kHz. Nevertheless, this delay can be taken into account in the digital control system. The

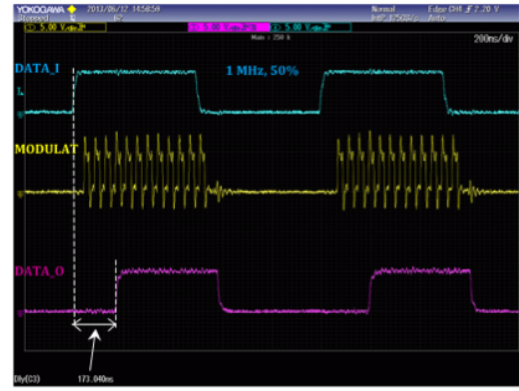


Fig. 8. Experimental verification of the operation of the transceiver ship-set implemented with the coreless transformers. Courtesy of X-Relsemi.

proposed solution reduces the transformer footprint and height by a factor of 5 when compared with a transformer using a toroid magnetic circuit.

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REFERENCES

- [1] M. Munzer, W. Ademmer, B. Strzalkowski, and K. Kaschani, "Insulated signal transfer in a half bridge driver ic based on coreless transformer technology," *Power Electronics and Drive Systems, 2003. PEDS 2003. The Fifth International Conference on*, vol. 1, pp. 93–96, nov. 2012.
- [2] K. Falahi, B. Allard, D. Tournier, and D. Bergogne, "Evaluation of commercial soi driver performances while operated in extreme conditions," in *Integrated Power Electronics Systems (CIPS), 2010 6th International Conference on*, 2010, pp. 1–3.
- [3] D. Bergogne and all, "Integrated coreless transformer for high temperatures design and evaluation," *ECCE-Power Electronics and Applications (EPE 2013), Proceedings of the 2013-15th European Conference on*, pp. 1–6, sept. 2013.
- [4] S. S. Mohan, M. del Mar Hershenson, S. P. Boyd, and T. H. Lee, "Simple accurate expressions for planar spiral inductances," *IEEE journal of solid-state circuits*, vol. 34, pp. 1419–1424, oct. 1999.
- [5] G. Fontana, "Coreless transformers with high coupling factor," *Review of Scientific Instruments*, vol. 66, no. 3, pp. 2641–2643, 1995.
- [6] S. Timothe, R. Nicolas, C. Jean-Christophe, and A. Jean-Daniel, "Design and characterization of a signal insulation coreless transformer integrated in a cmos gate driver chip," in *Power Semiconductor Devices and ICs (ISPSD), 2011 IEEE 23rd International Symposium on*, 2011, pp. 360–363.