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Keywords

<<Passive component>>, <<Device characterization>>, <<Integrated Circuit (IC)>>

Abstract

A novel coreless technology based on an existing process, initially designed to produce integrated passive components for commercial temperatures, is used and its capability at 200°C is tested. Design aspects and electrical characterizations of the samples are presented. Finally, an endurance test shows a satisfactory behaviour at high temperatures.

Introduction

Ever since power electronics converters were implemented, either as laboratory scale demonstrators or in industrial applications, a major issue had to be solved: insulation of the high voltage power circuit from the low voltage control circuit. The resulting voltage stress is particularly focused at a specific point where digital meets power, the driver. The on/off digital signal is converted to some kind of voltage and current in order to turn the power device on or off. Engineers and scientists have produced a huge variety of solutions ranging from transformers to optical systems links. Recently coreless transformers have gained popularity as it is now possible to integrate them with driver integrated circuits,[4, 5, 1]. For some applications especially or when full integration is not practical, it could be advantageous to have a discrete integrated coreless component. This is the first goal of the work described in this paper. More, recent applications involve high operating temperatures (the ambient is over 200°C), where the driver, closely placed to the power core, is stressed at the same time by high voltages and high temperatures. The second goal of the research involved here is the extension of the temperature range of the industrial process that is used to produce the coreless chips.

Coreless transformer for insulating control signals in a power converter at high temperatures

Recent advances have brought to industrial level the coreless technology for the insulation of control signals in an integrated driver chip [4]. However, there is an interest to develop a discrete coreless transformer. In fact, discrete components require less development efforts than fully integrated systems and permits flexibility in various applications for example. The authors are studying an existing technology designed for for a mass production market in order to evaluate it for an airborne high temperature application specified in table I.

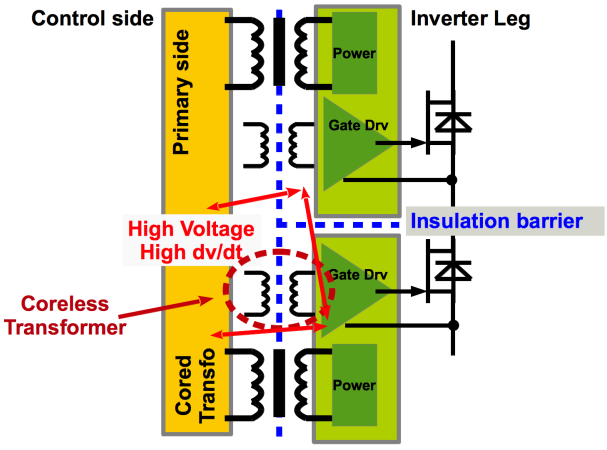


Figure 1: Bloc diagram of an Integrated Power Core. Insulation in mandatory for both signal and gate driver supply. Coreless transformers are good candidates for the integration of the signal insulation.The insulation transformer is exposed to high voltages and high transients.

Table I: Specifications for the insulation system of control signals for inverters used in airborne applications.

Parameter	Value	Constraint
DC breakdown voltage	$>$ 2 kV	Insulating resin dielectric strength and thickness
dv/dt immunity	$>$ 75 kV/us	Transmitter and Receiver electronics
Parasitic capacitance	$<$ 18 pF	Insulating resin dielectric constant and thickness
Low Temperature ambient	-50 °C	Materials and electronics
High Temperature ambient	+200 °C	Materials and electronics
Temperature cycling	$>$ 30 000 cycles	Assembly, packaging
Life span	50 000 hours	Ageing of insulation material and assembly

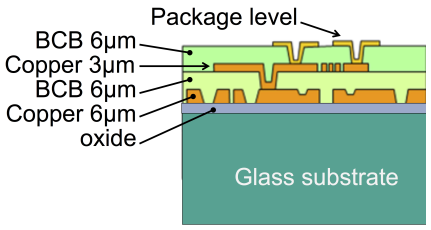
Coreless technology

Coreless transformers are processed using Integrated Passive Device technology (IPD) from STMicroelectronics. It consists of a glass wafer onto which two layers of copper are placed, insulated by a specific resin. It should be noted that the resin is a broad band-sensitive photopolymer named B-staged bisbenzocyclobutene (BCB). It is intended to be used as dielectrics in thin film microelectronics applications. The specifications for the BCB used in our process are given in table II. This polymer was not specially developed for high temperature applications, however the process of reticulation that happens during the initial curing process leads to believe that an extension of the usual temperature limit (125°C to 175°C) is achievable. For this purpose, an endurance test is carried out and described further down. Note that the windings are made of copper and have a square shape, they are built using two layers of metal,

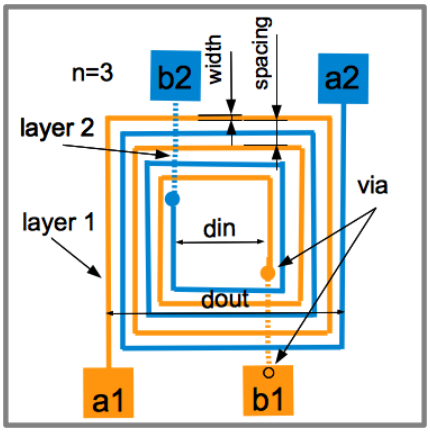
see figure 2. The primary winding and the secondary winding are etched on the same metal level, while the second metal level is used to "bring back" the extremum of the coil from the center of the device to the side of the chip. For some applications it is necessary to have the contact pads at the corner of the chip, for improved insulation in the package for example. This implementation is called "single layer" transformer and is noted "TRS". It was chosen over a double layer structure because the parasitic capacitance is less. In the double layer structure, an additional capacitance is introduced by the coils facing each other to form a plannar capacitor.

Table II: Electrical and Thermal Properties of Photo-BCB (CYCLOTENE 4000 resin series)

Property	**Value**
Dielectric constant	2.65 (1kHz – 20GHz)
Dissipation factor	0.0008
Breakdown voltage	5.3 MV/cm
Leakage current	4.7 x 10^{10} A/cm2 at 1.0 MV/cm
Volume resistivity	1 x 10^{19} Ω-cm
Thermal conductivity	0.29 W/m°K at 24°C
Thermal stability	1.7% weight loss per hour at 350°C



Simplified cross section of the technology used for the coreless transformer. Integrated Passive Device technology (IPD) used for the realization of cordless transformers. *Courtesy of STMicroelectronics*



Simplified top view of the coreless transformer showing design parameters for single layer transformer topology (TRS)

Figure 2: Technological description of a single layer transformer.

Table III: Geometrical limits for copper tracks used in the coreless transformer

Parameter	**Value**
track thickness	6 μm
minimum track width	10 μm
minimum etching distance	10 μm

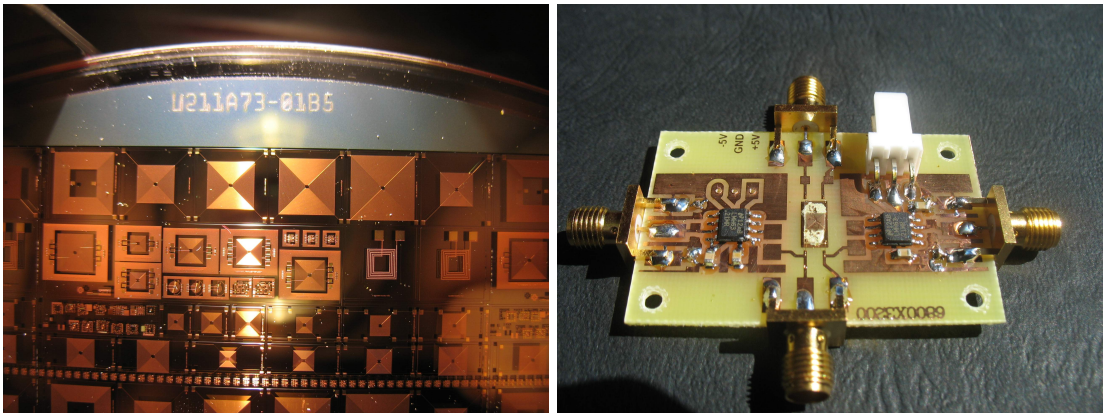


Figure 3: Left: photograph of a limited area of the wafer showing the various experimental patterns. Right: one of the tests boards developed for the coreless transformers chips.

Coreless design

The design of the coreless transformer is based on system specifications such as maximum frequency and current for the transformer transceiver, maximum mechanical dimensions and the 200°C operating temperature. The coreless transformer is fed with a 5V square wave at 20MHz, this data permits to calculate the peak current that the transceiver has to produce. The integration objective sets the maximal mechanical size. Designing the coreless transformer is basically a three step iterative process. First, usage of a formula, see equation 1, to compute the inductance of a flat square coil according to [3], the winding resistance and the mechanical size. The technology description is presented in figure 2. Secondly, the calculus of the peak current for a fixed voltage and frequency. Thirdly, the parasitic capacitance is estimated. The input parameters are : inner diameter din, track width w, track spacing s, number of turns n. Using a modified Weeler inductance equation and an empirical capacitance equation, the output parameters are calculated: track resistance $rtrk$, transformer's primary inductance lmw and primary to secondary parasitic capacitance $capa$. These equations are listed in Table IV and the result, an optimized transformer, is presented in Table V. Three constraints are taken into account: mechanical dimensions $<$ 3mm, transceiver drive current $<$ 25mA and parasitic capacitance between primary and secondary coils $<$ 15pF. Many solutions, ranging from 30 turns to 60 turns, have been built with different layout options in a first explorative wafer run. In this paper, the optimal solution is presented, a single layer 30 turn transformer with maximized winding density: minimal allowed track spacing and width.
The parasitic capacitance between the primary winding and the secondary winding can be evaluated by considering single layer structure of the transformer. Two wires, primary and secondary are wound side by side producing a wire-to-wire capacitance. The resulting capacitance is calculated using the design equation "capa" from table IV in which the rectangular shape of the wire has been approximated to a circle to match the generic expression of the capacitance of two wires placed side by side.

$$L_{mw} = \mu_0 K_1 \frac{n^2 d_{avg}}{1 + K_2 f_r} \tag{1}$$

$$\begin{aligned} &\text{for a square inductor: } K_1 = 2.34 \quad \text{and } K_2 = 2.75 \\ &\qquad n \text{ is the number of turns} \quad \text{and } \mu_0 = 4\pi 10^{-7} \\ &\text{with } d_{avg} = \frac{din + dout}{2} \qquad \text{and } f_r = \frac{dout - din}{dout + din} \end{aligned} \tag{2}$$

Table IV: Design equations for the integrated single layer coreless transformer. Please refer to figure 2 for the geometrical signification of parameters.

$$
\begin{aligned}
dout &= din + 2n(w+s) \\
davg &= (din + dout)/2 \\
len &= 4\ davg\ n \\
fr &= \frac{dout - din}{dout + din} \\
rtrk &= \frac{\rho\ len}{w\ t} \\
lmw &= \frac{\mu_0\ K_1\ davg\ n^2}{1 + K_2\ fr}
\end{aligned}
$$

$$
d = w + s/2 \quad a = (w+t)/\pi \quad K_1 = 2.34 \quad K_2 = 2.75 \quad \epsilon_0 = 8.810^{-12} \quad \rho = 1/51300000
$$

$$
capa = \frac{\pi\ \epsilon_0\ \ len}{log(d/2a + \sqrt{(d^2/(4a^2)) - 1})}
$$

Table V: Dimensions of the coreless transformer computed from the values of the design parameters.

Transformer reference : TRS-10w30s300di30n

Design parameter	Value	Dimension	Value
inner diameter	300 [μm]	inductance	1.2 [μH]
width	10 [μm]	capacitance	17 [pF]
spacing	30 [μm]	size	2.6 [mm]
n	30	peak current	25 [mA]

Electrical characterisation

For the purpose of verification and checking the design equations the transformer is characterized using an impedance analyzer. The primary impedance is studied to determine the frequency range in which the impedance is mainly inductive. It was found to be 100kHz to 20MHz. Below 100kHz the impedance is so low that the signal to noise ratio impairs the measurement. On a practical point of view, there is no interest in reducing the operating frequency of the transformer. What is looked after is, on the contrary, an increase of the carrier frequency to reduce the coil's driving current and to reduce the physical dimensions. The upper frequency limit for the transformer is set by the parasitic capacitances and the coil inductance with defines a self resonant frequency. Because this frequency is related to parasitics and electrical connections, it would not be a good idea to use this mode of operation for repeatability issues. The other limiting factor for the high frequencies is the ability of the transceiver to source and sink current at high frequency. The coils are measured by an impedance analyzer and matched to a simple equivalent circuit model because it is well adapted to low frequencies, lower than 100MHz. An electrical model schematic is proposed in figure 4.

Coupling factor The coupling factor k is a key parameter and is calculated from two measurements made on the primary coil of the transformer, [2]. Equation 3 gives the coupling factor value as a function of two inductance measurements made on the primary coil, L_{oc}: open secondary and L_{sc}: short-circuited secondary. Due to the compactness of the chosen technology, the coupling factor is very good, $k = 0.9$.

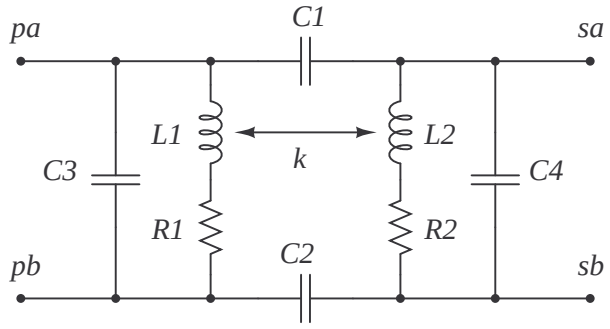
$$
k = \sqrt{\frac{L_{oc} - L_{sc}}{L_{oc}}} \tag{3}
$$

Parasitic capacitance. To determine the parasitic capacitance between primary and secondary coils, the coils are short-circuited and a measurement of capacitance is made, corresponding to the parallel association of $C1$ and $C2$, see figure 5(a). The measured capacitance is 16pF, which complies with the global specifications of table I. Because of the symmetry of the transformer, one can assume that the capacitance is evenly spread between $C1$ and $C2$, see figure 4.

Winding capacitance. The winding capacitance is determined by measuring the self resonance frequency f_{sr} of the transformer while shorting the insulation between primary and secondary in order to reject the effect of such a capacitance.

$$C = \frac{1}{L_{eq}(2\pi f_{sr})^2} \qquad \text{with} \quad L_{eq} = \frac{1-k^2}{2(1-k)}L1 \tag{4}$$

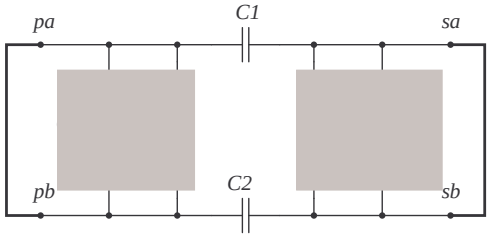
The equivalent circuit becomes two coupled inductors (giving an inductance L_{eq}) placed in parallel with a capacitor C, see figure 5(b). Again, by using symmetries in the transformer, here, $L1$ and $L2$ are identical, one can determine the resulting inductance using equation 4, where L is the primary inductance measured with an unloaded transformer and k the coupling factor already determined. The capacitance C calculated using equation 4 is the equivalent capacitance of $C3$ and $C4$ placed in parallel because $C1$ and $C2$ have been shorted to experimentally determine the self resonant frequency. Finally, The winding capacitance is 2pF for each coil.



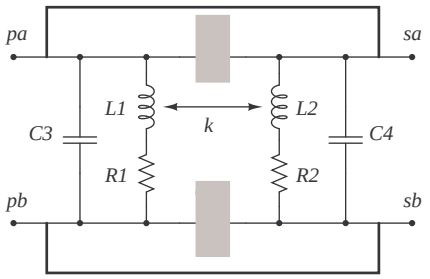
$L1 = 1300\ nH$
$R1 = 54\ \Omega$
$L2 = 1300\ nH$
$R2 = 54\ \Omega$
$k = 0.9$

$C1 = 8\ pF$
$C2 = 8\ pF$
$C3 = 2\ pF$
$C4 = 2\ pF$

Figure 4: Electrical model of the coreless transformer with the values of the identified parameters. Primary terminals are *pa* and *pb*, secondary terminals are *sa* and *sc*.



(a) Parasitic capacitance identification



(b) Self-resonant freq. identification

Figure 5: Characterization of the electrical model of the coreless transformer using shorts, some parts of the circuit disappear because the voltage is nulled in grey areas. The impedance measurement takes place between the shorts.

Electrical tests

Measuring electrical parameters is a first step to determine if a component technological solution is valid. Secondly, it is needed to prove that the component is able to provide it's functionality in a practical application. For that, an experimental test board has been developed. In comprises an onboard adjustable oscillator – 4 to 40 MHz range – for the carrier signal, a modulator controlled

by an external Pulse Width Modulation signal and a bridge coil driver on the primary side. The modulator uses synchronized gating to produces full carrier periods during the on-state of the PWM signal and zero differential voltage during the off-state of the PWM signal. In that way, the inductive coil of the coreless transformer is never excited by portions of square waves and is not submitted to any DC voltage component. On the receiver side, a passive network is connected to the secondary coil, adapting the coreless output to an amplitude modulation detector. Figure 6 shows the measurements made using an oscilloscope on the demonstrator board. The modulated signal has been transmitted successfully through the coreless transformer and the level of the received signal is strong, a 2 V amplitude square wave. This signal is compatible with many detector circuits, from example a re-triggerable one-shot circuit.

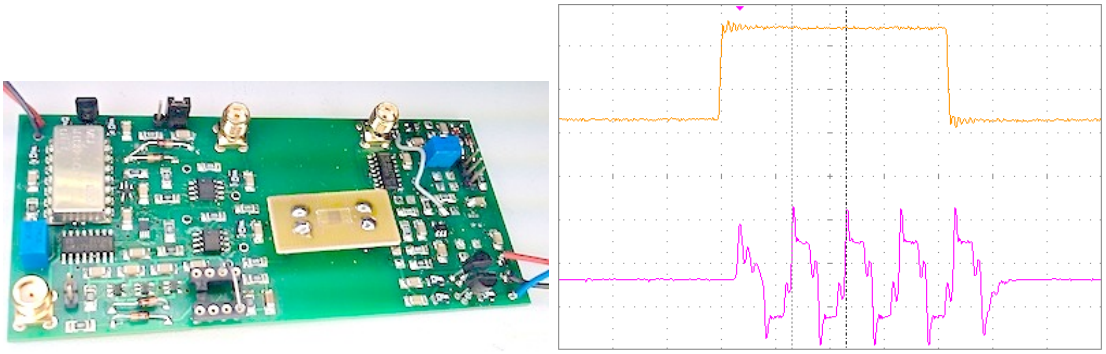


Figure 6: Left. The evaluation board implementing the 20MHz modulation, a piggy-back circuit with the coreless sample, a receiver circuit. Right. Oscilloscope measurement showing : Top trace, PWM input signal prior to modulation at 20MHz, 5V amplitude and Bottom trace, the received modulated signal, 2V amplitude. The time base is 200ns/div.

High temperature endurance test

The first step in endurance tests is to place the component under a constant high temperature of 200°C. Temperature cycling is another aspect that will be treated in a second step, nevertheless, during the experiment, the coreless transformer has been cycled more than 500 times, every time it was taken out of the oven for the impedance measurement at room temperature. The technology implements glass, copper and an organic matter, BCB. The study focuses on the BCB as it is known that organic materials are more sensitive to high temperatures than metals or mineral compounds. The coreless transformer, as any transformer, has a parasitic capacitance

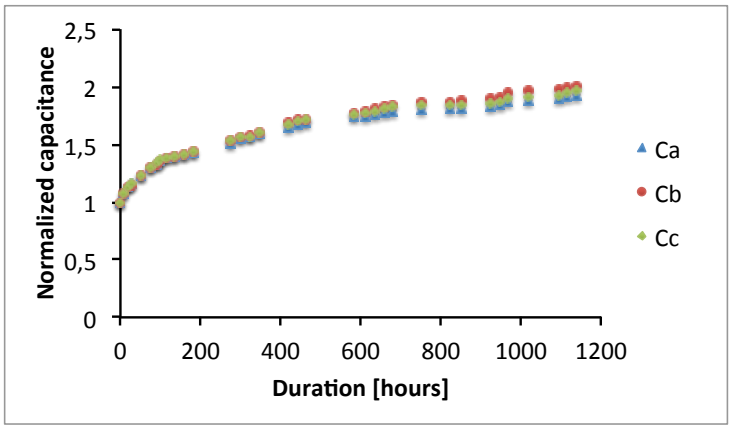


Figure 7: Measured normalized capacitance versus the number of hours at 200°C. Three transformer chips are tested, some dispersion occurs with aging. The variation of capacitance is used as an indicator of aging.

between the primary winding and the secondary winding. The idea is to monitor the evolution of

the transformer capacitance during the endurance test. The test consists in placing the samples at 200°C for a long period compared to the initial curing time of the BCB used for the insulation. Measuring the insulation resistance does not seem to be very reliable as oxidation on the pads might occur. Capacitance measurement can be made independent of resistance variations.
The increase of capacitance can be explained by two different phenomena: weight loss of the BCB and modifications of the molecular arrangement. The physical basic formula to calculate the capacitance, C, of two flat metal parts of surface, S, separated by a distance, e, with a material of dielectric constant ϵ_r is: $C = \epsilon_0 \epsilon_r \frac{S}{e}$ with $\epsilon_0 = 4\pi 10^{-7}$. So, as the copper structure is unlikely to be modified – S remains constant –, the weight loss impacts the volume of dielectric material, resulting in a reduction of the distance, e. The other possibility is a chemical evolution of the molecules that affects the dielectric constant. After checking of the experimental protocol it was found that the BCB of the coreless transformer had been exposed to ambient oxygen resulting in an oxidation at high temperatures. Such a phenomenon is well known and can be avoided using controlled atmosphere airtight packaging or protective overlaying with silicone gels for example. The aging that is observable on figure 7 is due to a lack of appropriate packaging, it will be corrected in the next endurance experiment. Nevertheless, the integrated coreless transformer was proved to withstand high temperatures, it is only the insulation that was degraded by the uncontrolled action of oxygen.

Conclusion

A specific integrated coreless component was designed and fabricated using an industrial production process. It was characterized using a specific simplified model. Electrical measurements gives a magnetic coupling factor of 0.9 and a primary to secondary capacitance of 16pF, which are two key parameters when designing a control signal insulation system for a power converter. During a preliminary aging test, a significant variation of the parasitic capacitance indicates a variation in the insulating material, this was due to an uncontrolled oxygen exposition of the samples. A new test using hermetic packages with gel is programmed in order to verify the possibilities of this technology at high temperatures. Further work encompasses extended endurance tests, implementation of the coreless transformer component in a transmitter-receiver circuit.

References

[1] K.E. Falahi, B. Allard, D. Tournier, and D. Bergogne. Evaluation of commercial soi driver performances while operated in extreme conditions. In *Integrated Power Electronics Systems (CIPS), 2010 6th International Conference on*, pages 1–3, 2010.

[2] G. Fontana. Coreless transformers with high coupling factor. *Review of Scientific Instruments*, 66(3):2641–2643, 1995.

[3] Sunderarajan S. Mohan, Maria del Mar Hershenson, Stephen P. Boyd, and Thomas H. Lee. Simple accurate expressions for planar spiral inductances. *IEEE journal of solid-state circuits*, 34:1419–1424, oct. 1999.

[4] M. Munzer, W. Ademmer, B. Strzalkowski, and K.T. Kaschani. Insulated signal transfer in a half bridge driver ic based on coreless transformer technology. *Power Electronics and Drive Systems, 2003. PEDS 2003. The Fifth International Conference on*, 1:93–96, nov. 2012.

[5] S. Timothe, R. Nicolas, C. Jean-Christophe, and A. Jean-Daniel. Design and characterization of a signal insulation coreless transformer integrated in a cmos gate driver chip. In *Power Semiconductor Devices and ICs (ISPSD), 2011 IEEE 23rd International Symposium on*, pages 360–363, 2011.