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Failure Analysis of ESD-stressed SiC MESFET

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Abstract

Reliability studies are required for SiC device development. In a previous work we studied the intrinsic ESD robustness of a SiC MESFET. The failure mechanism was related to the triggering of an NPN parasitic transistor. In this work, a new MESFET layout is considered, which optionally include a Zener diode for internal protection. TLP testing and failure analysis has been carried out. Two new failure mechanisms are evidenced. Based on this knowledge, solutions are proposed to further improve the ESD robustness.

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1. Introduction

Due to Silicon Carbide (SiC) intrinsic properties, SiC based devices enable high voltage, high frequency, high temperature applications and are becoming significant actors of the power-devices market. However, reliability studies have to be carried-out in order to improve and accelerate their development. Qualifying devices against ElectroStatic Discharge (ESD) is a key factor for power modules. In a previous work on SiC MESFET, we have demonstrated that the avalanche triggering of a parasitic NPN transistor during an ESD was responsible of low ESD failure level [1].

In order to facilitate the integration of these MESFET's, a new architecture has been designed, with a planar isolation [2]. In this work two new devices are compared: one reference structure and one including an additional internal Zener diode protection. We analyse the ESD robustness of each device with a TLP test, and discuss the different observed failures. Understanding the failure mechanism should help improving the ESD robustness of SiC MESFET.

2. Presentation of the different elements

2.1. Description of the two different MESFET's

In a previous work, an ESD failure analysis on a SiC mesa MESFET has been carried out. Triggering of a parasitic NPN transistor due to the avalanche multiplication, was reported and was limiting the ESD robustness [1].

A completely new MESFET layout has been created in order to facilitate integration on the same crystal of the driver near the power device. The main transformation of the layout is related to the device isolation. Instead of mesa isolation, a P⁺ diffusion circled the N channel. Drain corners are not circular anymore, and inter-electrode distances have changed as well compared to the previous-work version.

The new elementary cell allows a larger flexibility for the circuit designers. For example, with this elementary cell, three types of device were generated, one buffer MESFET, one signal MESFET

and one power MESFET [3]. The device is *normally on* with a -16 V pinch off voltage (**Figure 1**). The drain current saturation of one cell is equal to 16 mA and its normalized current density is $J_{ds} = 60.6 \text{ mA/mm}^2$. The intended operating voltage of this driver is 0-10V. The body electrode can be used as a second gate. Global area of the device is 400 μm . Despite the normally on state of these devices high performance circuitry can be design at the expense of a higher circuit complexity like oscillators, like differential pair of like totem pole [4].

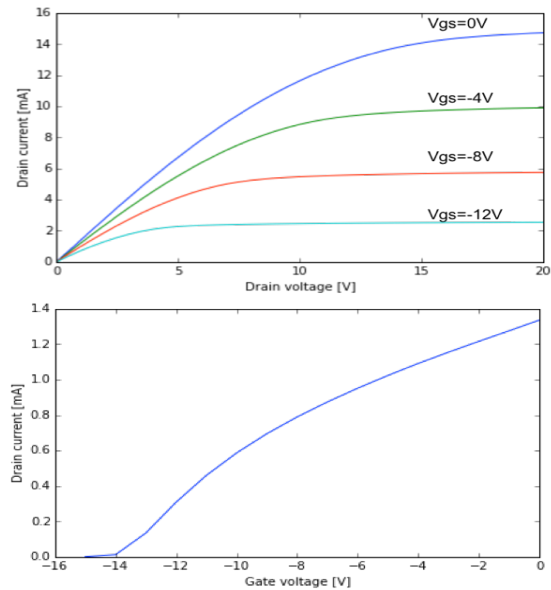


Figure 1: Id-Vd and Id-Vg static measurement at room temperature of normally on MESFET. Body and Source electrodes are grounded. Id(Vg) curve is measured for Vd=1V

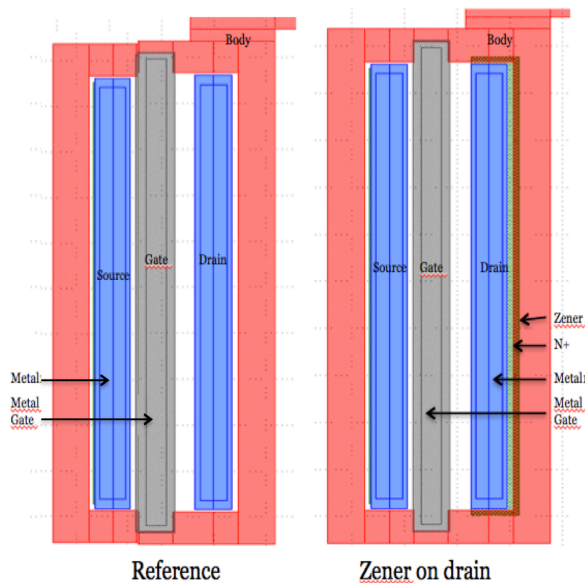


Figure 2: layout of planar Reference MESFET and Zener on Drain MESFET (MZD). In red, the P⁺ isolation circled the three electrodes and is connected to the body pad. The Schottky metal (Nickel) is represented in grey. In green, below the blue metal, is the N⁺ area. The two-micron-long common area between N⁺ and P⁺ represents the Zener diode.

Layouts of the new structures are presented in Figure 2. In red, the P⁺ isolation circled the three electrodes and is connected to the body pad. The Schottky metal (Nickel) is represented in grey. In green, below the blue metal, is the N⁺ area. The two-micron-long common area between N⁺ and P⁺ represents the Zener diode.

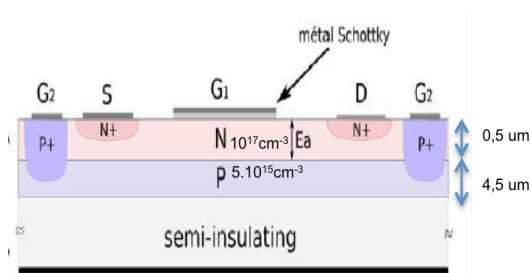


Figure 3: Schematic of cross section of Reference MESFET.

The structure is composed of 0.5 μm thick N channel doped at 10^{17} cm^{-3} and a 4.5 μm thick P layer doped with arsenic at $5.10^{15} \text{ cm}^{-3}$. From each side of the device, we found the P⁺ ring isolation

doped at $4.10^{19} \text{ cm}^{-3}$ (Figure 3).

One device has been designed in order to bring an internal overvoltage protection using a Zener diode, located near the drain electrode. This protection doesn't impact the normal operation (0 to 10 V) and doesn't induce any space penalty. Dynamic behavior and signal consequences are not studied yet Static behavior is focused. This protected device will be named "protected" in the following while the standard device will be named "reference". A Zener diode is often used for ESD protection because of his capacity for driving current without being broken in both forward and reverse operation. That's its goal placed near the body.

The added diode has no impact on the standard IV characteristics of the protected MESFET in the considered standard biasing operation, with gate and body floating. The electrical characteristic of the standalone Zener diode is presented on Figure 4, measured between drain and body with gate and source grounded (same result with gate biased). A 50 Ω series resistance and a Zener voltage of around 30V is measured, that corresponds to the Zener effect in SiC Zener diode [5].

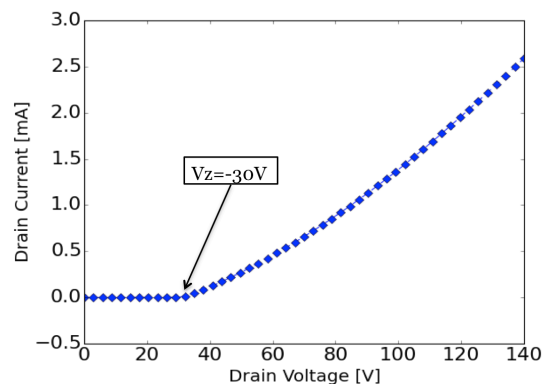


Figure 4: Zener diode electrical characteristics between body and drain electrodes; gate and source are floating. At 3V the diode starts to conduct current in reverse.

2.2. ESD test

A Transmission Line Pulse (TLP) has been used. TLP is a pulsed IV measurement, used in this case in order to correspond, in term of stress, to a Human Body Model (HBM) discharge, which simulate a human-being electrostatic-

discharge in an electronic device. HBM is however an ESD qualification standard. The difference between both tests is in the transmitting power. TLP can only give an estimate of the ESD robustness. It provides a 100ns current pulse with one nanosecond rise time, which is applied on the drain electrode while the source is grounded and body and gate electrode are left floating. Experiments are performed at ambient temperature. After each pulse, a static measurement (DC leakage) allows to verify that the device is not broken. Voltage-pulses level is increased until a physical impact is observed, or until the DC leakage is shifted by more than 10% compared to the reference curve. Because of the short pulses length, self-heating in the device is limited, and thus, the maximum TLP voltage and current are expected to be higher than the allowed maximum static values.

3. Results and comments

3.1. ESD Robustness for reference device

For the reference device, the characterization results of the drain to source pulsed stress are quite scattered (Figure 5). In a range of 150-260V, a large current increase occurs suddenly. Nevertheless the same damage is always instantly created and observed in the drain-diffusion corner of the device below the metal electrode (Figure 6). In a following section we will try to understand why as soon as the current increase the device is broken. As no overcurrent can be accepted before failure, the reference device is not ESD robust.

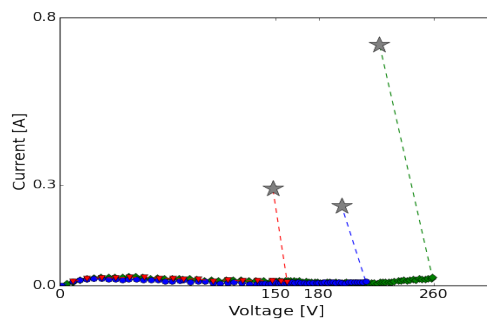


Figure 5: TLP I(V) characteristics of three experiments for the reference SiC MESFET. The grey stars indicate the point were the devices were broken.

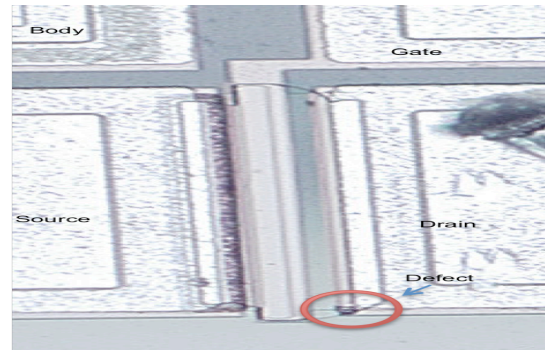


Figure 6: Damage localization for the reference MESFET, at the drain corner after TLP test.

3.2. ESD Robustness for Zener on drain device

The TLP measurement results for the Zener on drain MESFET were perfectly reproducible (Figure 7) on three samples. At 115V, the current starts to increase but the devices are not degraded. The Zener should drive some current in reverse even if we have seen before (Figure 4) that the Zener was triggered in static measurement for a lower voltage (~30V). The high serial resistance of the diode due to the P⁺ ring and the poor resolution of the TLP tester at low current levels can explain this difference. In all case the device is broken only for a current level greater than 0.91A. For MZD experimental results, the red curve shows TLP characteristic of an undestroyed device (test was stopped before any degradation) whereas for the blue one the device was destroyed at 0.91A. The Green curve device seems to present a different failure mechanism. Indeed the FIB cross section image (Figure 8) shows a defect located at the surface, in addition to the classical defect associated with MZD device failure as it is demonstrated in the following part. It is supposed that the TLP test did not capture the first failure of the device and continue the test to higher voltages, which triggered the same failure mechanism of the unprotected device i.e. oxide breakdown.

Concerning the MZD devices tested, the microscope image let suppose that the damage is an internal breakdown at the P-N junctions (Figure 9). The defect appears suddenly at one or both side of the drain and is located below the metallization at the extremities whereas for the previous defect (reference device) the oxide and metallization layer were melted.

About one ampere of pulsed current can be conducted and 160 V hence it can sustain around

150 Watts during 100 ns before being broken.

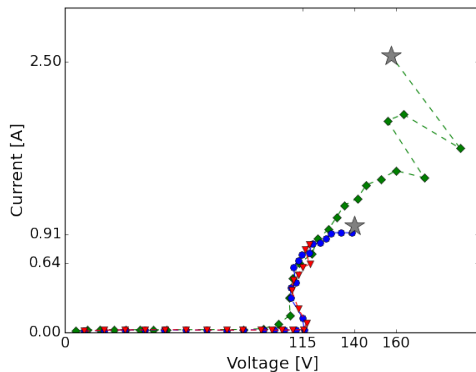


Figure 7: TLP Id-Vd for MESFET with Zener on drain. The grey stars indicate when the devices were broken (if broken).

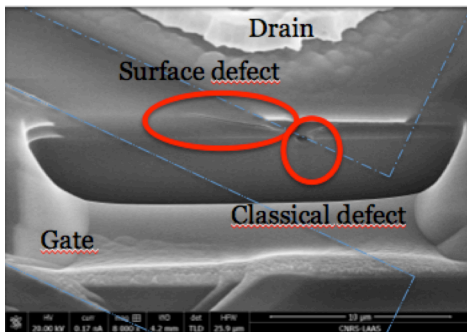


Figure 8: SEM photography of FIB analysis of unusual breakdown for MZD for MZD

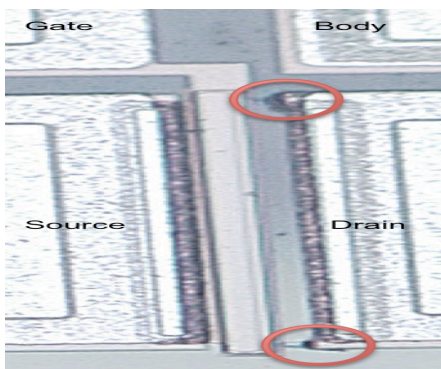


Figure 9: Failure after TLP test on Zener on drain MESFET.

These results were analyzed with the help of Sentaurus TCAD simulations (Figure 10). Simulation allows to obtain the same triggering voltage for the standalone Zener (i.e. $V_z=30$ V) but as the internal body resistance is not the same in

experiment than in simulation, the avalanche looks to start earlier in simulation (30 V instead of 115 V).

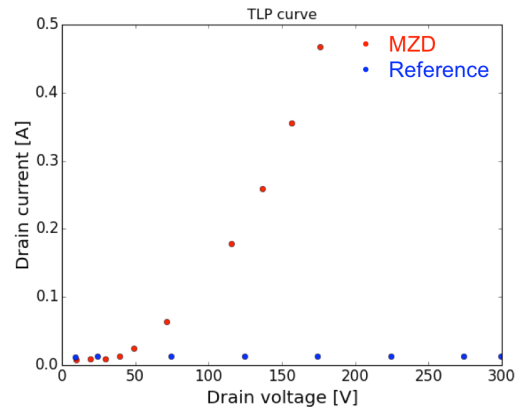


Figure 10: TCAD Sentaurus simulation TLP Id(Vd) result. MZD current increase at $V=30$ V

3.3. Failure analysis

As described above, for the reference device, the defect appeared suddenly before any drain current increase whereas in the MESFET of the precedent study (old layout), a slight current increase was noticed before breakdown. This increase was related to the start of the avalanche generation and a parasitic NPN parasitic transistor triggering. Therefore the failure mechanism of the new design device seems to be different from the old layout ones.

In the following section we will try to understand what is the failure mechanism in both the case of the reference and protected device. The role of the Zener diode will be also investigated and the parasitic NPN transistor behavior will be described as eventually responsible of the failure observed.

3.3.1 Zener robustness

We have investigated the ESD robustness of the standalone Zener diode. It is demonstrated here that this diode is robust against ESD and is not limiting the robustness of the whole device. Indeed, before being damaged, the diode can hold around 400V in TLP (Figure 11), and its failure signature is different from the one of the protected MESFET. We biased the drain while body was grounded and source and gate electrodes were kept floating (settings with MESFET gate blocked was tested but didn't

change the result). The failure is located at the surface of the device between the drain and body pads, in the P⁺ layer (Figure 12). It corresponds to the “melting” of the P⁺ diffusion that connects the P⁺ ring to the substrate pad. Furthermore, the total current that this Zener diode can carry is rather low (around 400V the current is about 20 mA). Therefore, the main current in the protected MESFET does not only flow through this diode that, therefore, cannot directly explain the observed damages of the protected device.

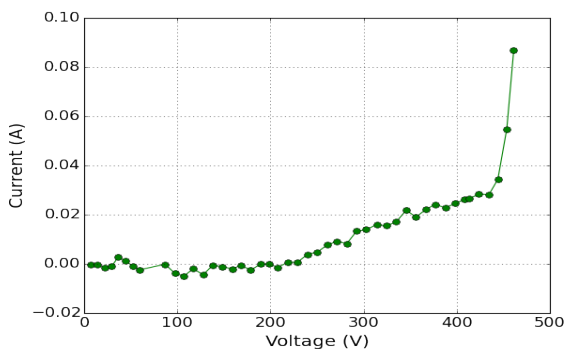


Figure 11: TLP on the Drain Body Zener diode. Significant TLP current is detected only above 200V. The diode can sustain more than 400V before being broken but it only carries few tens of milliamps before being degraded.

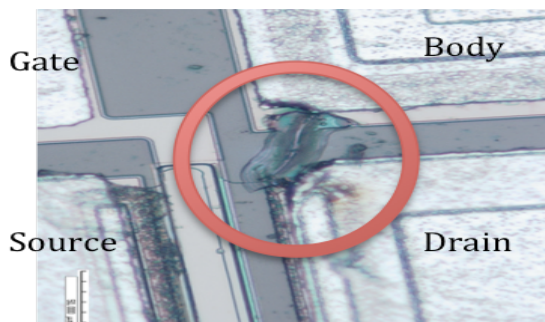


Figure 12: Defect created by TLP stress on the standalone Zener diode.

3.3.2 Reference failure

The failure of the reference device seems to be related to passivation layer damage. We have carried-out a Focus Ion Beam (FIB) and SEM analysis on one defective device. We observed a vertical hole in the passivation layer that stops before the substrate SiC layer. We have identified the observed layers with the device layout (Figure 13). Metal 2 is covering the P⁺ isolation. This overlap is not very large but the electric field in the

corresponding insulator region might be very high. Indeed we have an electrical-potential difference between the P⁺ that has a potential closed to the source potential (hence at 0V) and the metal 2 where the drain voltage is applied. We know SiO₂ layer breakdown field is around 3 to 5 MV/cm² for this type of dielectric. The oxide layers thickness (Figure 14), from P⁺ surface to underlying metal 2 is about 0,5 μm of SiO₂. Therefore, the passivation layer can normally held around 150-250V before breaking. A hole is then created because of the temperature increase due to the high electric field and current density at this point. Simulation result (Figure 10) corroborates the high electric field in the oxidation layer hypothesis. Therefore oxide is removed and a slight hole in the SiC is produced by high temperature and sublimation process occurring with SiC.

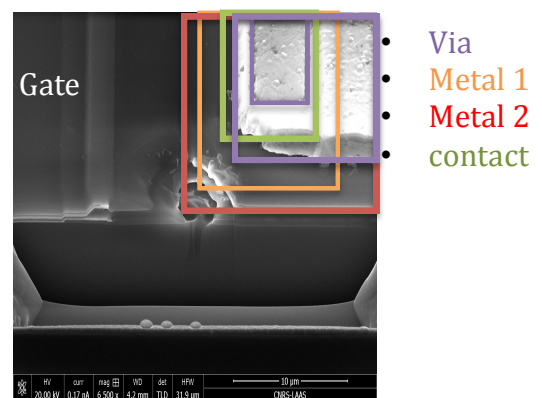


Figure 13: SEM photography after FIB operation on ESD broken MESFET.

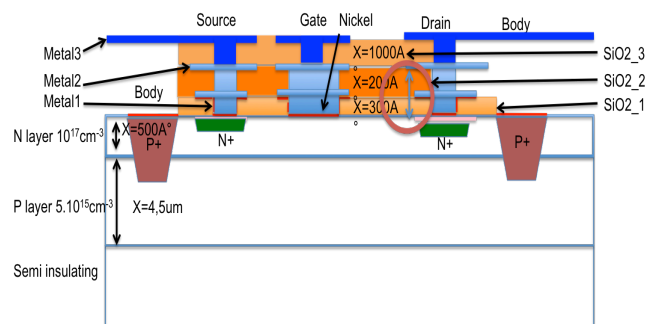


Figure 14: Reference MESFET device, oxide breakdown location

3.3.3 A parasitic NPN transistor

To understand the different results and defects observed for the protected device, we will first

analyze the role of the Zener diode in the protection system. The Zener PN junction near the Drain is reversed bias. When a sufficient potential is reached, The Zener diode is polarized on and a current is going through the P⁺ ring. Adding a Zener diode near the drain allows controlling the current discharge via the body.

With the Zener in reverse between the drain and body P⁺ diffusion, the overcurrent will be driven in the body and then through the forward biased source-substrate diode during an ESD. As the source is grounded, a potential difference is created between the P body and the N⁺. A parasitic NPN transistor will be biased with its base being the P layer and its collector being the drain region. A larger current can then be carried from the drain to the source and temperature will increase at the drain side until a damage occurs. The parasitic NPN has been triggered on as shown by TCAD simulated current density (Figure 15), impact ionization in the P layer (Base) and hole density cut below the source electrode (Emitter) (Figure 16), where holes become the main carriers in the N channel

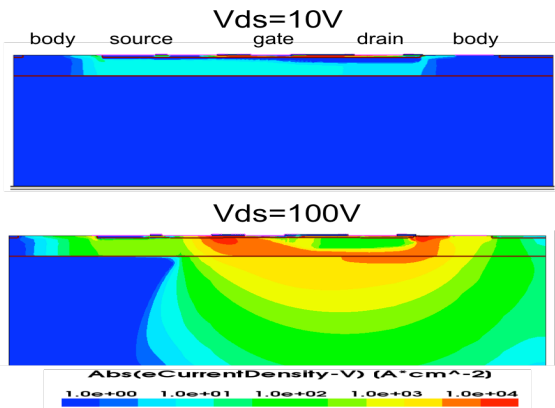


Figure 15: MZD Electron current density before (Top) and after (Bottom) avalanche

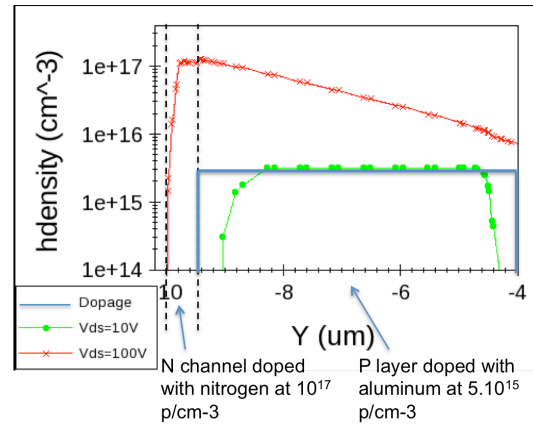


Figure 16: Hole density cut below the source electrode, demonstrate that the NPN parasitic transistor is triggered.

This structure corresponds to the same parasitic NPN than in the previous work [1].

4. Optimization of the ESD protection

A way to increase the maximum voltage capability and thus the ESD robustness would be to increase the thickness of the oxide layer or to find a more robust material, and more adapted for SiC (Figure 17).

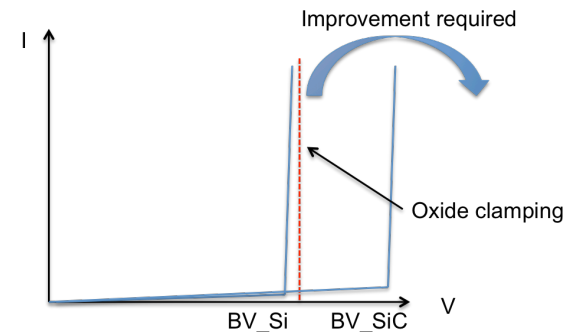


Figure 17: Necessities for SiC

The Zener on drain is an effective ESD protection for the MESFET that still can be optimized. First with a better homogenization of the electric field by adding a metallization layer over the P⁺ ring along the source electrode. Indeed it will ensure a better electrical repartition, which can delay the damage in the corner. Second by ensuring a large enough distance between the drain metals and the P⁺ ring.

Conclusion

An internal ESD protection has been tested for a

SiC MESFET. The reference and protected version presents two different failure mechanisms: the passivation layer failure and the parasitic NPN transistor triggering. Increasing the oxide layer thickness should improve the maximum voltage capability. New experiments have to be realized with new devices in order to verify the ESD robustness progress. In any case, improving the electrical potential homogeneity in the P⁺ along the source should lead to robustness improvement for the SiC MESFET. In summary, SiC device failure mechanism appears to be significantly different compared to silicon devices. Mainly for two reasons related to SiC material properties. First, its higher dielectric strength induce higher junctions breakdown which, as a consequence, tends to narrow the classical ESD design window by reducing or even inverting the triggering and oxides breakdown margin. This requires higher caution for metal-layers-layout design and/or working on the dielectrics strength. Second, as SiC a no liquid phase at atmospheric pressure and is thus sublimated when reaching too high temperatures, the observed defects are essentially different than the one observed in silicon. While melted and recrystallized regions are often observed as ESD related defect in silicon, material-hole defects are observed in silicon carbide as shown in this study.

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