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Energy-Aware Computing via Adaptive Precision under Performance Constraints in OFDM Wireless Receivers

Fernando Cladera

University of Rennes 1, IRISA, INRIA
fcladera@fcladera.com

Matthieu Gautier

University of Rennes 1, IRISA, INRIA
matthieu.gautier@inria.fr

Olivier Sentieys

INRIA, IRISA, University of Rennes 1
olivier.sentieys@irisa.fr

Abstract—To cope with rapid variations of channel parameters, wireless receivers are designed with a significant performance margin to reach a given Bit Error Rate (BER), even for the worst-case channel conditions. Indeed, one of the steps during the design phase is the choice of the architecture bit-width, and the smallest wordlength that ensures the correct behaviour of the receiver is usually chosen. In this paper, an adaptive precision OFDM receiver is proposed. Significant energy savings come from varying at run time processing bit-width, based on estimation of channel conditions, without compromising the BER constraints. To validate the energy savings, the energy consumption of basic operators has been obtained from real measurements for different bit-widths on a FPGA and a processor using soft SIMD. Results show that up to 63% of the dynamic energy consumption can be saved using this adaptive technique.

I. INTRODUCTION

Mobile wireless channels are characterized by time-varying multipath propagation, noise, and interference effects. To cope with these rapid variations of channel parameters, wireless receivers are designed with a significant performance margin to be able to reach a given quality of the link, even for the worst-case channel conditions. In particular, in the baseband processing, data and operator bit-widths are oversized to deal with these unfavorable conditions. Nevertheless, today's mobile wireless devices are often battery powered, hence the necessity of low energy consumption is a strong design constraint [1]. One of the keys for lowering the energy consumption is adaptive bit-width wireless receivers. Dynamic Precision Scaling (DPS) has been proposed in the literature [2][3] as an adaptive precision system for wireless receivers. In DPS systems, the influence of the bit-width under multiple channel conditions is analyzed in the design phase. During the execution, the wordlength is changed dynamically to fit the performance requirements. The use of variable precision reduces the energy consumption, compared to a receiver where the bit-width is constant. Indeed, in [2] the energy consumption of the digital baseband processing is decreased by 25% to 40% in a WCDMA receiver.

Orthogonal Frequency-Division Multiplexing (OFDM) is a widely used standard for modern wireless receivers (e.g. LTE, DVB, DAB, 802.11a/g/n). Prior literature [3][4][5][6] focused on the use of adaptive bit-width in OFDM receivers. In [4], intensive simulations have been used to optimize the Fast Fourier Transform (FFT), the most consuming block in an OFDM system. The potential of DPS applied to OFDM

receivers is shown, because up to 50% of the energy can be saved. However, in this work it is not specified how to switch between the fixed-point implementations during the execution. Indeed, a fixed-point implementation selector will decrease the announced energy savings. In [5], an adaptive wordlength OFDM receiver is developed without the need of an off-line simulation step. This method has the drawback of modifying the OFDM frame specified in the standards, because a search symbol is inserted in order to estimate the quality of the received signal. Some improvements are made in [6] with the addition of a Viterbi decoder. Yet, a high number of iterative operations is needed to find the correct wordlength, decreasing the amount of energy saved by the adaptive method. Another DPS approach has been presented in [3]. In this paper, analytical models have been used to determine the optimum size for each component of the FFT, reducing the time needed for intensive simulations. Nevertheless, only an Additive White Gaussian Noise (AWGN) channel is analyzed. As OFDM was designed to deal with multipath channels [7], the influence of non Gaussian channels must be considered. Our work in this paper is similar in concept with the recent work in inexact circuit design [8][9] or the philosophy of designing adequately-engineered systems [10]. However, in the case of adaptive precision it is possible to guarantee that the reduced accuracy respects a given performance constraint, based on the estimation of external conditions.

In this paper, a new channel-aware variable wordlength method is presented for wireless OFDM systems. Energy consumption is reduced by modifying at run time the receiver bit-width based on the estimation of the channel conditions, without compromising the Bit Error Rate (BER) constraints. First, the BER is determined for various Signal-to-Noise Ratio (SNR) levels, channel types, and processing wordlengths. A simulation approach is used: for each channel type and SNR, a receiver with a specific fixed-point architecture is simulated and the BER is measured. Then, the best fixed-point implementation for each channel condition is determined through an off-line optimization process. At run time, the DPS algorithm is used (Fig. 1): the channel condition is determined by combining low-complex yet efficient estimation algorithms generating the metric p , which allows the choice of the fixed-point data format $f_{fp}(p)$ that minimizes the energy consumption subject to a given BER performance constraint. To validate the energy savings, the energy consumption of basic operators processing random data has been obtained from

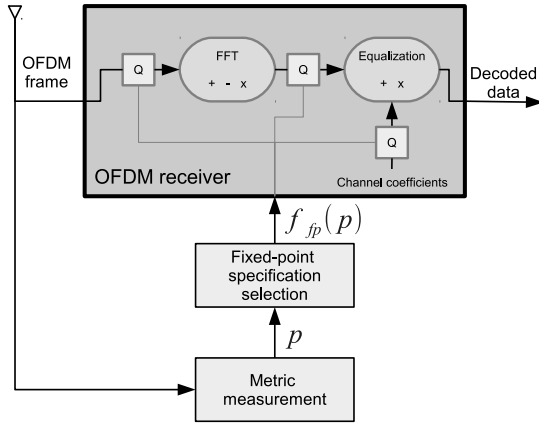


Fig. 1: DPS algorithm applied to an OFDM receiver.

real measurements. The energy spent by the operators depends on their bit-width. Two architectures have been considered: a Virtex-5 Field-Programmable Gate Array (FPGA) and an ARM processor using soft Single Instruction, Multiple Data (SIMD). Finally, the architecture consumption is estimated as a function of the number of operators and the wordlength.

To summarize, this paper studies an adaptive precision OFDM receiver, where a low complex selector is used to choose the processing wordlength at run time, estimating the energy savings with real measurements issued of experiments and taking into account not only AWGN, but also multipath channels.

This paper is organized as follows: Section II describes the OFDM system model used, as well as the energy reduction strategy. In Section III, the energy consumption estimation method is presented for both FPGAs and ARM processors. Section IV presents the fixed-point DPS receiver and the performance results are discussed in Section V. Finally, Section VI draws some conclusions.

II. OFDM SYSTEM MODEL

A. Floating-Point Receiver Model

In this study, an OFDM frame-based model has been defined using the following parameters: 512-point FFT (N_{FFT}) with 300 used subcarriers, 16-QAM modulation and 128-point Cyclic Prefix (N_{cyp})¹. Each frame is composed of at least ten OFDM symbols. The channel coefficients for the equalizer are known and the synchronization is presumed perfect. Introduced in Fig. 1, the system model is reduced to three important blocks: the FFT, the simple one-tap equalizer and the hard decision block². The blocks which execute intensive calculations during the operation, the FFT and the equalizer, will be optimized.

Two channel models are used: a simple AWGN channel and a Frequency Selective Fading (FSF) channel with AWGN. For both channels, the noise level varies from 0dB to 48dB, in steps

¹These parameters have been extracted from [11] to emulate a long Cyclic prefix LTE receiver working at 5 MHz.

²In Fig. 1 some quantizers have been added to simulate the fixed-point behaviour. Those quantizers are obviously not present in the floating-point model.

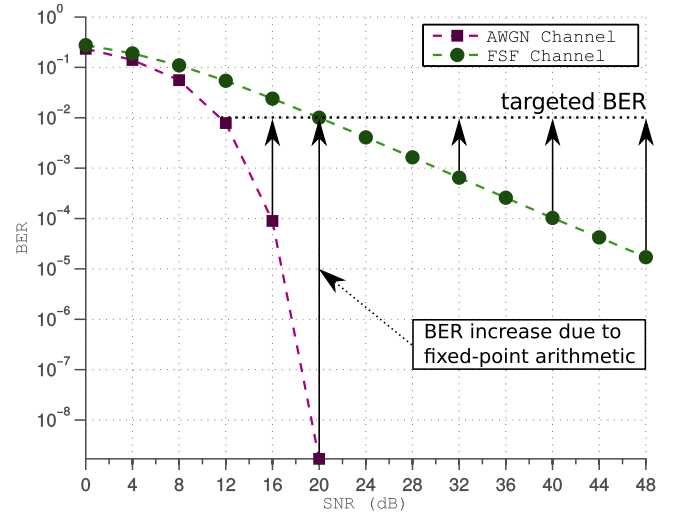


Fig. 2: Floating-point OFDM receiver performance showing the superlative quality for high SNR values and the energy saving strategy.

of 4 dB. The FSF channel has an exponential delay profile, with a length of $\approx 0.3 N_{cyp}$, 9 paths and 16 dB between the first and the last path. This channel is similar to the Extended Vehicular A Model from [12]. In order to reduce the number of simulations, only one FSF channel has been considered in this study.

B. Energy Saving Strategy

Wireless channels are usually designed to target a specific application (voice, video, data). Each application imposes specific parameters such as a required bandwidth, a maximum latency or a level of reliability. These parameters are related with the link quality, which is evaluated using metrics like the BER, the Packet Error Rate (PER), and the Error Vector Magnitude (EVM). Indeed, these metrics are linked [5]. In our work, the BER is used for measuring the link quality. A BER of 10^{-2} is targeted as the desired quality, independently of the channel condition. This BER is a standard value for voice applications [13]. However, the same procedure of optimization can be applied for different BER values (may be lower), to target another applications.

Fig. 2 shows the simulated BER performance of the receiver for the channels specified in Sec. II-A. Low values of SNR will not be optimized, because the BER constraint cannot be achieved. High values of SNR imply a superlative quality, for both channels. The use of reduced precision will degrade the quality of the link, up to the objective value. However, it will decrease the energy consumption.

III. ENERGY CONSUMPTION ESTIMATION

To evaluate the amount of energy spent by the receiver, a high level estimation step is carried out. The energy consumption of the receiver is calculated based on the number of operations. To this purpose, the energy consumption cost function $C(wl)$ of simple arithmetic operators (multipliers, adders) is obtained from experiments. $C(wl)$ links the amount of energy spent to do one operation depending on the bit-width wl of this operator. In addition, a maximum activity

| Operation | | wl | | | | | | | | | | | | |
|-----------|-------|------|------|------|------|------|------|------|------|------|------|------|------|--|
| | | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | |
| ADD | UInt | 1.55 | 1.57 | 1.58 | 1.60 | 1.61 | 1.63 | 1.64 | 1.66 | 1.67 | 1.69 | 1.70 | 1.72 | |
| | SIMD2 | 0.80 | 0.81 | 0.83 | 0.85 | 0.86 | 0.88 | 0.89 | 0.91 | 0.93 | 0.94 | 0.96 | 0.97 | |
| | SIMD3 | 0.55 | 0.56 | 0.58 | 0.60 | 0.61 | 0.63 | - | - | - | - | - | - | |
| MULT | UInt | 1.97 | 1.99 | 2.01 | 2.03 | 2.04 | 2.06 | 2.07 | 2.08 | 2.10 | 2.11 | 2.12 | 2.13 | |
| | SIMD2 | 0.98 | 0.99 | 1.01 | 1.04 | 1.07 | - | - | - | - | - | - | - | |

TABLE I: Energy consumed for simple arithmetic operations in an ARM7TDMI (in $[nJ]$).

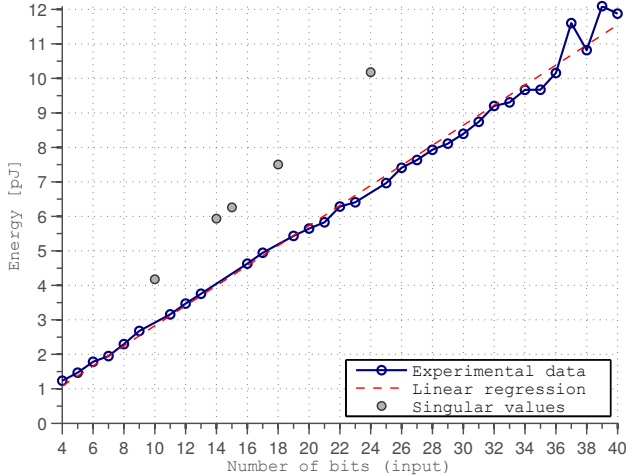


Fig. 3: Energy consumption of Virtex-5 adders with variable wordlengths.

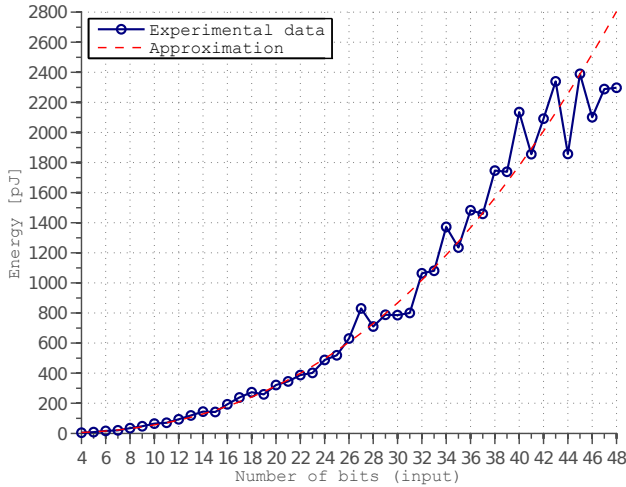


Fig. 4: Energy consumption of Virtex-5 LUT multipliers with variable wordlengths.

is considered by feeding the operators with random data. Even when this energy consumption computation is not highly accurate, these values can be used as a rough estimation of the gains achievable by our variable wordlength algorithm.

A. FPGAs

One of the targets chosen to estimate the $C(wl)$ was a Virtex-5 XC5VLX50T FPGA. Special architectures with a high number of operators were synthesized. Then, arithmetic operations were carried out using random data from a Pseudo-Random Binary Sequence (PRBS). The energy consumed by the operators can be measured using the technique described

in [14].

Only the dynamic energy consumption (related to the activity in the circuit) is considered. Also, only Look-Up Table (LUT) operators have been used. Fig. 3 and Fig. 4 show $C(wl)$ obtained for adders and LUT multipliers respectively.

B. ARM

An instruction-level energy estimation has been carried out for an ARM7TDMI processor (SAM7X256). Indeed, in order to estimate the dynamic energy consumed to do an operation (addition, multiplication), the energy to load a pair of values from the memory, calculate and store the result in memory has been measured. In addition, the energy when the NOP (No Operation) instruction is executed has also been measured. The NOP instruction does not imply an access to the data memory nor an arithmetic calculation. Thus, it can be used to estimate the static power consumption of the processor. Finally, both values are subtracted to obtain the dynamic energy consumption of the processor.

Single Instruction, Multiple Data (SIMD) architectures allow multiple parallel calculations per instruction. However, this processor is not capable of executing SIMD instructions natively. Thus, the soft-SIMD technique described in [15] was used to improve the parallelism in the processor. Table I summarizes the energy values obtained. SIMD2 implies that two operations are made simultaneously, whereas SIMD3 implies three simultaneous operations in a 32-bit word.

IV. FIXED-POINT DPS RECEIVER

A. Fixed-Point Receiver

After validating the floating-point model in Section II-A, quantizers have been introduced to simulate a fixed-point architecture, as shown by Fig. 1. The quantizers limit the dynamic and reduce the precision in the FFT input, the FFT output and the channel coefficients. Finding the appropriate fixed-point wordlength for each quantizer is a task composed of two steps: first, the dynamic range is found (the integer part in a fixed-point data). Secondly, the precision (the fractional part in a fixed-point data) has to be chosen.

The dynamic range can be easily obtained using a simulation approach: the floating point model is simulated for every channel type and SNR. The data in each block is stored and analyzed afterwards. The dynamic range that suits at least 99% of the values determines the number of bits in the integer part, for each channel condition.

Obtaining the fractional part implies a much more difficult work: for every channel type and SNR, multiple simulations have been executed using different fractional parts for each block. Each precision implies a BER, and the precision chosen is a tradeoff between quality of the link and the energy spent

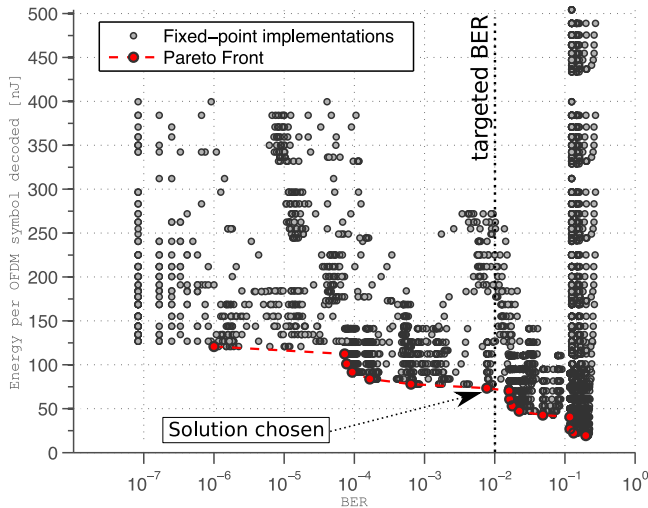


Fig. 5: Fixed-point implementation selection for an AGWN channel and a SNR of 24 dB, using $C(wl)$ of a Virtex-5 processor.

during the reception. Fig. 5 represents this method using the cost function of the Virtex-5 FPGA: the points represent different fixed-point implementations of the receiver, with an associated BER and energy consumption. The fixed-point implementation on the Pareto front closer to the objective BER is chosen. The cost of the solution is estimated using $C(wl)$ and knowing the number of operations needed to demodulate an OFDM symbol: 13×10^3 real additions and 9×10^3 real multiplications in the FFT, 600 real additions and 1200 real multiplications in the equalizer.

After choosing the fixed-point implementations for all the possible channel conditions, Fig. 6a is built using the cost function of the Virtex-5 FPGA, showing the energy consumption per OFDM symbol for each channel condition. As expected, there is an important difference depending on the channel type and SNR. The “worst-case” FPGA receiver will always use the largest wordlength, spending approximately 278 nJ per OFDM symbol, independently of the working conditions. Oppositely, in a DPS receiver the energy consumption can be reduced down to 71 nJ if better channel conditions are available. Therefore, up to 74% of the energy consumed can be saved, without taking into account the consumption of the implementation selector.

This analysis can be extended using the cost function of the ARM processor. The following hypotheses are made: the processor will run the most optimized SIMD mode available for a given bit-width, and the energy to bind multiple sub-word operands into a 32-bit word is not considered. Fig. 6b shows the energy consumption for each channel condition. The “worst-case” receiver consumes $30.2 \mu\text{J}$, whereas the dynamic receiver can reduce its energy consumption down to $18.7 \mu\text{J}$, saving 38% of the energy.

B. Fixed-Point Implementation Selector

The implementation selector is composed of two low complexity estimators with the aim to determine the SNR and the channel type. A 12-bit fixed-point architecture has

been implemented for both estimators³. In our receiver, the channel conditions are estimated for each OFDM symbol, and the system has no memory about previous channel conditions. Both estimators were optimized to target a detection error of 10^{-3} .

1) *SNR Estimation*: The Cyclic Prefix (CP) introduces some redundancy in the OFDM symbol, to prevent multipath channel effects. When the channel conditions are not too severe, this redundancy can be used to estimate the SNR [16]. This estimator is chosen due to its simplicity, good performance, and low energy consumption. The estimator is set to use the 64 last points of the 128 available in the CP. Thus, 513 real additions, 256 real multiplications and one division are needed. The energy consumption due to SNR estimation is 25.15 nJ per OFDM symbol in the FPGA and $1.03 \mu\text{J}$ in the ARM processor.

2) *Channel Type Estimation*: In an OFDM receiver, the equalizer coefficients are estimated dynamically during the reception using training symbols and reference signals. If the channel has only a single path, the equalizer coefficients are flat. But, if the channel presents multiple paths, the coefficients show peaks and depressions. Hence, the variance of the equalizer coefficients can be used as an indicator of the channel type. Only 32 points from the 300 available in the equalizer are used. With these parameters, 129 real additions, 64 real multiplications and 1 real division are needed. The energy consumption due to channel type detection is 6.84 nJ per OFDM symbol for the FPGA and $0.27 \mu\text{J}$ for the ARM. More points would allow a better channel detection, which is useful for distinguishing between multiple channel models. In our receiver, the equalizer coefficients are presumed known. However, to ensure a correct behavior of the channel estimator, the coefficients have been tuned with a Normalized Linear Mean Squares (NLMS) equalizer in a floating point receiver.

V. PERFORMANCE RESULTS

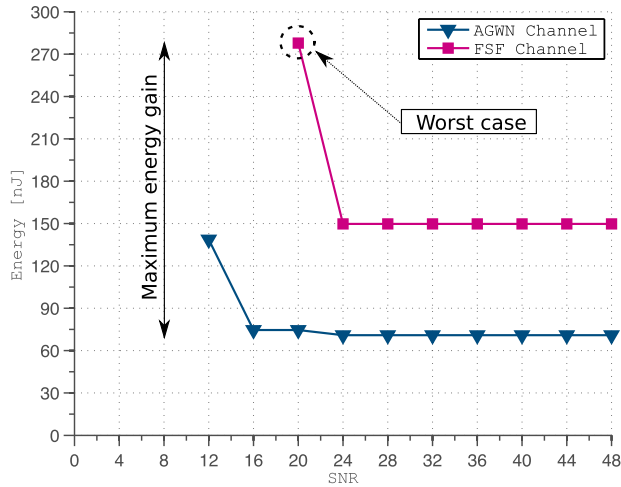
A. Implementation Selector Performance

As it was pointed out in Section IV-B, the number of points for both selectors was chosen targeting a detection error of 10^{-3} at 16 dB. During the simulations, the average detection error was approximately $10^{-2.5}$ for the AWGN channel and $10^{-1.9}$ for the FSF channel proposed in Section II-A. This may be seen as a drawback because more than 1% of the frames are decoded with a wrong fixed-point implementation in the FSF channel. A deeper analysis shows that most of the errors for the AWGN channel are due to erroneous SNR detection. In contrast, for the FSF channel, the errors are due to both the channel ($10^{-2.1}$) and the SNR ($10^{-2.2}$) detection. Nonetheless, an erroneous detection does not imply necessarily a reduction in the BER: if a fixed-point implementation with a larger wordlength is chosen instead of the right one, the energy consumption will be increased but the quality constraint will be reached.

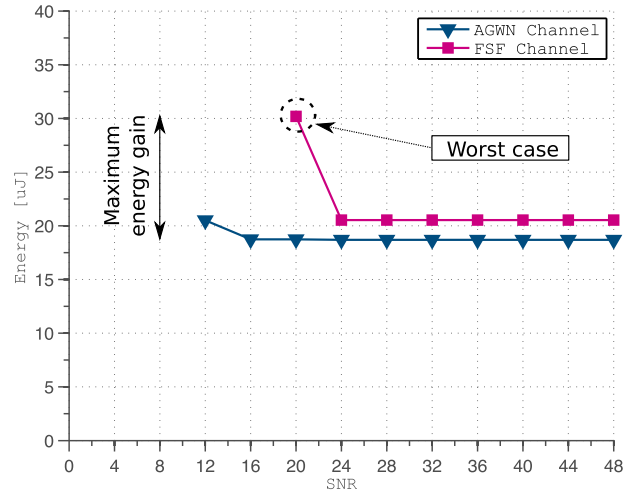
B. Global System Performance

The DPS system is built, linking the fixed-point OFDM receiver with the implementation selector. Simulations have

³A wordlength analysis has been carried out for the implementation selector, obtaining the best tradeoff with 12 bits.



(a) Virtex-5 FPGA.



(b) ARM processor.

Fig. 6: Energy consumption per OFDM symbol for AGWN and FSF channels, depending on SNR values.

been run in time-varying channels to evaluate the global system performance. Fig. 7 shows the BER-SNR curve for the dynamic receiver (full line) compared with the “worst-case” receiver (dotted line). The system operates correctly: when the BER increases beyond 10^{-2} , the precision is reduced and the system follows the targeted constraint. In order to evaluate the energy savings, the global energy consumption is calculated by

$$E_{total} = E_{receiver} + E_{selector}, \quad (1)$$

where $E_{receiver}$ are the values found after optimization in Section IV-A and $E_{selector}$ corresponds to the constant energy consumption of the selector, 32 nJ for the FPGA and $1.3 \mu\text{J}$ for the ARM. Hence, the performance of our system can be calculated easily: in the worst condition, the FPGA receiver uses the largest wordlength and, due to the energy needed by the selector, the consumption is 111% compared to the “worst-case” receiver. Moreover, in the best case (high SNR and AWGN channel), the consumption of the receiver is only 37% of the total consumption (63% of the energy saved). The ARM receiver uses 104% of the energy in the worst condition and 66% in the best one (34% of the energy saved).

Fig. 8 shows the real energy consumption of the receiver for the FPGA, compared with the “worst-case” solution. It also shows the accuracy of the implementation selector. For each channel condition 1000 simulations have been carried out. A receiver with a perfect selector would follow the dotted line, whereas the results of our receiver are shown using dots (correct channel condition estimation) and triangles (bad channel condition estimation). It can be seen in Fig.8a that for the AWGN channel, those errors are generally due to a wrong SNR estimation. In Fig. 8b, for the FSF channel, wrong estimations are due to erroneous channel and SNR estimations. However, the system performance is guaranteed as shown by Fig. 7.

C. Discussion and Further Work

Our system proves a correct behavior, reducing the energy consumed during the execution. A low-power yet efficient

selector is presented and tested in a fixed-point receiver. Compared with [4], our work uses a similar technique to find the correct fixed-point implementations, reaching similar energy reductions (50%). However, a selector to choose the right implementation is described in our work. In [5], modifications are introduced in the OFDM frame to save up to 30.2% of the energy. In [6], multiple calculations are needed to estimate the channel conditions, reducing the amount of energy saved (23.9%). Our savings are higher without modifying the OFDM frame. [3] proposes using the DPS offline optimization method too. Still, the channel type is not considered into the optimization, obtaining an average saving of 17%. The importance of analyzing multiple channel conditions, not only the SNR but also the channel type, is demonstrated in this work. Thus, our energy reductions are higher compared to state-of-the-art proposals.

In our system, the number of quantizers is reduced because of the simulation time needed. To solve this problem, analytic methods such as those proposed in [3] may be used

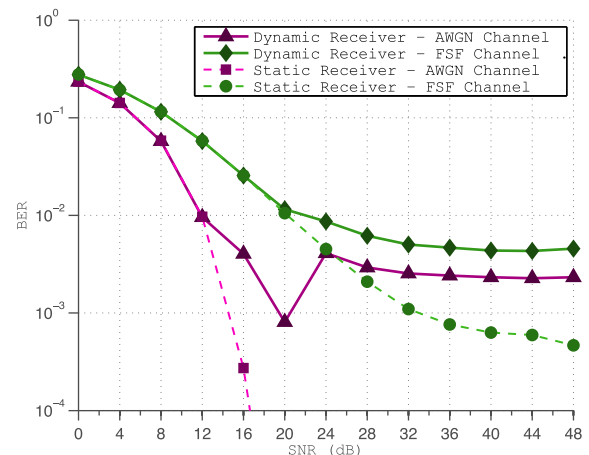
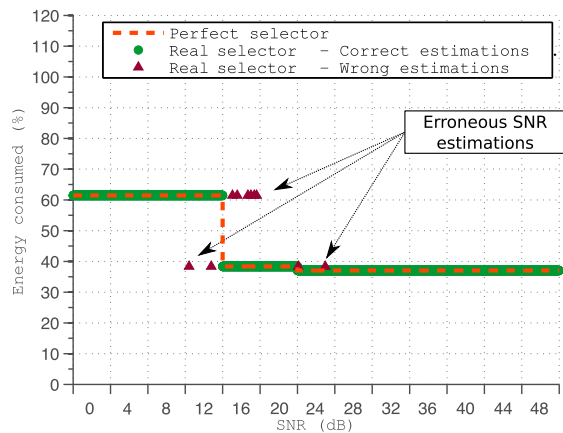
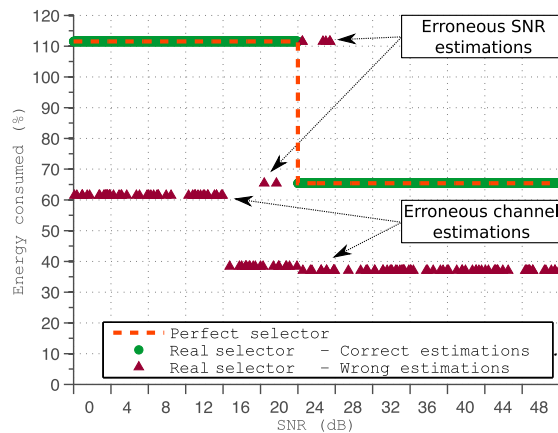


Fig. 7: Correct performance of the dynamic system, following the BER target.



(a) AGWN channel (FPGA cost function).



(b) FSF channel (FPGA cost function).

Fig. 8: Energy consumption in a DPS receiver compared to the “worst-case” static fixed-point implementation.

to determine the correct fixed-point implementation for each channel condition. The influence of omitted blocks, such as the channel coefficients estimation and the synchronization should be considered too.

Finally, our energy estimation only considers arithmetic operators. Other components, such as memories, should be considered, but their energy consumption will also be improved by our adaptive precision approach. Other parameters, such as the energy needed for the reconfiguration of the architecture, have to be measured in a real DPS OFDM receiver in order to ensure that the energy savings are still high to justify this approach.

VI. CONCLUSIONS

This work demonstrates a DPS OFDM receiver that can switch its fixed-point specification depending not only on the noise level but also on the channel type. After presenting an OFDM receiver with its corresponding parameters, a floating to fixed-point conversion process has been carried out. The influence of the channel type and SNR in the energy consumption was shown. A low-power implementation selector was built using two estimators of the channel type and noise level. The whole system was assembled and successfully tested. Compared to related work the energy savings were higher due to the use of a channel-aware DPS receiver. In addition, no modifications to existing standards nor intensive calculations are needed to select the fixed-point implementation. Estimations using FPGA show that up to 63% of the energy can be saved using this technique. Using an ARM7 processor, an energy saving of 34% is achieved. An ASIC implementation would probably take even more advantage of the energy savings offered by the proposed adaptive precision technique.

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