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## Multijunction photovoltaics: integrating III–V semiconductor heterostructures on silicon

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**Summary :** Gallium arsenide phosphide nitride shows promise for developing highefficiency tandem solar cells on low-cost silicon substrates..

To date, the highest efficiency conversions have been reached by using III–V (that is, compounds of elements from groups III and V of the periodic table) monocrystalline multijunction solar cells (MJSCs) under concentrated sunlight. Soitec and the Fraunhofer Institute have pushed the solar cell record to 44.7% for terrestrial applications.<sup>1</sup>

They achieved this record with a wafer-bonded fourjunction gallium indium phosphide / gallium arsenide // gallium indium arsenide phosphide / gallium indium arsenide (GaInP/GaAs//GaInAsP/GaInAs) solar cell under concentration of 297 suns (that is, light 297 times as bright as sunlight). Soitec and Fraunhofer also announced on the Soitec website very recently the achievement of 46% efficiency under concentration of 508 suns. Moreover, Solar Junction has demonstrated a III–V triple junction coherently grown (lattice-matched) onto a gallium arsenide (GaAs) substrate with 44% efficiency under 942 suns (AM1.5D spectra, representing the direct-radiation— that is, without the diffuse radiation and albedo—annually averaged solar spectrum at ground level at mid-latitudes).<sup>2</sup> It contains a highly sought-after 1eV gallium indium arsenide nitride antimonide (GaInAsNSb) diluted-nitride compound. However, maintaining the GaAs or germanium substrates to build these high-efficiency III–V solar cells is costly.

With the strategic challenge cost of €0.25–0.5 per watt of peak power in mind, we have investigated using silicon, which is the most abundant element on earth and inexpensive. Indeed, true monolithic integration of III–V compound semiconductor heterostructures with silicon would enable both highly efficient and low-cost PV production and is the subject of great research interest.

A tandem solar cell, made of a 1.7eV III–V top and a 1.1eV crystalline silicon (c-Si) bottom cell, would theoretically reach an efficiency of 37%, under AM1.5G illumination (that is, the global incident solar radiation, including the direct, diffuse, and albedo radiation).<sup>3</sup> However, MJSC efficiency is very sensitive to structural defects, such as misfit dislocations, which appear during metamorphic growth; they dramatically reduce the carrier lifetime and thus current extraction and solar cell performance. A perfect lattice-matched epitaxial PV structure of III–V and silicon technologies on silicon substrate would significantly increase efficiency, as well as reducing the overall cost of multijunction PV cells.

We have developed promising building blocks for GaAsPN/silicon-based dual-junction solar cells. The tandem GaAsPN/silicon double-junction solar cell will be electrically connected with a tunnel junction (TJ), which connects successive p-n junctions made up of a p-type semiconductor and an n-type semiconductor. One of the main issues in developing the dual-junction solar cell is obtaining an efficient TJ. We have modeled this and found high theoretical current densities for both GaP/silicon and silicon/silicon TJs with experimentally attained GaP alloy doping levels and considering an n-doped silicon bottom absorber.<sup>4</sup> Modeling the top-PIN-junction GaAsPN absorber with a ‘tight-binding’ calculation crossed with critical thickness modeling showed that a GaAsPN alloy (composition 9% arsenide and 4% nitride) is promising with an expected bandgap energy of 1.81eV and a critical thickness that allows pseudomorphic growth of a 1μm-thick absorber.<sup>5</sup> To assess this material independently of defects potentially generated at the GaP/silicon interface, we grew a lattice-matched 100nm-thick GaAsPN alloy on the 001 face of a gallium phosphide (GaP) substrate. After a post-growth annealing step, this alloy displays strong absorption around 1.8–1.9eV, and efficient photoluminescence at room temperature suitable for targeted solar cell top junction development.

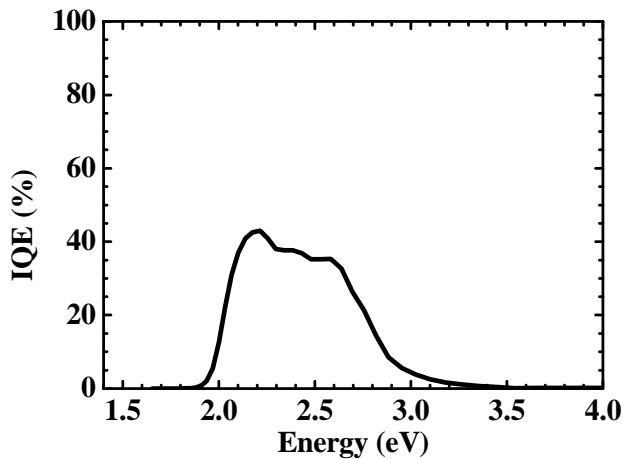
Finally, we have developed early stage GaP/GaAsPN/GaP PIN (that is, made up of layers of p-type, intrinsic, and n-type semiconductors) solar cell prototypes by molecular beam epitaxy (MBE) on a (001)-

oriented GaP substrate, which is easier than growth directly on a silicon (001) substrate.<sup>6</sup> Next, we will do the same on a GaP/silicon pseudo-substrate—a silicon substrate with a thin (45nm) GaP layer on top—and then on a silicon solar cell with a GaP layer on top). The difficult part is growing a defect-free GaP crystalline layer on top of the silicon substrate. Indeed, the first GaP layer of the PIN junction will be the GaP layer of the GaP/Si pseudo-substrate in the case of a silicon/ silicon TJ, or will be part of the TJ in case of an hybrid GaP/silicon TJ.

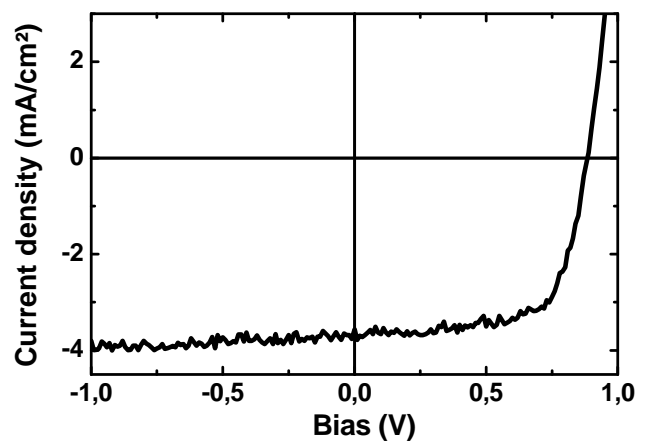
The internal quantum efficiency of around 40% shows that carriers have been successfully extracted from a 1 $\mu$ m-thick GaAsPN alloy absorber (see Figure 1). Current-voltage measurements performed on this sample show a remarkable record open-circuit voltage of 1.18V. Our best-performing cell contained a 300nm-thick absorber with 2.25% efficiency under AM1.5G illumination (see Figure 2). This cell exhibits a remarkable fill factor (the ratio of the maximum obtainable power and the product of the open-circuit voltage and short-circuit current) of 71%.<sup>7</sup> The short-circuit current is 3.77mA/cm<sup>2</sup> but the open-circuit voltage is relatively low at 0.89V. Assuming that a 1 $\mu$ m thick GaAsPN layer is necessary to absorb the main part of the solar spectrum and, considering the absence of any anti-reflective coating, the sample with a thinner (300nm) absorber displays a short-circuit current density close to its theoretical maximum at 1 sun of roughly 5mA/cm<sup>2</sup>. The theoretical maximum takes into account the small absorber thickness and assumes perfect carrier collection, but in practice some carriers are lost inside the absorber. That carrier extraction is better from the thinner than the thicker absorber may be attributed to a small carrier diffusion length, which is less than the thickness of the thicker absorber.

In summary, we have developed promising building blocks for GaAsPN/silicon-based dual-junction solar cells. Concerning the top subcell development, we have obtained an efficient absorber by growing a lattice-matched GaAsPN alloy on a GaP substrate. We next grew early-stage GaP/GaAsPN/GaP PIN solar cell prototypes by MBE on GaP substrates. We are now working to grow a defect-free GaP crystalline layer on a silicon substrate. These results are promising and validate our approach for elaborating a lattice-matched dual junction solar cell on silicon substrate. We are now developing the tunnel junction and the overall tandem cell with a purpose-designed bottom silicon subcell. A clear pathway to higher efficiency of the top GaAsPN cell would require thorough optimization of both the MBE growth and the post-growth annealing steps accompanied by improvements in PIN junction architecture similar to the development of the GaInAsN 1eV subcell on GaAs substrates.<sup>2</sup>

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**Fig1.** Internal quantum efficiency of a PIN junction made up of a p-doped gallium phosphide (GaP) on top of a 1 $\mu$ m-thick layer of an intrinsic gallium arsenide phosphide nitride (GaAsPN) absorber on top of an n-doped GaP layer, grown on a (001)-oriented GaP substrate, where (001) represents a particular crystal plane



**Fig2.** Current-voltage measurements under AM1.5G solar spectrum, of a GaP/GaAsPN 300nm/GaP PIN junction grown on a (001)-oriented GaP substrate

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