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► **To cite this version:**

Jérôme Tissier. MMIC/RFIC for receivers front-end. SAME 2006, Oct 2006, Sophia-Antipolis, France.
hal-01130373

HAL Id: hal-01130373

<https://hal.science/hal-01130373v1>

Submitted on 11 Mar 2015

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SAME 2006 Forum

Session : Mixed Signal, RF, Communication.

MMIC/RFIC for receivers front-end

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Abstract:

This paper deals with the work, realized in the Electronics and Physics Department of ESEO (Graduate school of engineering in Electronics, Computer sciences, Telecommunication and Networks) in the area of MMIC and RFIC circuits for wireless applications. To be more precise, a mixer, a filtering amplifier and Low Noise Amplifiers (LNA) will be presented in this article in GaAs and SiGe technologies.

Table of Contents of the paper

- I. INTRODUCTION
- II. DUAL-GATE MIXER
 - 1. *Circuit topology and layout*
 - 2. *Simulation and measurement results*
- III. FILTERING AMPLIFIER
 - 1. *Circuit topology and layout*
 - 2. *Simulation and measurement results*
- IV. WIDE BAND LOW NOISE AMPLIFIERS (LNA)
 - 1. *Wide band SiGe LNA for 2.45 GHz and 5.8 GHz ISM bands*
 - 2. *Ultra Wide band GaAs LNA*
- V. CONCLUSION

I. INTRODUCTION

Nowadays, the frontier between analog processing and digital processing is moving close to the antenna. However, as the RF signal from the antenna cannot be directly digitally processed, Low Noise Amplifiers (LNA), Power Amplifiers (PA) and, to a lesser extent, mixers remain essential components of receivers or transmitters front-end.

The Microwave Monolithic Integrated Circuits (MMIC) design is a recent research axis developed at ESEO (for about three years). At the beginning, two simple circuits, a mixer and a filtering amplifier, operating both at 5.8 GHz, have been realized, in a 0.2 μm GaAs process from OMMIC (EDO2AH). For each circuit, a compromise has been done between simplicity and performances in order to obtain compactness (circuits have to be implemented on the smallest chip size available with this process, that is to say 1.5*1mm²), easily to implement and easily to test structures with sufficient characteristics for an integration in a receiver front-end.

The use of the GaAs OMMIC process EDO2AH was justified by the fact that it is a well known process for microwave frequencies, with a complete library (including spiral inductors) and which is available for academic institutes by way of the CMP (Multi-Projects Circuits) in Grenoble. But, for our frequency band (centred at 5.8 GHz), a simple SiGe BiCMOS process could be used. The use of a SiGe process leads to compactness structures, compatible with a CMOS process, with results as good as those obtained with a GaAs process (except for linearity). The drawback of this kind of technology is that the library is not so complete than the GaAs one, specially concerning spiral inductors, which can cause some problems at microwave frequencies.

Nowadays, our field of interest is the Low Noise Amplification. Two circuits are in development. The first one, use a 0.35 μm SiGe BiCMOS process from AMS (available by way of the CMP) for the reasons explained above. It is a wide band LNA which have to operate in the two ISM bands, centred at 2.45 GHz and 5.8 GHz

The second one is an ultra wide band LNA designed to be used for UWB or Wimax applications for example. The process used to design this Low Noise Amplifier is the GaAs OMMIC process ED02AH.

II. DUAL-GATE MIXER

II-1. Circuit topology and layout

A double balanced mixer is frequently used in communication systems [1] [2]. Balanced mixers generally have better power-handling capabilities, and higher isolation characteristic between ports than unbalanced mixers. In addition, certain spurious responses, LO noise, and spurious signals can be rejected by balanced mixer scheme. Their disadvantages are the need for greater LO power to drive many nonlinear devices and the complicated structure due to the external devices, such as balun and many devices. Thus, it is often practical to use a single device dual-gate FET mixer in applications where a balanced mixer would otherwise be needed [3] [4]. Although characteristics of this kind of mixer are not so good as balanced mixer's ones, the possibility of applying LO and RF to separated gates without the use of baluns makes dual-gate FET mixer easy to implement in MMIC technology with sufficient performances for an integration in a receiver front-end. That is why our mixer is based on a simple dual-gate P-HEMT mixer matched simultaneously at its three ports, as shown in figure 1.

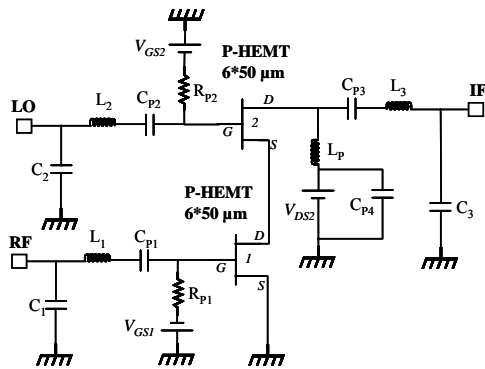


Figure 1 : Dual-gate mixer circuit topology

This dual-gate mixer has been implemented on a chip of 1.5x1mm², using the 0.2 μm GaAs process (ED02AH) from OMMIC. The layout of the circuit is shown in figure 2.

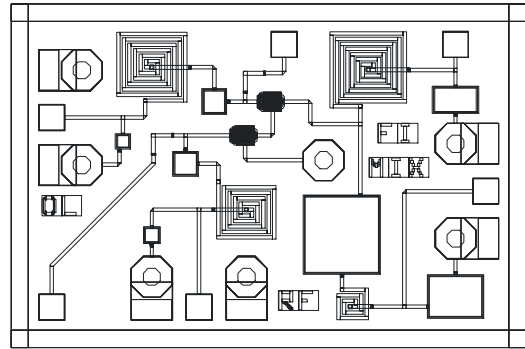


Figure 2 : Dual-gate mixer layout

II-2 Simulated and measured results

All the results are summarized in table 1.

Parameters	Unit	Simulated results	Measured results
		$f_{RF} = 5.8$ GHz $f_{LO} = 5.2$ GHz $P_{LO} = 4$ dBm $P_{RF} = -30$ dBm	$f_{RF} = 5.8$ GHz $f_{LO} = 5.4$ GHz $P_{LO} = 4$ dBm $P_{RF} = -30$ dBm
Conversion gain	dB	1.7	1.7
LO-IF Isolation	dB	31	24
RF-IF Isolation	dB	20	19
LO-RF Isolation	dB	12	-
Input P_{-1dB} Compression	dBm	-8.5	-
Output P_{-1dB} Compression	dBm	-7.7	-
Input IP3	dBm	3	-
N_{FSSB}	dB	16	-
DC power	mW	<10	<10

Table 1. Simulated and measured results of the dual-gate mixer

This dual-gate mixer is a down-converter mixer, operating at a 5.8 GHz RF frequency (ISM band). It has been designed to achieve gain conversion at an intermediate frequency of about 600 MHz, good LO-IF, RF-IF and LO-RF isolations (≥ 20 dB), good linearity and low power consumption (< 10 mW). An example of simulated results obtained for an intermediate frequency of 600 MHz is presented on table 1. All the results are closed to those expected, except for LO-RF isolation which is not very high (risk of DC offset) and for the noise figure which is not very good. All these results have been confirmed in measure. Because of the bad LO-RF isolation and a drift in the EDO2AH process, the results obtained for a f_{IF}

of 600 MHz in simulation are obtained for a f_{IF} of 400 MHz in measurement.

To improve these characteristics we have decided to combine filtering and low noise amplification in a filtering amplifier.

III. FILTERING AMPLIFIER

III-1. Circuit topology and layout

Unlike LNA, the filtering function does not have its monolithic version yet. That is why we have decided to implement on a same chip low noise amplification and filtering functions. This filtering amplifier, based on a single P-HEMT transistor cascaded with input/output matching and filtering networks was designed to achieve 10 dB gain at 5.8 GHz, good input/output matching, very good linearity, a noise figure of 4 dB at 5.8 GHz and a -3dB bandwidth of about 1GHz (our filter is not selective enough but for sensitive problems we have decided not to optimize this parameter).

The topology used is presented in figure 3.

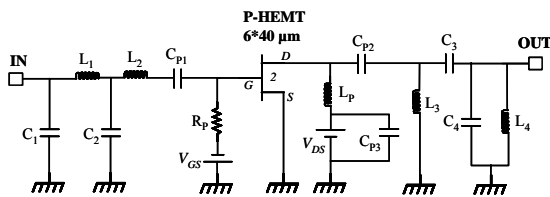


Figure 3 : Filtering amplifier circuit topology

This filtering amplifier is implemented using the same monolithic technology as in the second part. The chip size is always 1.5x1 mm². A photograph of the circuit is shown in figure 4.

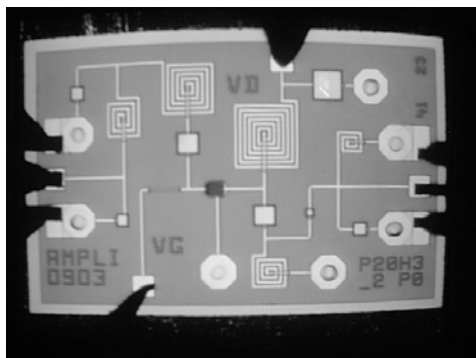


Figure 4 : Photograph of the filtering amplifier

III-2. Simulated and measured results

As for the first circuit, simulation results have been confirmed by measurements thanks to our microwave probe station. Good agreement between simulated and measured results has been obtained, as shown on figure 5.

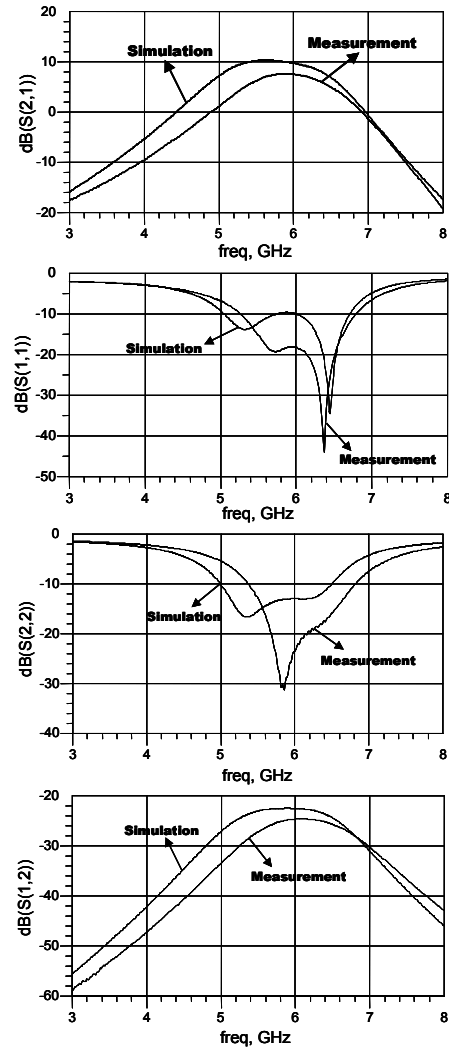


Figure 5 : S parameters simulated and measured

Except the gain max which has a little bit decreased (8 dB measured, certainly due to a drift of the EDO2AH process), all the S parameters measured are equivalent to those simulated. Concerning input matching (S_{11}), output matching (S_{22}) and isolation (S_{12}), measurement is even better than simulation.

The -1 dB compression point occurs for an input power of about 5 dBm, which denote a good linearity behaviour.

Concerning noise figure at central frequency (5.8 GHz), it is equal to the minimum noise figure of 4 dB which is quite low.

IV. WIDE BAND LOW NOISE AMPLIFIERS (LNA)

IV-1. Wide band SiGe LNA for 2.45 GHz and 5.8 GHz ISM bands

IV-1-1. Circuit topology and layout

The transistor used is a bipolar transistor from the AMS 0.35 μm SiGe process. To achieve high gain, 30 unit transistors have been wired in parallel. The advantage of this technique is to increase gain without increasing the noise figure (minimum noise figure of n wired in parallel two-ports networks is equal to the minimum noise figure of this two-ports network) [5]. As explained in [5], a high load impedance can improve input impedance Z_c in order to obtain a good power matching. This high load impedance can be realized by a simple capacitor. We need then a second stage to achieve output matching. The topology obtained is presented in figure 6.

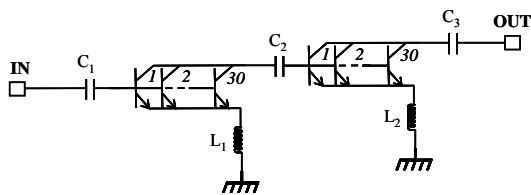


Figure 6 : SiGe LNA circuit topology

L_1 and L_2 are small inductors used to improve stability and matching. They will be replaced by transmission lines in the layout.

In this figure, biasing elements do not appear. This biasing has been realized thanks to five PMOS transistors. Four of them, act as current mirrors to generate the base current and to bias the fifth, which have to supply the collector current wanted.

A layout of the circuit is presented in figure 7.

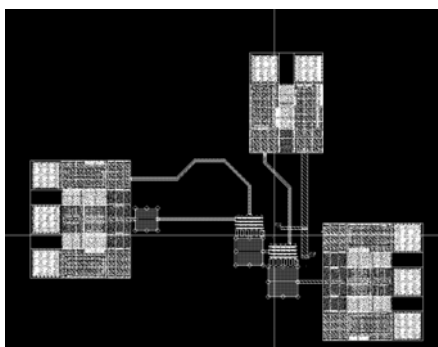


Figure 7 : SiGe LNA layout

IV-1-2. Simulated results

The simulated gain and the noise figure are plotted on figure 8. The input and output matching are plotted on figure 9.

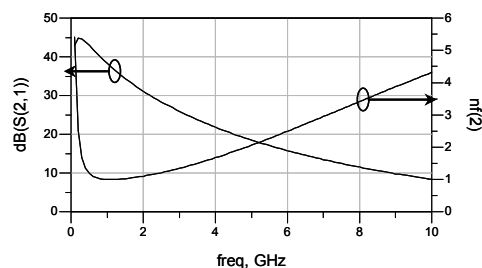


Figure 8 : SiGe LNA simulated gain and simulated noise figure



Figure 9 : SiGe LNA input and output matching

We can achieve a gain of 28 dB and 16 dB at respectively 2.45 GHz and 5.8 GHz. The noise figure obtained at 2.45 GHz and 5.8 GHz is very low (1.2 dB and 2.4 dB) and the matching parameters (S_{11} and S_{22}) are ≤ -10 dB over all frequency band.

IV-2. Ultra wide band GaAs LNA

IV-2-1. Circuit topology and layout

The topology, presented in figure 10, is a two stages amplifier (to achieve about 20 dB amplification on the 2-11 GHz band) with shunt feedback on each stage to obtain broadband matching and good noise figure [6].

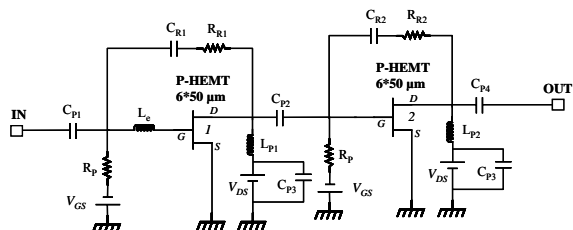


Figure 10 : Ultra wide band LNA topology

This dual-gate mixer has been implemented on a chip of $1.5 \times 1 \text{ mm}^2$, using again the $0.2 \text{ }\mu\text{m}$ GaAs ED02AH process. The layout of the circuit is shown in figure 11.

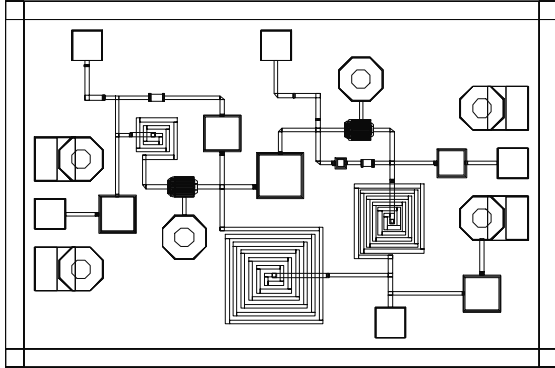


Figure 11 : Ultra wide band LNA layout

IV-2-2. Simulated results

The simulated gain is plotted on figure 12. The input and output matching are plotted on figure 13. The noise figure is plotted on figure 14.

In the 2-11 GHz band we obtain a gain contained between 23.4 dB (at 2GHz) and 19.1 dB (at 11GHz). The noise figure is very low and below 2.3 dB over the all band (2.3 dB at 2 GHz and 1.8 dB at 11GHz), the input matching is good ($S_{11} \leq -10 \text{ dB}$) and the output matching very good ($S_{22} \leq -14 \text{ dB}$). This LNA will be again implemented on the smallest chip size available with the ED02AH process ($1.5 \times 1 \text{ mm}^2$). This LNA will be sent to foundry soon.



Figure 12 : Ultra wide band LNA simulated gain

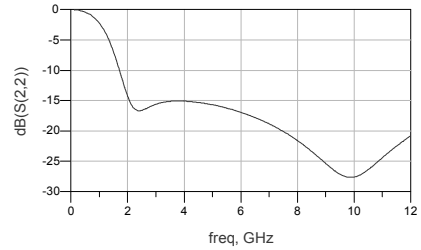
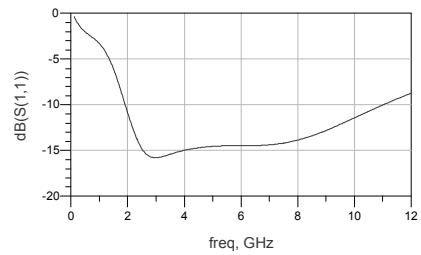


Figure 13: Ultra wide band LNA input and output matching

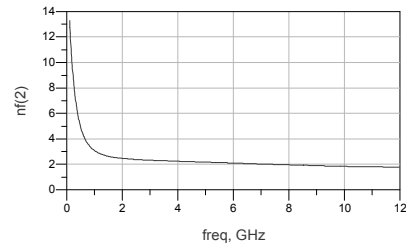


Figure 14 : Ultra wide band LNA simulated noise figure

V. CONCLUSION

In this article, work realized at ESEO, in the MMIC/RFIC design area is presented. The first circuit developed is a dual-gate mixer with each port matched on the chip. Good characteristics have been achieved according to the topology chosen, except for the RF-LO isolation and the noise figure. To improve this, a simple filtering amplifier based upon a classical matching technique has been designed, manufactured and tested, with excellent agreement between simulation and measurement. At present, our field of interest is the Low Noise Amplification. Two circuits are in development, using two different technologies. One uses the same GaAs P-HEMT technology as for the dual-gate mixer and filtering amplifier. This technology is particularly interesting for having high gain and very low noise in a very large microwave bandwidth, with good linearity. That is why the circuit

developed with this technology is an ultra wide band (2-11 GHz) LNA for Wimax or UWB applications. The second technology used is a common 0.35 μm SiGe BiCMOS process from AMS. It is used to design a wide band LNA, which have to operate in the two ISM bands, centred at 2.45 GHz and 5.8 GHz. because the emitter width is not small enough to allow sufficient gain at higher frequencies. However, the design of an ultra wide band LNA with an appropriate SiGe process is possible and has still been published [7]. In fact, nowadays, high frequencies SiGe processes are joining two different domains, the microelectronic domain and the microwave domain to design more and more complicated and integrated chips.

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About the Authors



Jérôme TISSIER was born in Limoges, France, in October 1973. He received the PhD degree from the University of Limoges in 2001. During his PhD, at the Microwave and Optical Communications Research Institute of Limoges (IRCOM) he has worked on active inductors, negative resistances and active filters in MMIC technology. Since 2002, he is an Associate Professor at ESEO (Graduate school of engineering in Electronics, Computer sciences, Telecommunication and Networks), Angers, in the Electronics and Physics Department. His main field of interest is MMICs and more specially mixers and Low Noise Amplifiers for receivers front-end.