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Polysilicon nanowires FET as highly-sensitive pH-sensor:

modeling and measurements

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Abstract

Silicon nanowires have several advantages, such as small size comparable to the size of molecules and high surface to volume ratio. Polycrystalline silicon nanowire based field effect transistors (poly-SiNW FETs) are used as ultrasensitive electronic sensors for pH detection. They are fabricated using a top down approach with simple and low cost fabrication process. Modeling of Metal-Insulator-polysilicon Nanowires (MINW) structure capacitor is performed to estimate the distribution of carrier concentration in the channel. Simulations highlight the effect of positive and negative charges at nanowire–electrolyte interface. Experimental characteristics according to different pH are presented, showing high sensitivity and correlate the modeling.

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1. Introduction

Owing to their high surface to volume ratio, silicon nanowires are currently attracting much attention as promising components for future nanoelectronic devices. Nanowire field effect transistors have emerged as good candidates for ultra-sensitive electrical detection of chemical or biological species, and, in particular, for pH sensing. Indeed, electrical characteristics and, also, sensitivity of SiNW-based sensors are substantially influenced by the surface to volume ratio, taking into account that surface charge effects.

In this paper, we present technological development of SiNW-based sensors is a fully CMOS compatible process. To understand the response mechanisms, we describe in this work a numerical modeling of the Metal-Insulator-

Silicon Nanowires (MINW) capacitor, which represents the basic structure of the NWFET. Modeling is performed to highlight the effect of positive and negative charges at nanowire–electrolyte interface on the carrier concentration in the channel. The insulator exposed with electrolyte reacts by developing interfacial charges layers. The actual amount of charges depends on the concentration of specific ions present in the solution, in particular on the H^+ ionic concentration, i.e. on the pH of the solution that modulates consequently the surface charge at the insulator/semiconducting interface. This implies a shift of the threshold voltage of the device. Finally, experimental characteristics according to different pH are presented.

2. Devices fabrication

Nanowires are synthesized using the sidewall spacer formation technique [1-2] to achieve 100 nm SiNWs (fig.1a). A 100nm thick highly *in-situ* doped polysilicon layer is deposited on insulated substrate and patterned to form step-gate. A 80nm thick APCVD oxide is deposited and acts as gate insulator. Then, two layers of polysilicon layers are successively deposited. The first one is an undoped and the second one is a highly *in-situ* N-type doped. Accurate control of the undoped polysilicon layer etching rate leads to the formation of nanometric size sidewall spacers used as undoped nanowires (fig. 1-b). Source and drain regions are made of heavily *in-situ* N-type doped polysilicon. Then, the polysilicon nanowires are capped with a 70nm thick APCVD oxide. Finally, an aluminum layer is deposited by thermal evaporation and patterned to define gate, source and drain electrodes (Fig. 1-c). Silicon nanowires based devices with 2 to 16 parallel nanowires-channels, 100nm width and 3 to 20µm lengths are fabricated.



Figure 1 (a) Fabrication of polysilicon NWs by the sidewall spacer formation technique, (b) SEM image of a nanowire synthesized using step made of highly in situ doped polysilicon used as gate electrode in the final structure, (c) 3-D view of the final structure of the fabricated device step gate SiNW FET.

Silicon dioxide (SiO₂) is used as sensing surface and the whole structure is encapsulated with silicon nitride passivation layer, except the active region (not shown in fig. 1. c), in order to ensure measurements in solutions.

3. Modeling of Metal-Insulator-Polysilicon Nanowire capacitor

3.1. Physical models

Electrical characteristics and, also, sensitivity of SiNW-based sensors are substantially influenced by the surface to volume ratio, taking into account that surface charge effects will be predominant. Modeling of Metal-Insulator-polysilicon Nanowires (MINW) capacitor (which is the basic vertical structure of the transistor) (fig.2-a) is performed to highlight this effect through the response of carrier concentration in the channel versus positive and negative charges concentration at silicon nanowire–solution interface. The numerical modeling solves the Poisson equation in order to calculate the electrostatic potential variation induced by an applied voltage. Finite element method is used to solve Poisson equation in an iterative scheme in order to calculate the electrostatic potential, calculated at all the mesh points. The specific two-dimensional mesh is adapted to the nanowire structure polysilicon (fig.2-b). The polycrystalline silicon is formed by crystallites composed of grains (considered as single crystal silicon), separated by grain boundaries, highly disordered and very narrow areas, of the order of several nanometers. This separation between two grains is very close to an amorphous silicon layer, and we use a model distribution of traps [3], taking into account the dangling bonds, tails bands and discrete traps. The mesh is very tight near the grain

boundaries because of strong potential variations near grain boundaries. Moreover, modeling takes into account all the physical parameters characterizing the structure: thickness of the various layers, permittivity, work output, silicon doping...



Figure 2: (a) Schematic structure of the Metal-Insulator-polysilicon Nanowires (MINW) capacitor, composed of 4 monocrystalline grains (width 80nm) and 5 amorphous grain boundary (2.5 nm thickness), with a 80nm gate oxide thickness. (b) Mesh capacitor, tight near the grain boundaries and at interfaces. (c) Distribution of electrons in the nanowire for different sizes (between 50 to 200nm).

Carrier concentration at any point of the nanowire is determined from the calculated potential. The electron distribution at thermodynamic equilibrium is given in fig. 2-c for nanowires ranging in size from 50 to 200 nm. We observe an accumulation of carriers at the gate oxide/silicon nanowire interface and a decrease to the outer surface. It may be noted that the distribution changes according to the size of the nanowire: electron concentration increases inversely to the size.

3.2. Influence of ions on the surface of the nanowire

For pH detection, FET channel conductance increases or decreases depending on the H^+ ionic concentration i.e. on the pH in electrolyte that modulates consequently the electrostatic surface charge of the insulator exposed to the electrolyte. The originality of the model is to predict the influence of positive or negative fixed charges present on the outer surface of the nanowire on the spatial distribution of electrons in the nanowire. Then, donor or acceptor fixed states (positive or negative states traps) located on the outer surface (fig 4-a, b) were taken into account in the simulation.



Figure 4: Schematic representation of a ions a) negative and b) positive positioned on the extern surface of the nanowire, (c) effect of these ions on the distribution of the calculated electron concentration in the nanowire (100nm). The structure here is biased with $V_G = 0.5V$

Fig4-c shows that the influence of positive charges results in an increase of electrons near the outer surface of the nanowire (and reversely depletion with negative charges). We also observe that a change in electron concentration at gate oxide/nanowire interface, i.e. in the channel: there is a slight decrease in the number of electrons when negative charges are present on the outer surface. We can deduce that H_3O^+ on the outer surface of the nanowire (acid pH) will involve increasing current at fixed gate voltage. Conversely, the current will decrease in the presence of negative charges (OH⁻ions, basic pH) at fixed gate voltage.

4. Experimental pH measurements

The measurement principle is to consider the variation of the transfer characteristic depending on the pH value of the solution, for a voltage V_{DS} =1V. Variations in the transfer characteristic (fig.5-a) are due to the presence of H₃O⁺ ions (acid pH) or OH⁻ions (basic pH). We observe a shift of the characteristics toward the positive voltage V_{GS} (i.e. increasing of the threshold voltage) when the pH increases. In other words, at a fixed gate voltage variation from acid to basic pH implies a lower current. These results correlate with those of the simulation.



Fig. 5: (a) Evolution of the transfer characteristic for different pH, (b) pH sensitivity of a sensor based on silicon nanowires

Sensitivity (fig.5-b) is given by the following equation: $S=(V_1-V_2)/(pH_1-pH_2)$. Three different sensitivities are obtained $S_1=87 \text{ mV/pH}$, $S_2=95 \text{ mV/pH}$ and $S_3=103 \text{ mV/pH}$ for respectively three arbitrary values of the current I_{DS} 50 nA, 80 nA and 100 nA. It is then important to choose the current level to obtain optimal sensitivity. However, these values are significantly larger than the Nernst maximum sensitivity limit (59 mV/pH at room temperature). One hypothesis to explain these high values of sensitivity is derived from Schönenberger *et al.* [4], which could explain this phenomenon as a capacitive amplification effect.

5. Conclusions

In conclusion, we demonstrate that nanowire field effect transistors can be used for pH detection. The modeling has shown the major influence of charges at the electrolyte/nanowire surface, correlated with experimental pH measurements. The first results are promising for the development of ultrasensitive polysilicon nanowires based pH-sensors with low-cost CMOS compatible technology.

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